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TCAD Simulation and Analysis of Drain Current and Threshold Voltage in Single Fin and Multi-Fin FinFET

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Abstract

Objectives: This study involves analysis the characteristics of Tri-gate single and double-fin FinFET. It shows the threshold voltage change due to depletion charges. Further, we investigate the effect of increasing number of fins on drain on-off current **Methods/Statistical Analysis:** In this work, it characterize leakiest path (minimum potential point in the channel) at weak inversion and strong inversion using analytical model. Here, the drain current equation is modelled by considering the effects of the depletion charges in the channel near the Source/Drain and substrate interface. Later, these results are verified using TCAD simulations. **Findings:** This model is extended for multi-fin FinFET, for analyzing the effect of increasing the number of fins and varying the thickness of fin on the drain ON (at $V_{GS}=V_{DD}$) current and drain OFF (at $V_{GS}=0$) current (Leakage current) of trigateFinFET. Finally, it analyze the corner effect in trigateFinFET and propose a solution to reduce it. **Application/Improvement:** The increase in Threshold voltage with the inclusion of depletion charges. Also, an order increase in drain ON current with two fins keeping the short channel effects minimized.

Keywords: Corner Effect, Drain Current, FinFET, Round Corner

1. Introduction

According to Moore's law[1], the number of transistors per chip increases for every 18 months, in agreement the scaling of the devices has been done to accommodate a high number of transistors on the chip. As the devices are scaled down, planar transistors have brought several detrimental effects such as gate oxide tunnelling, high leakage currents, and enhancement of Short-Channel-Effects[2]. Several independent studies conducted over the past few decades which have suggested various device architectures that offer a better solution for short channel effects and allow transistors to shrink below sub100 nm regime. Double-gate MOSFET[3] is becoming an intense subject of VLSI research because, in theory, it can be scaled to the shortest channel length possible for a given gate oxide thickness. The difficulty in fabrication of DG MOSFET (Double gate MOSFET) is encountered due to the misalignment of top gate and the back gate[4]. Hence to eliminate the misalignment of gates in DG MOSFET, FinFET[5,6] considered one of the most promising candidates for future generation transistor technologies due to their excellent electrostatic integrity such as Low leakage current, improved short-channel effect, high performance resulting from the un-doped channel structure, high carrier mobility and reduction of random dopant fluctuation. The structure for FinFET is shown in the Figure 1. With the scaling of the devices, the fins needed to be thinner due to which scattering of dopants increases. Hence, lightly doped fins are preferred to reduce the scattering or random dopant fluctuations[7]. For the tri-gate rectangular FinFET(TG-ReFinFET), there are several drain current model proposed[8], but these models do not account for the effect of depletion charges which is taken into consideration in this paper. Due to thinner fins, the drain current is reduced as the charge carriers participating in the on current are lesser. So to increase the drain current, the number of fins has to be increased.

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In this paper, it has introduced a model of drain current for multi-fin FinFET. Finally, it analyzed the effect of corners on device performance.

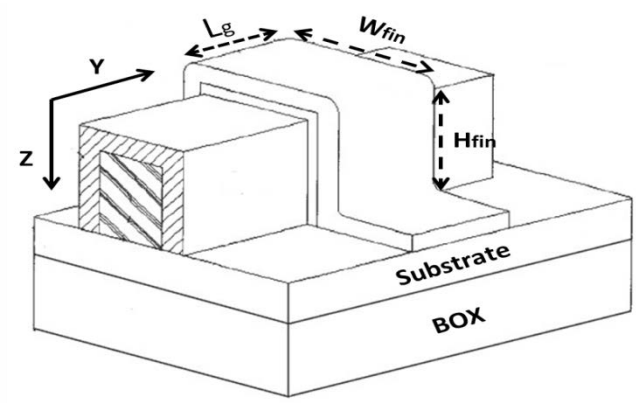

Figure 1. Schematic view of trigateFinFET.

This paper is organized as follows-Section 2 describes the device architecture and the simulation setup used in this study. In Section 3, we present the complete analysis of current flow including depletion charges and present a compact model for trigateFinFET. Section 4 shows the obtained results and discussion on corner effects. Finally, in section 5 we concluded this work.

2. Device Architecture and the Simulation Set-Up

In the FinFET device the conducting channel is raised up into a 'fin' with the gate wrapped around it in a 3-dimensional structure. The fundamental advantage of a FinFET is, having channel from all 3 sides, the controllability of gate over channel increases and the device can be switch on-off quickly. The drive current is more in TG-FinFET as compared to DG-FinFET and the effective width of TG-FinFET is W_{eff}= n× (2×H_{fin}+W_{fin}). Here 'n' is the number of fins and n=1 for single fin FinFET, the main drawback of single-fin FinFET is the lower drive current due to thinner fins as in comparison to other architectures. However, the increased thickness of fins leads to increase in short channel effects. Hence, here multi-fin structure to increase the number of fins on the same substrate as shown in Figure 2 and thus, it improve the effective width of the fin without increasing the width of the single fin and hence the drive current increases with minimum short channel effects.

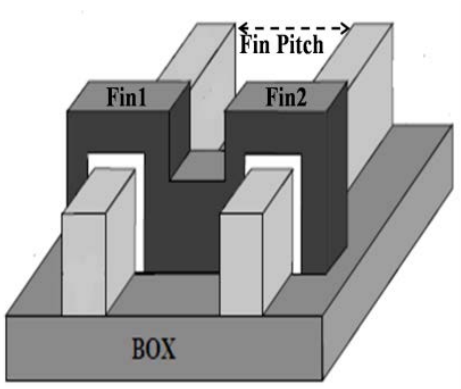

Figure 2. Schematic view of double fin FinFET.

Table 1. Parameters used for simulations

Parameters	Value used
silicon width W_{fin}	30nm, 10 nm
Silicon height H_{fin}	20nm
Gate-oxide thickness	1nm
Gate work function	4.5eV
Channel length	50nm
Source/Drain doping	$1x10^{20}$ cm^{-3}
Channel doping	$1x10^{18}$ cm^{-3}

The device dimensions are shown in Table 1. The device structure has been made with 3-D TCAD Tool Cogenda Genius.

3. Analysis of Current Flow and Compact Model of TrigateFinFET

In the weak inversion region of TG-FinFET the leakiest path exists in the bottom centre of the channel[9]. At lower gate voltage, the effect of the gate decreases when it moves away from the gate. By increasing the gate voltage the channel starts moving from bottom centre to silicon-to-oxide interface. In TG-FinFET, the height of the fin is greater than the width of the fin; hence each half of the top gate width contributes to channel formation with the side gates. The gate covers channel through all three sides. So, the leakiest path exists at the bottom centre which is far from all three gates and the effect of drain potential is higher at that point as shown in Figure 3. This is due to the fact that channel first forms at bottom centre of

the silicon substrate and this phenomenon is known as volume inversion.

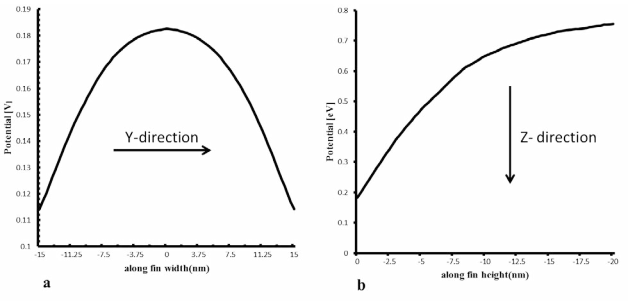

Figure 3. Potential graph at weak inversion (a) along the fin width (y direction) showing that the maximum potential at the middle of the fin (b) along the fin height (z direction) showing that the maximum potential at the bottom of the fin.

The overall current equation of TG-FinFET can be derived from DG-FinFET[10] with few modifications and including channel length modulation given by Equation 1[11].

$$I_d = \mu_0 2W_{eff}\frac{\varepsilon_{ox}}{t_{ox}}\left(\frac{2kt}{q}\right)^2\left[\frac{(q_{is}-q_{id})}{L}+\frac{1}{2}\frac{(q_{is}^2-q_{id}^2)}{L-\Delta L}\right] \quad (1)$$

Here ΔL is gap between L and channel pinch-off point. L is the physical length of the channel, μ_0 is the low field electron mobility,ε_{ox} is permittivity of oxide and t_{ox} is thickness of oxide, q_{is} and q_{id} are normalized inversion sheet charge density at the source and drain side which is given in terms of Lambert W function by Equation 2.

$$q_{ix} = \text{Lambert W}\left[e^{\frac{(V_g-V_t-V_x)}{2V_{th}}}\frac{e^{\frac{(V_g-V_t-V_x)}{2\eta'_{TG}V_{th}}}}{A+e^{\frac{(V_g-V_t-V_x)}{2\eta'_{TG}V_{th}}}}\right] \quad (2)$$

A is given by Equation 3

$$A = \frac{4e^{\frac{V_t+V_{fb}}{Vo}}}{e^c} \quad (3)$$

V_o is 1V, V_x is the channel voltage, and at source side and it is 0V and at drain it is V_d, V_{th} is thermal voltage which is KT/q, V_t is threshold voltage and $\eta'_{tg} = \eta_{tg}/(\eta_{tg}-1)$is the sub-threshold switch coefficient. The threshold voltage given by Equation 4 is[12]

$$V_t = V_{fb} - \frac{A_{1,TG}(V_{bi}+V_d)+A_{2,TG}V_{bi}}{1-(A_{1,TG}-A_{2,TG})} + \frac{V_{th}}{1-(A_{1,TG}-A_{2,TG})}\ln\left(\frac{Q_{th}N_a}{n_i^2 W_{fin}}\right) \quad (4)$$

Where $V_{fb} = \Phi_{ms} - V_{th}\ln(N_a/n_i)$ is flat band voltage, Φ_{ms} is the work function difference between metal and silicon, V_{bi} is built in potential calculated by $V_{bi} = \frac{kt}{q}\ln(N_d/n_i)$. In this model the effect of depletion charges is neglected. If the substrate is highly doped than the effect of depletion charges came into effect which affects the built in potential as well as threshold voltage, thus this effect should be modified as explained below.

The modified V_t and V_{bi} are given by Equation 5 and 6

$$V'_t = V_{fb} - \frac{A_{1,TG}(V'_{bi}+V_d)+A_{2,TG}V_{bi}}{1-(A_{1,TG}-A_{2,TG})} + \frac{V_{th}}{1-(A_{1,TG}-A_{2,TG})}\ln\left(\frac{Q_{th}N_a}{n_i^2 W_{fin}}\right)+\frac{Q_d}{C_d} \quad (5)$$

$$V'_{bi} = V_{th}\,\text{Ln}\left[\frac{N_a N_d}{n_i^2}\right] \quad (6)$$

N_a and N_d are acceptor and donor charge densities and n_i is intrinsic silicon charge concentration, Q_i is the inversion charge, and Q_d is the depletion charges and C_d is depletion capacitance of the order of fem to farad given as:

$$Q_d = 0.5qN_a W_{fin}, C_d = \frac{C_{si}C_{box}}{C_{si}+C_{box}}$$

$A_{1,TG}$, $A_{2,TG}$ are the parameters which are the functions of natural length and channel length and it has finite values for short channel devices but for long channel devices their values are 0.Q_{th} is the minimum inversion charges required to form the channel is given by Equation 7.

$$Q_{th} = \frac{2V_{th}}{q}\times\frac{C_{ox}^2}{C_{si}} \quad (7)$$

Where C_{ox} and C_{si} is capacitance of oxide and silicon respectively which is given as $C_{ox} = \varepsilon_{ox}/t_{ox}$ and $C_{si} = \varepsilon_{si}/W_{fin}$. In the above model of current the switching parameter should be used to get the correct graph when the device is switching from weak inversion to the strong inversion. Switching parameter for TG-FinFET is modified and given by Equation 8.

$$\text{issTG} = C_1 + \tanh\left(C_2\times\left(V_g+\Delta V_t-V_t\right)\right) \quad (8)$$

C_1 and C_2 are the fitting parameters. Hence the new drain current equation proposed by us is given by Equation 9.

$$I_d = \mu_o 2W_{eff}\frac{\varepsilon_{ox}}{t_{ox}}(2V_{th})^2\left[\frac{(q_{is}-q_{id})}{L}+\frac{1}{2}\frac{(issTG)(q_{is}{}^2-q_{id^2})}{L-\Delta L}\right] \quad (9)$$

The comparison of new drain current equation given by Equation 9 and simulation results is shown in Figure 4. From the simulation the values of C_1 and C_2 is found to be 0.01 and 0.5, Q_{th} should be in the order of 1E17 and ratio of Q_d/C_d is equal to 0.001V. Here the mid-gap metal gate is used.

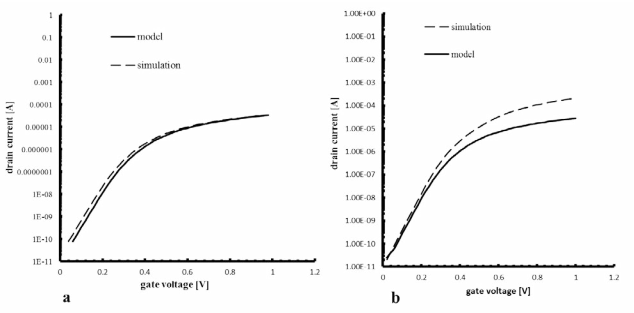

Figure 4. Drain current versus gate voltage (a) single fin FinFET(b) double fin FinFET at Vd=.6, tox=1nm dash line representing simulation results and continuous represents model result.

The change in the threshold voltage due to depletion charge effect is shown in the Figure 5. Threshold voltage without depletion charge effect was 0.30 V and with depletion charge is 0.32 V.

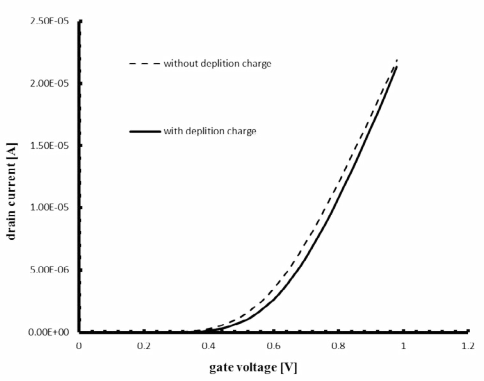

Figure 5. Simulation result of threshold voltage change due to depletion charge effect.

4. Results and Discussions

In order to increase the drive current, multi-fin FinFET is used. The drain current equation given Equation 9 can be extended to multi-fin FinFET by changing Weff = n(Hfin +Wfin/2). The simulation results for the multi-fin FinFET with current model is shown in Figure 6. Here two fins are used for simulation hence n=2. Clearly current is almost double for double fin structure as compared with the single fin because the equivalent fin width increases keeping short channel effects under control.

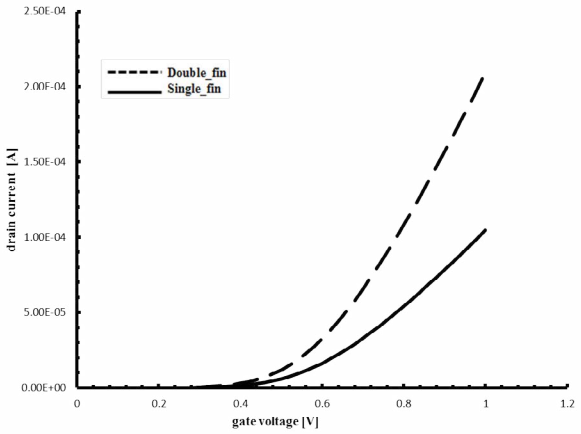

Figure 6. Drain current versus gate voltage of double fin and single fin at V_d=0.6V.

4.1 Impact of Fin Thickness

As the dimensions of the device are scaled down the oxide thickness is also been scaled but due to the scaling of oxide, tunneling current increases. So the concept of natural length evolved in representing the impact of penetration of drain electric field in the channel. The basic formula of natural length is given by Equation 10[13].

$$\lambda = \sqrt{\frac{\varepsilon_{si}t_{si}t_{ox}}{\eta\varepsilon_{ox}}} \quad (10)$$

η is the constant used for different structures, η is equal to two for double gate mosfet. t_{si} is the fin width and is proportional to square root of the product of device body thickness and gate oxide thickness, therefore by decreasing the substrate thickness it can decrease the short channel effects. The comparison of results for two different thicknesses is shown in Figure 7 and obtained parameters are shown in Table 2.

Table 2. Results at V_d =.6V for t_{si} =10nm and t_{si}=30nm

Parameters	Value at t_{si}=10nm	Value at t_{si}=30nm
I_{on}	1.23E-05 A	1.72E-05 A
I_{off}	1.7E-013 A	5.12E-08 A
DIBL	0.08 mV/V	0.33 mV/V
V_t	0.32 V	0.18 V

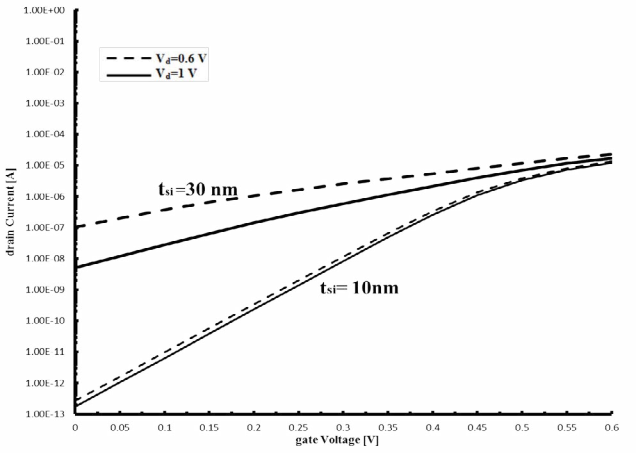

Figure 7. Drain current versus gate voltage for two different drain voltages at t_{si}=30nm and 10nm.

4.2 Corner Effect

In strong inversion region, in highly doped TG-FinFET, the leakiest path is shifted to the corners[14] where the maximum gate voltage is observed because of electric field fringing due to the coupling of the top gate and side gates as shown in Figure 8. It can be concluded that the potential and electron density is more at the corners and hence, corners offer lower threshold voltage as compared to the channel threshold voltage due to which leakage occurs[15]. This problem has become more severe as it go deep into submicron technologies. In strong inversion region, in highly doped TG-FinFET the leakiest path is shifted to the corners where the maximum gate voltage is observed because of electric field fringing due to the coupling of the top gate and side gates as shown in Figure 8. This problem can be solved by making the corner rounds[16] as shown in Figure 9. Comparison of electron density and potential along the fin width in round corner TG-FinFET is shown in Figure 10. From the Figure 10, it can be concluded that by making round corners of the fin, the potential, and the electron density will become almost equal as along the width due to which the leakage, because of an extra channel formed at the corners will be reduced.

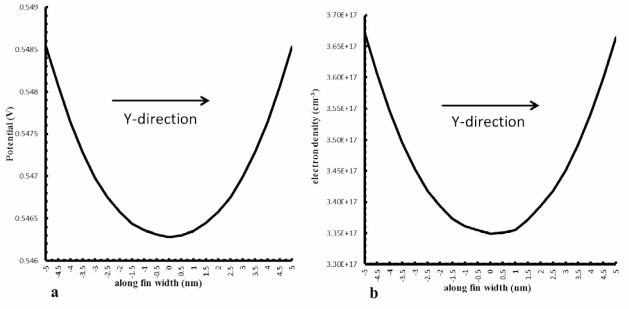

Figure 8. Plot for the Potential and Electron density profile at strong inversion along the fin width (y direction) showing that the maximum potential and electron density appears at the corners of fin.

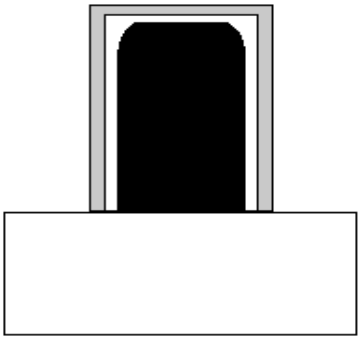

Figure 9. Schematic view of TG-FinFET with corner round.

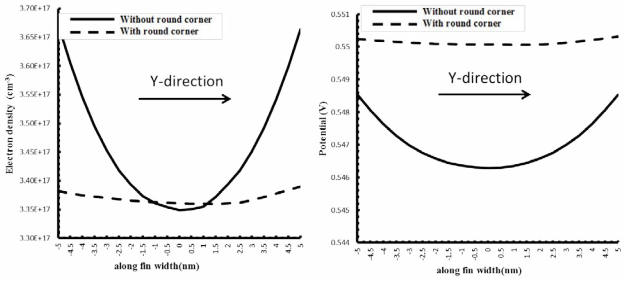

Figure 10. Plot for the Electron density and Potential profile at strong inversion along the fin width (y direction) for round corner tri gate FinFET.

5. Conclusion

This paper analyzes the effect of increasing number of fins of the TG-FinFET on the same substrate. Increasing the number of fins increases the drain current without

increasing the short channel effects. Further, it observes the effect of depletion charges in the channel due to which threshold voltage of the device increases. Effect of depletion charges can be reduced by lowering the substrate doping. The effect of corners in the FinFET device as corners are responsible for most of the leakage. It is found that making round corners the leakage can be reduced.

6. References

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