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Analysis of XOR Circuits for Ultralow-Power Applications in Deep Subthreshold Region

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Abstract

Objectives: This paper analyses various Complementary MOS (CMOS) based XOR circuits in terms of their output voltage levels at deep subthreshold/low frequency region at 16-nm technology node and finds out the suitable XOR circuit for ultralow-power applications. Methods/Analysis: It also provides the worst case high and low output level for various XOR circuits at supply voltage 130 mV. Findings: In addition, it compares the average power dissipation that is the sum of both dynamic and leakage power dissipation (stand-by power dissipation) of XOR circuits along with the variability analysis of power dissipation in order to find the XOR circuit which is most robust and dissipate the least average power. Novelty/Improvement: Simulation result shows that Power-less XOR circuit is having a good output high and low level in all cases and most promising in terms of robustness and average power dissipation among all the other XOR circuits at deep subthreshold/low frequency region of operation.

Keywords: Average Power Dissipation, CMOS, Low Frequency, Subthreshold Region

1. Introduction

With the evolution in battery operated devices (that is portable and wearable devices), personal communication systems like smart phones, net-books, tablets and the advancement in scalable technology, the endeavors in research in ultralow-power is exaggerated. In the recent times, portable applications that need less area and are designed using ultra-low power circuitry[1]. Power dissipation that is caused because of scaling the technology offered better improvement as the technology generation is changing. Nevertheless, power-density is extremely increased, since the existing system-on-chips are integrating trillion of devices on a miniaturized chip[2]. Circuits operating in subthreshold region can solve this issue. The absolute value of gate to source voltage (V_{GS}) in subthreshold region of operation is smaller than the threshold voltages of the transistors. Hence the device is weekly driven by the gate voltages at subthreshold region. These transistors consume less amount of energy and even dissipate less power than their higher voltage substitutes, at trade-off with speed. Hence, the circuits operated in subthreshold region can be a decent choice for ultralow-power applications where speed is considered as secondary performance[3,4]. For example all portable applications like micro-sensor nodes, ultra-low-power Digital Signal Processors (DSP) in portable devices like smart phones, and other bio-medical devices like stimulators opt for non-performance critical operations[4] with extended battery life. Even other examples like wrist watches and hearing-aids are also battery operated devices that require CMOS circuits in their design that are operated in subthreshold as well as deep-subthreshold regions which operate at very low frequencies approximately at 1 Hz. Hence, there is a requirement of investigation of those circuits which operate properly at deep subthreshold/low frequency region with full output swing. XOR circuit is one of the most fundamental and essential building blocks of complex arithmetic circuits[5]. It is also broadly implemented in circuits like shift register, compressors, and phase detectors[6,7]. According to the above point of view this research paper affords

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to give design strategies for the circuit designers, who can aptly select an appropriate CMOS based XOR circuit for ultralow-power applications with proper functionality with minimum energy consumption. XOR gate also finds its application in pseudo-random number sequence generators, specifically in Linear Feedback Shift Registers (LFSR). In other words, XOR gate models an LFSR, in order to generate random numbers (used for testing chips).

The paper is structured in the following manner. Simulation setup along with the truth table of XOR gate is given in Section 2. Section 3 provides the analysis of various XOR circuits used in this paper along with their circuit diagram. Simulation results including tables and graphs are given in Section 4. Lastly, conclusions are drawn in Section 5.

2. Simulation Setup

Extensive simulations are performed in SPICE environment at 16-nm node at a very low frequency of 1 Hz and the supply voltage used is in the range of 130 mV down to 100 mV. This simulation setup uses using Predictive Technology Model (PTM)[8]. According to ITRS (International Technology Roadmap for Semiconductors) guidelines, it shows up to a range of ±10% variations in device parameters which include channel length (L), channel width (W), oxide thickness (t_{OX}), threshold voltage (V_t), carrier mobility (μ_0) and channel doping concentration ($NDEP$)[9]. For the purpose of variability analysis, Monte Carlo simulations with 5000 run are performed by varying the above device parameters and generating different SPICE model files for each set of parameters at 16-nm technology. The above mentioned parameters are assumed to have independent Gaussian distributions with 3σ variation of 10%[10]. The channel length of all the transistors is set to 16 nm and the width of the device is varied as per the requirement. In order to get the power dissipation as low as possible, minimum possible size is taken for all the transistors[11]. Aspect ratio (W/L) of each transistor is given in the circuit diagrams illustrated in the later section. Simulation framework for the analysis of all the XOR circuits is shown in Figure 1.

In order to generate real scenario, the inputs and outputs of XOR circuit under test is loaded with the XOR gates with one of the input fixed at Logic 0. XOR gate with one input fixed at Logic 0 acts as a buffer which can be verified with the help of truth table as shown in Table 1.

3. Analysis of various XOR Circuits

3.1 INV-XOR Circuit

XOR circuit in Figure 2 consists of only 4 transistors (2 pMOS and 2 nMOS) but it does not show good output waveform for inputs (A = 1, B = 0) and (A = 0, B = 0) because of following reasons. When (A = 1, B = 0) pMOS MP1 is ON and value at node X is pulled up to logic high value and through nMOS MN2 which is also ON this high voltage is passed to the output. But as the voltage level at output increases Gate to source voltage (V_{GS}) of MN2 decreases much less than the threshold voltage (V_t) of nMOS transistor and hence the strength of leakage current flowing through MN2 becomes weaker and the output voltage rise to 108 mV only. When (A = 0, B = 0) pMOS MP2 is ON and high output voltage discharges to

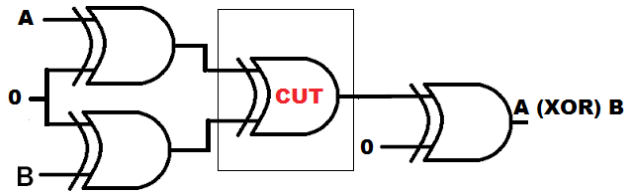

Figure 1. Simulation framework for the analysis of XOR circuits.

Table 1. Truth table for working of XOR gate

A	B	A (XOR) B
0	0	0
0	1	1
1	0	1
1	1	0

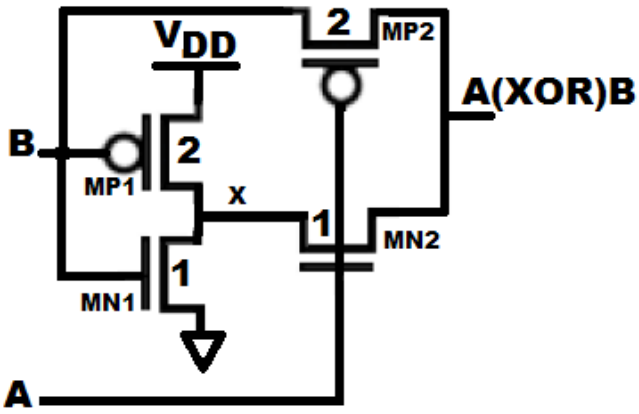

Figure 2. INV-XOR circuit[12].

low through transistor MP2. As the source voltage for MP2 decreases absolute value of gate to source voltage ($|V_{GS}|$) for MP2 increases which weakens the strength of leakage current flowing through MP2. Therefore the output voltage becomes stable at 36 mV instead of zero. Apart from output voltage level power dissipation of this design is also high as compared to other circuits. Hence, this circuit cannot be used as an option for ultralow-power applications in deep subthreshold region.

3.2 4T PTL based XOR Circuit

XOR circuit in Figure 3 also consists of 4 transistors (2 pMOS and 2 nMOS) but does not show good output waveform for inputs ($A = 0$, $B = 1$) and ($A = 0$, $B = 0$) because of following reasons. When ($A = 0$, $B = 1$) pMOS MP1 is ON and the value of node X becomes high which passes through nMOS transistor MN2 to rise the output voltage to high value. But due to increase in source voltage of transistor MN2 and decrease in the value of (V_{GS}) as compared to its threshold voltage (V_t) the output high level can only rise to 106 mV. Similar is the situation with the pMOS transistor MP2 when input is ($A = 0$, $B = 0$) where output voltage of the XOR circuit only decrease up to 33 mV instead of 0 mV. Power dissipation of this circuit is also high as compared to other circuits. Hence, it is also not suitable for ultralow-power application.

3.3 7T XOR Circuit

XOR circuit in Figure 4 consists of 7 transistors (3 pMOS and 4 nMOS) as shown. This circuit also shows bad output high level that is 111 mV instead of 130 mV when the input voltage is ($A = 0, B = 1$). This is because when ($A = 0$) pMOS MP3 is ON which rises the output to a high value but at the same time node X is high and transistor MN2 is also ON which discharges the output to a value lower than the supply voltage. Power dissipation of this circuit is better than the previous circuits due to less static power dissipation but still it is not the best option for the designers.

3.4 PTL XOR Circuit

XOR circuit in Figure 5 consists of 6 transistors (3 pMOS and 3nMOS). The two nMOS transistors (MN1 and MN2) are connected in cross coupled fashion as shown. This design shows the good output high and low level in all the input cases (122 mV as worst case high and 12 mV as worst case low) but the average power dissipation of this circuit is highest among all the other circuits. Hence, although it performs reliable operation it cannot be a good option for the designer in the designs which require very less power dissipation.

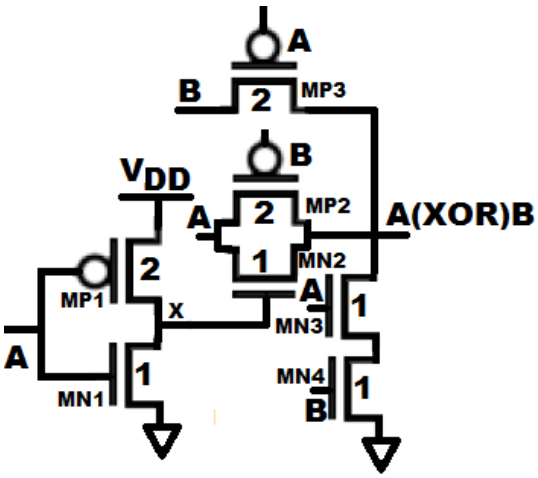

Figure 4. 7T XOR circuit[13].

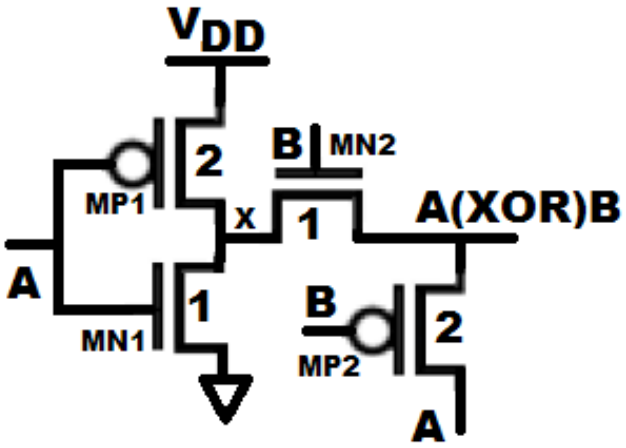

Figure 3. 4T PTL based XOR circuit[14].

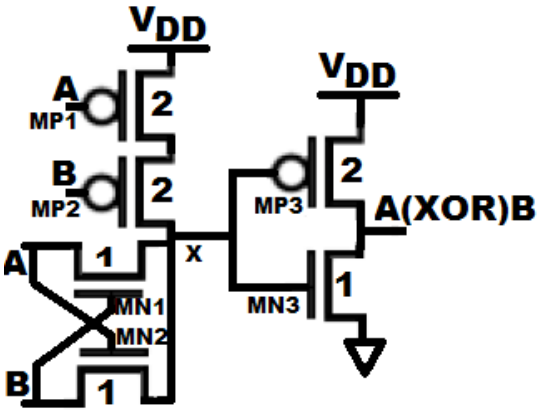

Figure 5. PTL XOR circuit[7].

3.5 Power- Less XOR Circuit

XOR circuit in Figure 6 consists of only 4 transistors (2 pMOS and 2 nMOS). In this design there is no V_{DD} supply voltage hence it is called Power-less XOR circuit. The output high and low level of this design is good in all the input cases (122 mV as worst case high and 07 mV as worst case low). This XOR circuit design also shows the least average power dissipation as compared to all the XOR circuits. This design is the most robust in terms of variability in power dissipation as it shows the least spread in power dissipation due to PVT variation as compare to other designs. Hence, Power-less XOR circuit is best option for the designers for the ultralow-power applications in deep subthreshold/ low frequency region.

4. Simulation Results

This section presents simulation results of the circuits considered in this work. Table 2 provides the worst case output high and low voltage values and Figure 7 shows the corresponding output waveforms of different XOR circuits at V_{DD} = 130 mV with input frequency of 1 Hz. Power-less XOR circuit shown in Figure 6 shows the reliable output voltages as compared to other circuits.

Table 3 provides the average power dissipation of various XOR circuits and Table 4 shows the variability of power dissipation at supply voltage ranging from 100 mV-130 mV and the corresponding curves are also shown in Figure 8 and Figure 9 respectively. Simulation results shows that XOR gate in Figure 6 dissipates the least average power and shows least spread in average power dissipation whereas XOR gate in Figure 5 dissipates the maximum average power and XOR gate in Figure 4 shows the maximum spread in average power dissipation.

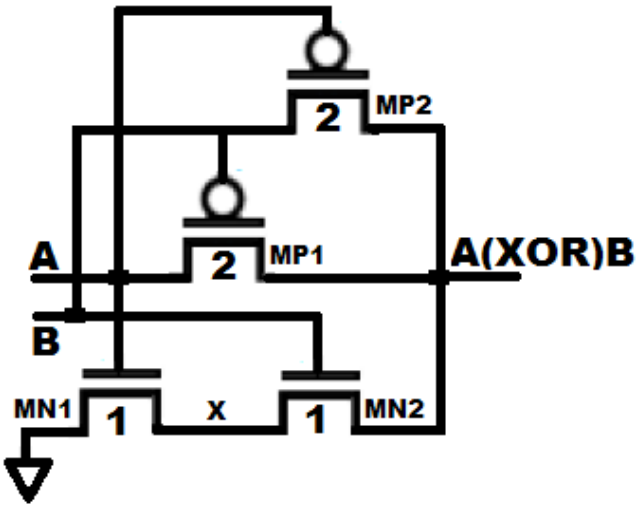

Figure 6. Power-less XOR circuit15.

Table 2. Comparison of worst case output voltage levels of different XOR circuits @V_{DD} = 130 mV

XOR circuits	Worst case high (max=130 mV)	Worst case low (min=0 mV)
Figure 2	108 (A = 1,B = 0)	36 (A = 0, B = 0)
Figure 3	106 (A = 0, B = 1)	33 (A = 0, B = 0)
Figure 4	111 (A = 0, B = 1)	11 (A = 1, B = 1)
Figure 5	122 (A = 0/1,B = 0/1)	12 (A = 0, B = 0)
Figure 6	122 (A = 0/1,B = 0/1)	07 (A = 1, B = 1)

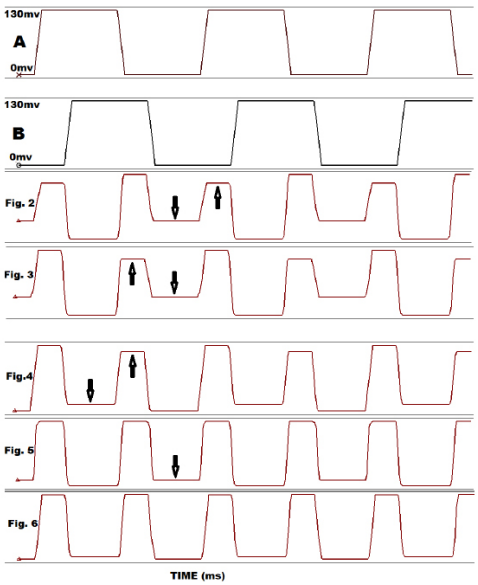

Figure 7. SPICE simulation waveform of the XOR circuits @ V_{DD}=0.13V with input frequency of 1 HZ. First two waveforms is of input *A* and *B* and rest of the waveforms are of A (*XOR*) B output of various XOR circuits.

Table 3. Comparison of average power dissipation of different XOR circuits at different supply voltages

Voltage	100 mV	110 mV	120 mV	130 mV
Figure 2	7.192e–12	9.015e–12	1.115e–11	1.362e–11
Figure 3	7.099e–12	8.912e–12	1.103e–11	1.350e–11
Figure 4	6.015e–12	7.494e–12	9.229e–12	1.126e–11
Figure 5	1.270e–11	1.629e–11	2.056e–11	2.560e–11
Figure 6	1.020e–13	1.110e–13	1.322e–13	1.551e–13

Table 4. Comparison of variability of avg. power dissipation of different XOR circuits at different supply voltages

Voltage	100 mV	110 mV	120 mV	130 mV
Figure 2	0.450	0.460	0.472	0.485
Figure 3	0.454	0.464	0.475	0.488
Figure 4	0.467	0.481	0.496	0.512
Figure 5	0.448	0.462	0.466	0.478
Figure 6	0.154	0.160	0.168	0.179

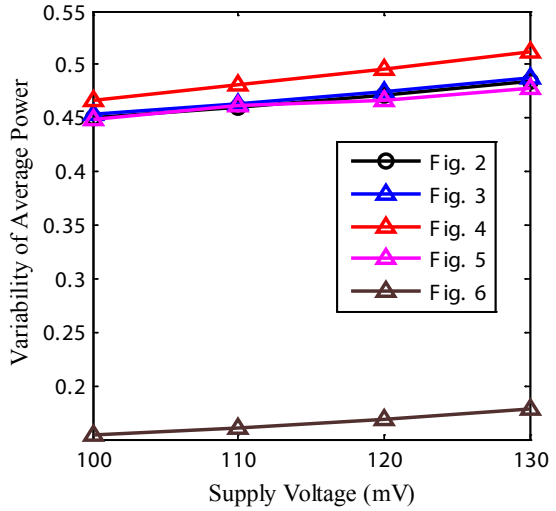

Figure 8. Comparison of average power dissipation of different XOR circuits @ different supply voltages.

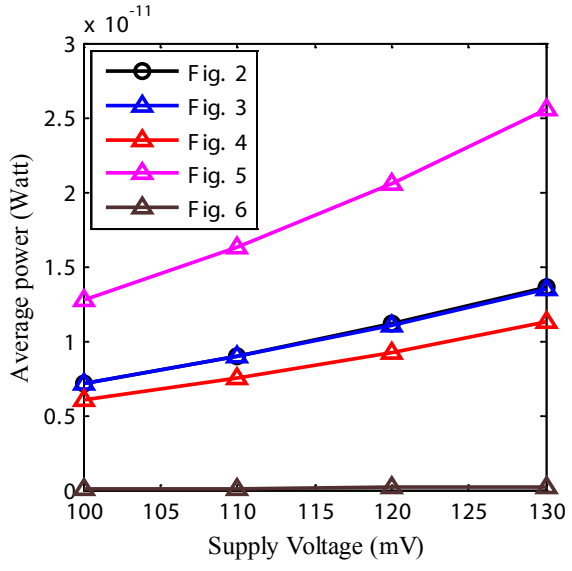

Figure 9. Comparison of variability in avg. power dissipation of different XOR circuits @ different supply voltages.

5. Conclusions

This research work fruitfully investigated different CMOS based XOR gates in order to find the XOR circuit which shows good output high and low level and also dissipates the least average power in deep-subthreshold/low frequency region of operation at supply voltages ranging from 100 mV–130 mV and at a frequency of 1Hz for ultralow-power applications. This work also offers the variability analysis of power dissipation of various XOR circuits to find the most robust design which exhibits better characteristics. Power-less XOR circuit exhibits acceptable output voltage levels with full output swing and dissipates lesser average power as compared to other XOR gates. In addition to that, Power-less XOR is found to be most robust as it shows least variability of power dissipation. Hence, Power-less XOR circuit can be a better choice for the circuit designer for ultralow-power applications.

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