Indian Journal of Science and Technology, Vol 9(40), DOI: 10.17485/ijst/2016/v9i40/94646, October 2016
ISSN (Print) : 0974-6846
ISSN (Online) : 0974-5645

Implementing All-Optical New Reversible Gate using SOA-MZI Architecture

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Abstract

Reversible circuits have gained a lot of attention lately because of its remarkable property of dissipating lesser power as compared to irreversible circuits due to the fact that they do not lose information. Because of continuing revolution in VLSI technology transistor count and thus power dissipation has increased to such an extent that it has put a limit on packing density and performance of the circuits. To overcome these limits reversible logic has came into picture and various reversible logic gates such as Feynman gate, Fredkin gate, Toffoli gate, Peres gate etc has already been designed in optical domain. Semiconductor optical amplifier (SOA) based mach-Zehnder interferometer (MZI) plays a promising role in this field of ultra fast all-optical information processing because of its advantages like high speed, low power, easy of fabrication and fast switching time. Thus various circuits designed by these basic gates has been analysed in terms of cost parameters and it was seen that optical cost and delay of digital circuits is more than desired, as a result performance of system is rendered. Thus new gates are designed by various researchers that focus on improving cost and thus performance of the system. Studying all these modified gates and the digital circuits implemented in literature, an idea of *New All-optical universal reversible gate* has been proposed which will further improve the performance of digital circuits. Applications of this gate include the design of full adder, half adder, multiplexer and various other combinational circuits and also 13 standard Boolean expressions can be implemented with improved cost. Simulation of this new gate is done using VPI Photonics software.

Keywords: All-Optical Communication, Reversible Gates, Mach Zehnder Interferometer, Semiconductor Optical Amplifiers

1. Introduction

With the advancements in all-optical computing technology, researchers have been paying more attention towards designing low-power applications. All-optical computing means there will be no optical-electrical-optical converters needed in the design and signal will remain photonics throughout its path. Advantage of this will be that, the increasing bandwidth requirements will be met and also 30% of energy will be saved which is otherwise wasted to convert electrons to protons and then back to electrons. Low power designs are also required because according to[1], numbers of transistors on an integrated circuit (IC) are doubling every 18 months. Reversible logic plays an important role in reducing or even eliminating the power dissipation in a circuit because there is no loss of information in processing the data and original data can be retrieved at any stage of computation. These are special type of logic functions where input vectors are one-to-one mapped with the output vectors i.e. the number of inputs will be same as the number of outputs[2]. The concept of reversibility was first introduced by[3,4]. According to Laundeur, every irreversible bit will dissipate energy in order of **kT** which later came out to be **kTln2** joules. So researchers are focussing on designing logic gates which are reversible and are all-optical in nature.

Various reversible logic gates like Feynman gate, Toffoli gate, Peres gate, Fredkin gate etc, already exist in literatures which are designed using SOA-MZI switch in[5-7]. These gates have been designed taking into account

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the parameters such as MZI switch count in designed circuit, number of beam splitters (BS), beam combiners (BC) and Optical delay which are also termed as cost parameters. Optical cost and delay for BC and BS are negligible, so it is not taken into account while calculating the overall optical cost and delay of the circuit. Several combinational circuits have been designed using these gates and are analysed in terms of cost parameters stated above. Attempt has been made by several researchers to reduce the MZI switch count and delay of these existing circuits by designing new gates or modifying the existing gates.

2. Reversibility

Reversibility means that there is bijective mapping[8] between the input and output vectors and also number of inputs should be equal to number of outputs. To maintain reversibility constant inputs and garbage outputs are required[9]. The constant input in the reversible circuit is also called as ancilla input. Both ancilla input and garbage output are a necessary part of reversible circuit. They are indispensable to realize any balanced logic function. Therefore minimizing the reversible gate count and garbage outputs produced are prime objectives in any reversible circuit[10].

There are two limitations that need to be taken care of while realizing a reversible circuit. Firstly fan out is not allowed, i.e. outputs from one stage cannot be used as input to the next stage. Secondly loops are not allowed in combinational circuits.

3. SOA-MZI Architecture

Semiconductor optical amplifier (SOA) based Mach-zehnder interferometer (MZI) switch is widely used architecture lately, to design all-optical reversible circuits because of its advantages like low energy requirements, fast switching time, high speed, compact size and ease of fabrication. Mach-zehnder interferometer is a device used for calculating phase shift introduced between two arms of interferometer with the help of change in refractive index of the medium[11]. Two couplers connected by arms of unequal optical length are used for creating a phase shift. Two input ports have corresponding two output channels i.e. upper channel and lower channel. First input port is given incoming signal and the second input port is given control signal both having different wavelengths and different laser power levels. It also has input coupler (50:50) to combine both the signals and split them into two arms of the interferometer and an output coupler (50:50) is used to later recombine these signals and split them into output channels[12].

Semiconductor optical amplifiers use a semiconductor for providing the gain medium. Latest SOA designs are based on anti-reflective coatings and tilted waveguide and window regions due to which end face reflection is reduced to less than 0.001%. Signal amplification is also done due to active region inside SOA without first converting the signal into electrical signal, i.e. directly the optical signal is amplified. MZI is integrated with SOA and this configuration is advantageous over other configuration because of the property of non linearity of SOA[13].

To make MZI an ultrafast optical switch, two semiconductor amplifiers are introduced in two arms of the MZI as shown in Figure 1 and this structure is termed as SOA-MZI architecture**.** Switching of incoming signal depends on the saturation of two semiconductor optical amplifiers (SOA's) which further depends on the amount of light entering into arms.

The principle on which this switch works is explained as follows:

- When both input port shave light i.e. when control signal is present, it saturates the SOA-1 and changes its refractive index which is given by $\Delta n = n.I$ where n is the refractive coefficient and I the intensity of light incident[14]. SOA-2 is still unsaturated thus the light will be present on the upper channel i.e. bar port and no light will be present at the lower channel.
- When incoming signal is high and control signal is low, both SOA's will be unsaturated thus no light will be present at the upper channel. Only the lower channel i.e. cross port receives light
- In all other cases there will be no light at any of the output channels.
- To block the control signal blocking filters (F) are placed at both the output ports.
- The logic value 0 and 1 represent the absence and presence of light respectively. This behaviour of MZI switch can be represented as

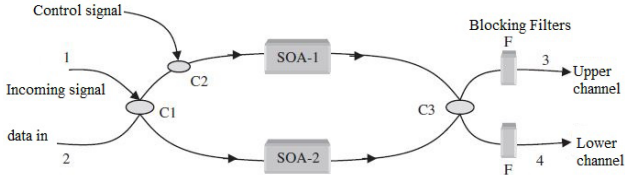


Figure 1. SOA-MZI switch architecture[5].

- X (upper channel) =$P.\overline{Q}$
- Y(lower channel) = $P.\overline{Q}$

This operation is also signified in the output waveforms shown in Figure 2 which are recorded in VPI PHOTONICS software. Here incoming signal is given a clock stream which produces PRBS (pseudo random bit sequence) of one's (11111111…1). Control signal is given clock stream which produces 10101010…10 streams of data. 'Data in' input is kept open. Here the output pulses of upper channel and lower channel are little time shifted and this delay is in nanoseconds (nS).

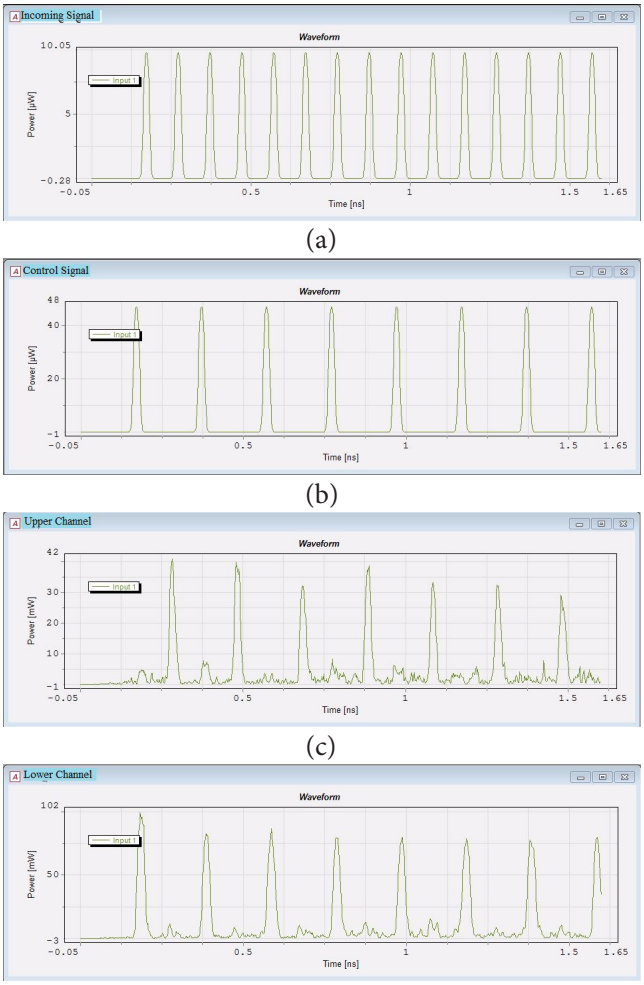


Figure 2: **(a)** Incoming Signal **(b)** Control Signal **(c)** Output at Upper Channel **(d)** Output at Lower Channel.

4. Basic Reversible Logic Gates

A circuit is said to be reversible if it is built of cascade of reversible logic gates and there cannot be any feedbacks or fan outs permitted. Thus basic building blocks are reversible logic gates, which are built in optical domain using SOA-MZI switch. There are many basics gates which already exist in literature like Feynman gate, Toffoli gate, Peres gate etc which can produce any Boolean function and are discussed below.

5. All Optical Feynman Gate

Feynman gate is the most basic reversible gate having simple XOR operation with two inputs and two outputs. If Input vectors are I= (P, Q) then corresponding output vector will be O= (X=P, Y= P ⊕ Q)**.** This gate can also work as a buffer if input Q=0 and as a NOT gate if input Q=1. Design of 2x2 Feynman gate using MZI switch is shown in Figure 3.

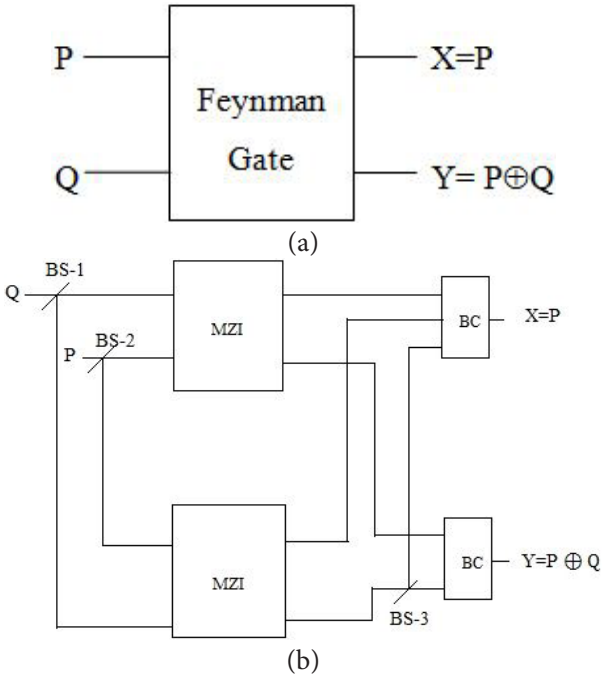


Figure 3: **(a)** Feynman Gate **(b)** Schematic using SOA-MZI switch[6].

In this gate MZI switch count came out to be 2, therefore it has optical cost of 2. Number of beam combiners (BC) used are 2 and number of beam splitters (BS) used are 3 and optical delay of this gate came out to be 1Δ as both MZI switches works in parallel.

6. All Optical Toffoli Gate

Toffoli gate is a 3X3 reversible gate with basic operation again as XOR. If the input vector is I= (P, Q, R) then the corresponding output vector for this gate will be O= (X=P,

Y=Q, Z=P.Q⊕R). Design of 3X3 Toffoli gate using MZI switch is shown in Figure 4.

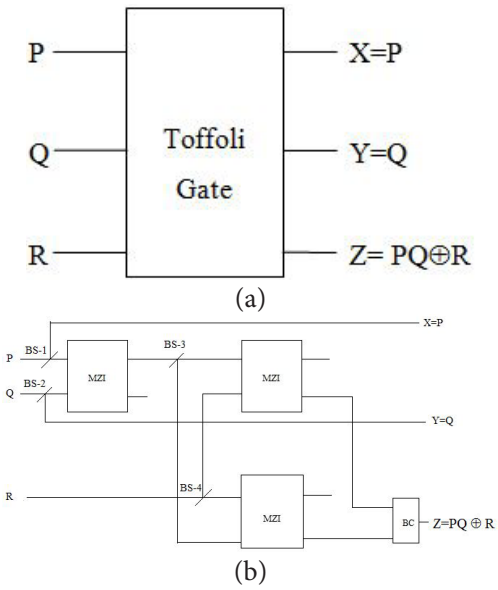
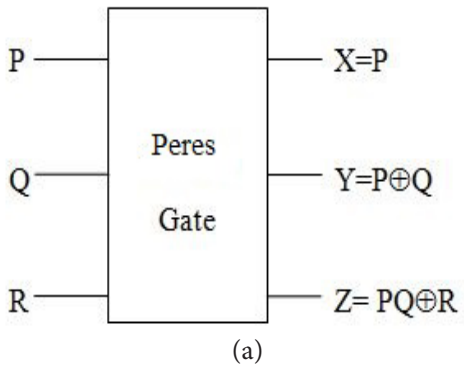


Figure 4: **(a)** Toffoli gate **(b)** Schematic using SOA-MZI switch[6].

So it is observed that MZI switch count came out to be 3, therefore its optical cost is 3. Number of beam combiner (BC) used is 1 and number of beam splitters (BS) used are 4. Optical delay of this gate is 2Δ as the last two MZI switches work in parallel. This gate can also work as n and gate as shown in Figure 4(b). If the input C is given logic 1 value thus output comes out to be NOT (AB).

7. All Optical Peres Gate

Peres gate is also a 3x3 reversible gate whose input vector is I= (P, Q, R) and the corresponding output vector will be O= (X=P, Y=P⊕Q, Z=PQ⊕R). Design of 3x3 Peres gate using MZI switch is shown in Figure 5.



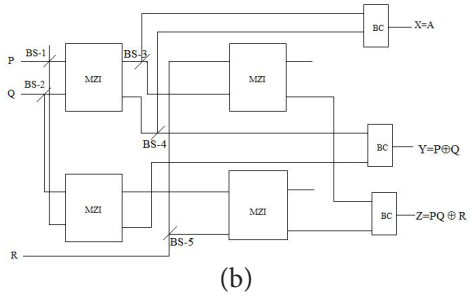


Figure 5: **(a)** Peres Gate **(b)** Schematic using SOA-MZI switch[7].

In this gate MZI switch count comes out to be 4, therefore its optical cost is 4. Number of beam combiners (BC) used are 3 and number of beam splitters (BS) used are 5. Optical delay of this gate is 2Δ as the last two pairs of MZI switches work in parallel.

8. Proposed All-Optical New Gate

Various new gates have been designed and implemented as shown in[15,16] and circuits built by them have advantages in terms of cost parameters. Therefore an attempt is made to design and implement such gate which further improves the cost of circuits. This section briefly describes the structure of new gate using SOA-MZI switch. Figure 6 has shown 3x3 new all-optical reversible gate and truth table of this gate is given in Table 1 and is verified by taking all

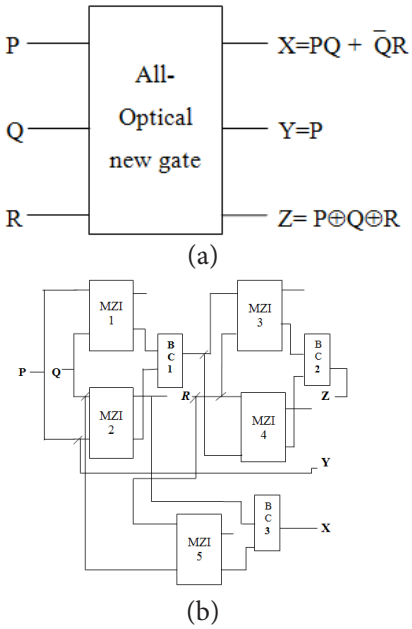


Figure 6: **(a)** All-Optical new gate **(b)** Schematic using SOA-MZI switch.

Table 1. Truth Table of New Gate

Inputs			Outputs		
P	Q	R	X	Y	Z
0	0	0	0	0	0
0	0	1	1	0	1
0	1	0	0	0	1
0	1	1	0	0	0
1	0	0	0	1	1
1	0	1	1	1	0
1	1	0	1	1	0
1	1	1	1	1	1

combination of inputs. If input vector is I= (P, Q, R) then the corresponding output vector will be O= (X=PQ +$\overline{Q}$R, Y=P, Z= P⊕Q⊕R).

This gate consists of 5 MZI switches which are as follows:

- Four MZI switches to implement P⊕Q⊕R thus optical cost for this implementation will be 4.
- One MZI switch to implement X=PQ + $\overline{Q}$R.

Therefore total optical cost of the circuit is 5 and optical delay is 2Δ as first three MZI switches works in parallel and next pair works in parallel so as a whole result will be obtained in 2 stages.

9. Functional Operation

Let us now discuss that how this gate operates in detail. The logic value 0 and 1 represent the absence and presence of light respectively.

- When we give no light at the input i.e. P=Q=R=0, then output shows no light i.e. X=Y=Z=0. This verifies first column of the truth Table 1.
- When both P and Q are given no light i.e. P=Q=0 and R=1 then incoming signal MZI-1 and MZI-2 will receive no light thus no light will emerge from upper and lower channels of both these switches. Due to this BC-1 will combine no light and as a result incoming signal of MZI-3 will be 0 and control signal of MZI-4 will be 0 so there will be light at lower channel of MZI-4 and thus it will be reflected at output Z through BC-2. Lower channel of MZI-5 will receive light therefore X will also be equal to 1. So second column of truth table 1 is verified.
- When no light is given at P and R i.e. P=R=0 and Q=1 then incoming signals at MZI-1, MZI-4, MZI-5 will be 0 and control signal of MZI-2, MZI-3 will be 0 therefore light will be present at lower channel of MZI-3. Thus Z=1, X=0 which satisfies the third column of Table 1.
- When light is given both at Q and R i.e. Q=R=l and P=0 then MZI-1 will receive no light but lower channel of MZI-2 will receive light therefore light will be present at incoming and control of MZI-3 thus lower channel of MZI-3 will receive no light. Similarly lower channel of MZI-4 will receive no light thus output Z=0, X=0 which satisfies fourth column of Table 1.
- When both B and C are given no light i.e. Q=R=0 and P=1 then incoming signal of MZI-2, MZI-4 and MZI-5 will be 0 and control signal of MZI-1 and MZI-3 will be 0, therefore lower channel of MZI-3 will receive light and thus Z=1. Also lower channel of MZI-5 will receive no light therefore X=Y=0 and this condition satisfies the column 5 of Table 1.
- When both P and R are given light i.e. P=R=1 and Q=0 then lower channel of MZI-3 will receive no light because its incoming signal is also 1, therefore Z=0. Lower channel of MZI-5 will receive light because R=0 and Q=1 therefore X=1 and Y=0 thus satisfying Column 6 of Table 1.
- When both P and Q are given light i.e. P=Q=1 and R=0 then incoming signal of MZI-3 and MZI-5 will be 0 thus Z=0, X=1 respectively which satisfies column 7 of Table 1.
- When all the inputs are given light i.e. P=Q=R=1 then lower channel of MZI-3 and MZI-5 will receive no light but lower channel of MZI-4 will receive light, therefore Z=1,X=1,Y=1 and this condition satisfies column 8 of Table 1.

10. New Gate as Universal Logic

This new all-optical new gate can also be used as universal logic gate and various operations are as shown below.

- **AND Gate**
  For AND gate realization we keep R=0 thus we get requisite output at port X i.e. X=P.Q as shown in Figure 7.
- **OR Gate**
  For OR gate realization we keep first input to be 1 thus we get requisite output at port X i.e. X=P+Q as shown in Figure 8.
- **XOR Gate**
  For XOR gate realization we keep first input to be 0 thus we get requisite output at port Z i.e. Z=P⊕Q as shown in Figure 9.

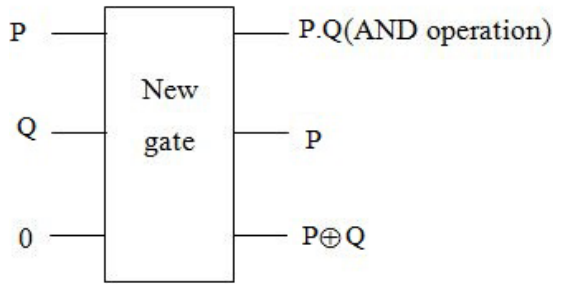


Figure 7. AND Operation.

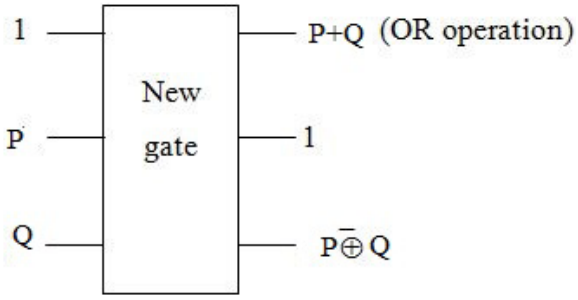


Figure 8. OR Operation.

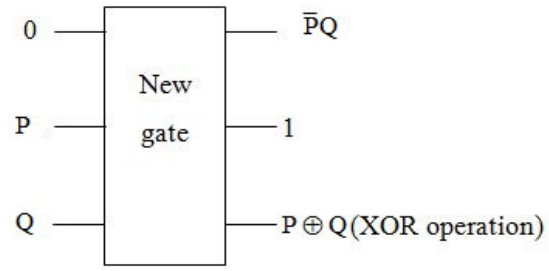


Figure 9. XOR Operation.

- **XNOR Gate**
  For XNOR gate realization we keep first input to be 1 thus we get requisite output at port Z i.e. Z=A⊕B as shown in Figure 10.
- **NOT Gate**
  For NOT gate realization we keep P=0, R=1 thus we get requisite output at port X and Z i.e. X=Z=$\overline{Q}$ as shown in Figure 11.
- **NAND Gate**
  For NAND gate realization we keep R=0 and then we give the output of this gate to NOT gate as shown in Figure 12. We get requisite output at port X and Z i.e. X=Z=NOT (PQ).
- **NOR Gate**
  For NOR gate realization we keep first input to be 1 and then connect NOT gate as shown in Figure 13. We get requisite output at port X=Z i.e. X=Z=NOT (P+Q).

11. Simulation Setup

The simulation of this new gate as shown in Figure 14 was performed using VPI PHOTONICS, a simulation based tool for optical communication systems. The orange block visible is MZI switch which is created as a galaxy before and is used as a module in this new gate implementation. Incoming and control signals are given as clock streams of type PRBS (pseudo random binary sequence) and their

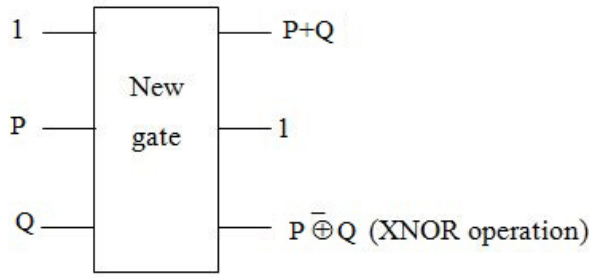


Figure 10. XNOR Operation.

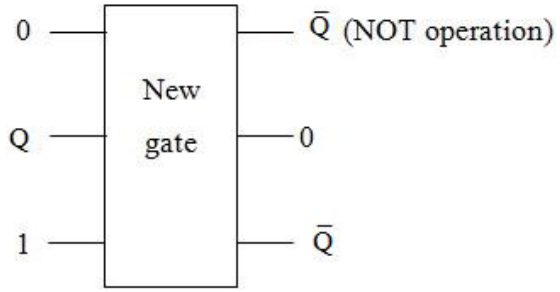


Figure 11. NOT Operation.

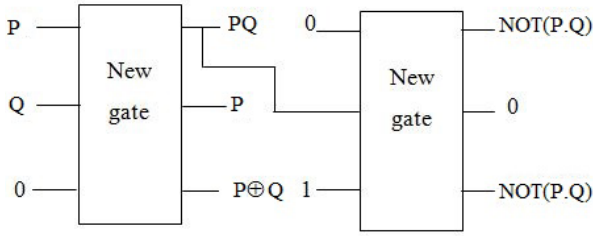


Figure 12. NAND Operation.

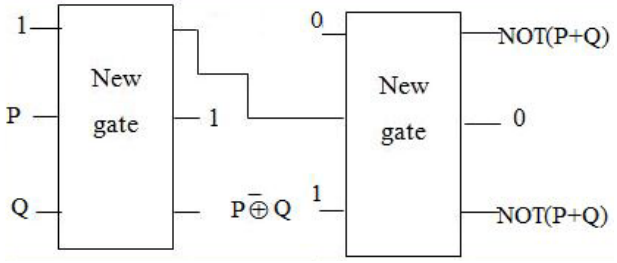


Figure 13. NOR Operation.

laser power levels are set to 20μW and 100μW respectively. Other parameters that are taken into account are shown in Table 2. Signal analyzers are connected at all the three inputs and outputs to record the corresponding waveforms.

This gate is unique in nature as all digital circuits can be designed using this gate. Half adder can be designed by simply putting R=0 and half subtractor can be designed by putting P=0. Output X acts as the output of a multiplexer by considering Q as a select line and P and R as the inputs. Multiplexer designed by this gate is improved in terms of optical cost and delay as compared to initial designs which were reported in[17] in[18-20]. Also various standard Boolean expressions can also be implemented using this gate with improved cost. Thus efficient designs of digital circuits can be implemented in future.

12. Results and Discussions

XOR operation is basically odd number of 1's detector i.e. the output goes high when odd number of 1's is detected.

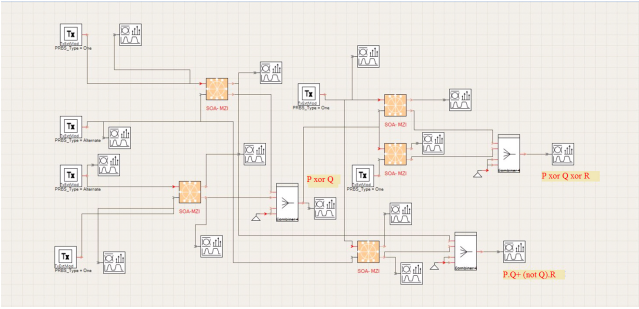


Figure 14. Schematic of New Gate in VPI Photonics.

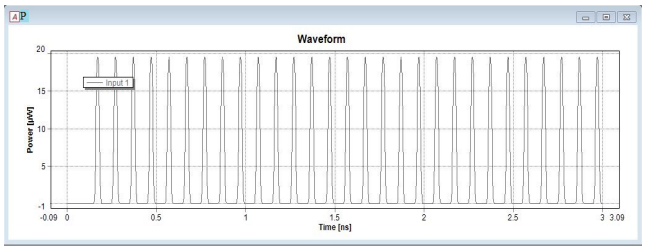
Table 2. List of Parameters

PARAMETER	VALUE
Bit Rate	10Gbps
Power of Incoming Signal	20μW
Power of Control Signal	100μW
Sample Mode Bandwidth	1280e9/2 Hz
Sample Mode Center Frequency	193.1e12 Hz
Time Window	30/10e9 s
Length of SOA	700e-6 m
Current density	480A/m^2
Active region width of SOA	2.5e-6 m
Active region Thickness	200e-9 m
Group Index	3.7
Confinement Factor	0.6

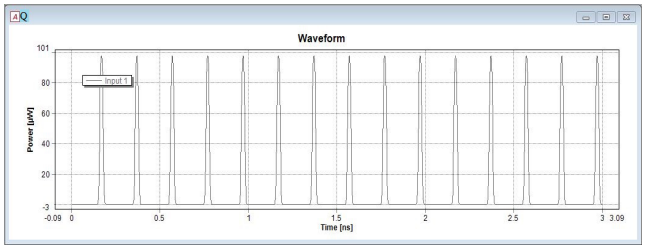
So this verifies our output wave form for the input bit sequence given as (P=11111….1, Q=101010…..10, R=111111…1). Output power levels in mill watts (mW) are observed due to semiconductor optical amplifiers which amplify the input signals. Input laser power should was taken in microwatts as it was observed that when power levels were increased to mill watts, the output was more and more distorted and it was difficult to distinguish between logic 0 pulse and logic 1 pulse. Thus input power was taken in the order of micro watts to observe distortionless and precise output. Input and output waveforms recorded in VPI analyzers are shown in Figure 15(a), (b), (c), (d), (e) and (f).

13. Conclusion

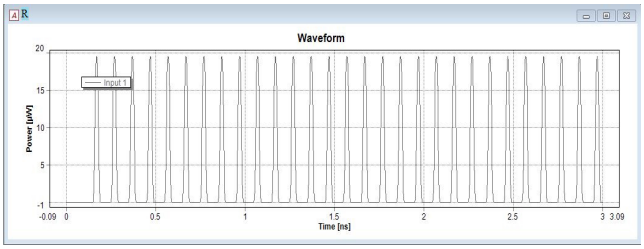
An All-Optical new gate has been successfully designed and implemented using SOA based Mach-Zehnder Interferometer switch architecture which has a fast response. Simulations are done using VPI PHOTONICS tool. Also the unique feature of this gate is that it's universal in nature and has many applications in the field of all-optical digital



(a)



(b)



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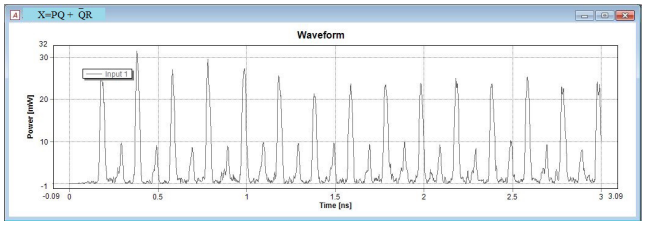

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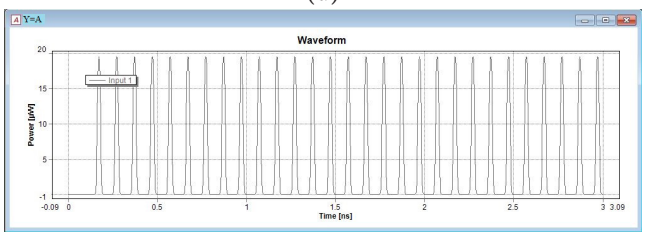

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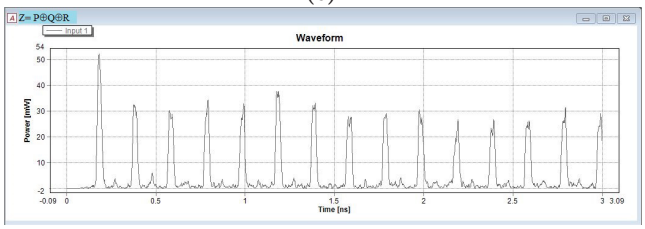

(f)

Figure 15: **(a)** Signal P **(b)** Signal Q **(c)** Signal R **(d)** Output waveform for X **(e)** Output waveform for Y **(f)** Output waveform for Z.

circuits. This gate works distortionless at bit rate of 10Gbps but if we increase the bit rate more than 40Gbps, the eye diagram is less opened i.e. we get distorted output. Future work will concentrate on increasing the bit rates for distortionless outputs. The input waveforms provided and the corresponding output waveforms obtained verify functionality of our new gate. Also realization of various standard Boolean expressions will be done and all-optical reversible circuits with improved optical cost and delay.

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