

Performance Analysis of Single-Wall Carbon Nanotubes and Copper as VLSI Interconnect

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Abstract

The work in this paper analyses the performance of Single Wall Carbon Nanotube (SWCNT) bundles as VLSI interconnect. Using equivalent RLC circuit models described in this paper, comprehensive analysis of delay and power is done at 22nm technology node for both SWCNT bundle and copper. Results show that SWCNT bundle has smaller value of resistance due to longer mean free path and lesser delay than copper. Therefore, SWCNT bundle is a promising alternative to copper as VLSI interconnect for advanced technology nodes.

Keywords: Carbon Nanotubes, Electromigration, Grain Boundary Scattering, Nanotechnology

1. Introduction

An Interconnect material helps in providing electrical connection between different nodes of the electrical circuit. Copper (Cu) was widely used as interconnect material due to its good conductivity and high current density¹. However, due to advancement in VLSI technology, several problems like surface roughness, grain boundary scattering, and increase in propagation delay, power dissipation and electro migration came into scene^{10,11}. Carbon nanotubes (CNT) has several micrometre long electron mean free path as compared to copper which has a few tens of nm mean free path³.

SWCNTs are hollow cylinders formed by only one thin wall of graphene with diameters ranging from 1-2nm¹. These can be either metallic or semiconducting. Metallic SWCNTs are used as interconnect material because of good thermal and mechanical stability. Isolated CNT gives high resistance, so to overcome this problem CNT bundles are used which consists of large number of isolated CNTs in parallel². Therefore, considerable reduction in resistance is achieved. This paper takes into account the effects of size on the electrical performance of Cu and SWCNT interconnects. The effect of size has been

studied and reported in this paper. For technology 22nm and below, Cu interconnects experience electromigration problems which increase its propagation delay as compared to SWCNTs. The rest of this paper is organised as follows: Section II and Section III introduces the electrical equivalent model of copper and SWCNT bundle as an interconnect material and the equations of their impedance parameters respectively. On the basis of impedance parameters Section IV shows the delay and power analysis and comparison of SWCNT bundle and copper at 22nm technology. Finally it is concluded that SWCNT bundle shows better performance than its counterpart and can be successfully used as interconnect for advanced technologies.

2. Copper as an Interconnect

Copper became the preferred interconnect material, especially for submicron and deep submicron high density and high performance chips. Copper has been evaluated as an interconnect material due to its high electrical conductivity and relatively high melting temperature around 1,357K¹³. The equivalent RLC circuit model of copper is shown in Figure 1.

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a. Resistance of Copper as an Interconnect

The resistance of Copper Interconnect is given by equation(2) as-

$$R_{Cu} = \rho(T) \left(\frac{l}{w \cdot t} \right) \quad (2)$$

Where, ‘ $\rho(T)$ ’ is the temperature dependent resistivity of copper, ‘ l ’ is the interconnect length, ‘ w ’ is the width and ‘ t ’ is thickness of the wire as given in Table 1.

b. Capacitance of Copper as an Interconnect

The capacitance of copper as an interconnect material is given by the Ground Capacitance⁶ due to area and fringing flux associated with underlying plane as shown in Figure 2. below-

$$C_{lg} = \epsilon \left[\frac{w}{h} + 2.22 \left(\frac{s}{s + 0.70h} \right)^{1.19} + 1.17 \left(\frac{s}{s + 1.51h} \right)^{0.76} \left(\frac{t}{t + 4.53h} \right)^{0.12} \right] \quad (3)$$

Where, C_g is ground capacitance per unit length. In above equation(3), ‘ s ’ is the separation between copper wires and is taken equal to the width and ‘ h ’ is the height of the

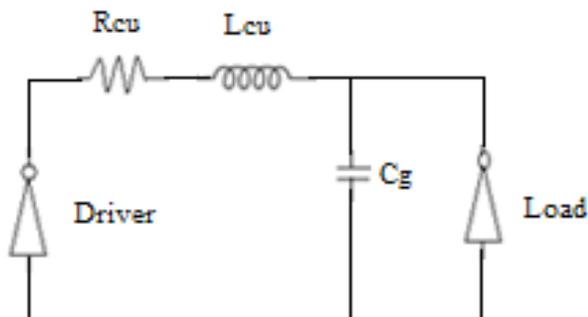


Figure 1. Equivalent RLC Circuit Model of Copper Interconnect.

Table 1. Simulation Parameters¹

Technology	32nm	22nm
Vdd	0.9v	0.7v
Length(l)	500um	500um
Width(w)	48nm	32nm
Thickness(t)	144nm	96nm
A/R (Global)	3	3
Separation between wires(s)	48nm	32nm
Height(h) ILD Thickness	110.4nm	76.8nm
$\rho_0(\mu\Omega.cm)$ (Copper)	3.52	4.2
ϵ Relative	2.25	2.05

wire. ‘ ϵ ’ is the relative permittivity of copper wire and its value depends upon technology.

c. Inductance of Copper as an Interconnect

The Inductance of Copper wire⁶ as an interconnect is given by equation(4) as-

$$L_{Cu} = \frac{\mu_0 l}{2\pi} \left[\ln \left(\frac{2l}{w+t} \right) + \frac{1}{2} + 0.22 \left(\frac{w+t}{l} \right) \right] \quad (4)$$

Where, ‘ μ_0 ’ is absolute permeability and its value is $4\pi \cdot 10^{-7}$ H/m.

3. SWCNT as an Interconnect

Carbon nanotubes are the strongest and stiffest materials discovered in terms of tensile and thermal strength. Basically, there are two types of CNTs- Single walled CNT (SWCNT) and Multiwall CNT (MWCNT). CNTs containing one thin wall of graphene sheet are SWCNTs having diameter in the range 1-2nm. Some CNTs which contains many concentric SWCNT like graphene tubes. These are termed MWCNT. Among these, SWCNT have been the choice because of its lower resistivity resulting from longer mean free path as an interconnect material¹.

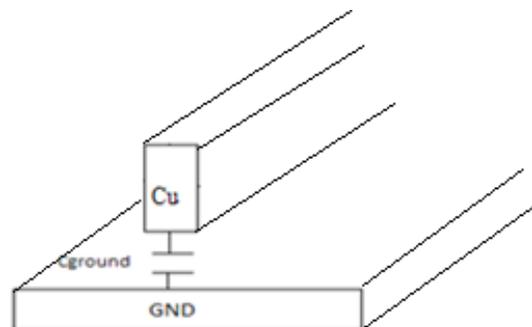


Figure 2. Cross section depicting Copper wires.

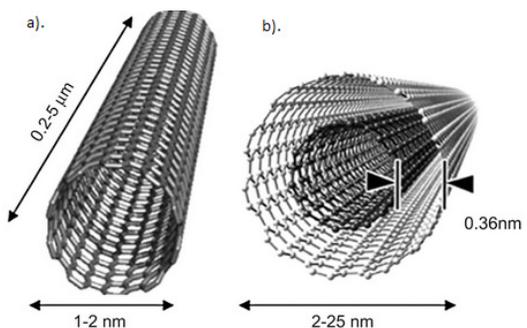


Figure 3. a).Single wall CNT (SWCNT),b). Multi wall CNT (MWCNT).

3.1 Impedance Parameters for SWCNT Bundle Interconnect

SWCNT-bundle interconnect comprises of identical metallic single-walled carbon nanotubes packed hexagonally. Each CNT surrounds six immediate neighbours; as shown in Figure 4. their centre's uniformly separated by a distance 'x'. The best performance is achieved with densely packed structure having 'x'=d' (CNT diameter)².

The expression(7) gives the total number of CNTs 'n_{CNT}' in the bundle, where 'n_h' is the number of "rows" in the interconnect bundle and 'n_w' is the number of "columns" in the bundle[2]-

$$n_w = \frac{(w - d)}{x}; \tag{5}$$

$$n_h = \frac{(h - d)}{\frac{\sqrt{3}}{2}x} + 1; \tag{6}$$

$$n_{CNT} = n_w n_h - \frac{n_h}{2}, \text{ if } n_h \text{ is even} = n_w n_h - \frac{n_h - 1}{2}, \text{ if } n_h \text{ is odd} \tag{7}$$

Where, 'h' is the thickness, 'w' is the width of the SWCNT bundle and generally, height is generally thrice the width for all technologies. The electrical equivalent RLC Circuit Model of the SWCNT bundle Interconnect is shown in Figure 5. below-

a. Resistance of a SWCNT-bundle

With N conducting channels in parallel, the resistance of SWCNT is h/Ne^2T^{12} , where 'h' is Planks constant,

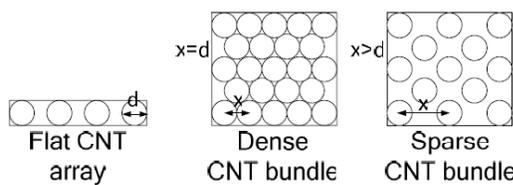


Figure 4. SWCNT Bundle as Interconnect².

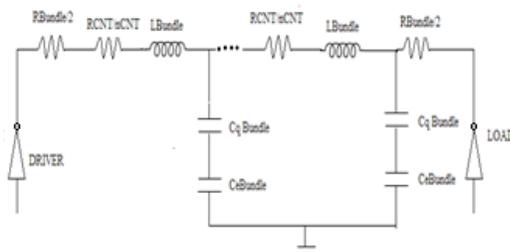


Figure 5. Equivalent RLC circuit model for an SWCNT Bundle Interconnect⁸.

'e' is electron charge and 'T' is electron transmission coefficient. There are 4 parallel conducting channel in SWCNT (N=4). Assuming perfect contacts (T=1), the resistance of an SWCNT is $h/4e^2$. In the equivalent circuit, this resistance (R_f) is equally divided between the contacts at the two ends of the nanotube given as-

$$R_f = \frac{h}{4e^2} \tag{8}$$

If the tube length (L) is larger than mean free path then electron scattering gives rise to an additional resistance⁵. This resistance increases with increase in SWCNT length and is expressed as-

$$R_{CNT} = \left(\frac{h}{4e^2}\right) \frac{L}{L_0} \tag{9}$$

The contact imperfection also leads to a very large value of resistance. SWCNT resistance of the order of 6-100 kΩ has been reported.

b. Capacitance of a SWCNT-bundle

The effective capacitance (C_{Bundle}) is the series combination of quantum capacitance of bundle which accounts for the quantum electrostatic energy stored in the nanotube when it carries current and electrostatic capacitance of SWCNT bundle due to charge stored by SWCNT ground plane system¹ and is given as-

$$C_{Bundle} = ((C_1(EBundle) + C_1(QBundle)) / (C_1(EBundle) + C_1(QBundle))) \tag{10}$$

Where, the values of C_{Ebundle} and C_{Qbundle} are given by equations (17) and (18) respectively and 'v_f' is the Fermi velocity of electron and its value is 8×10^5 m/sec.

$$C_{EBundle} = 2((2\pi \epsilon) \ln(s/d) + \text{floor}(((w - d - 2)/s)) ((2\pi \epsilon) \ln((s + w)/d))) + \frac{3(n_h - 2)(2\pi \epsilon)}{5 \ln(\frac{s}{d})} \tag{11}$$

$$C_{QBundle} = ((2e^2)/(\hbar v_f)) n_{CNT} \tag{12}$$

c. Inductance of a SWCNT-bundle

The inductance of a SWCNT bundle² is due to the parallel combination of the inductances corresponding to each CNT present in SWCNT bundle, and is given by equation (19) as-

$$L_{Bundle} = \frac{L_M + L_K}{n_{CNT}} \tag{13}$$

In above equation(20), total Magnetic energy resulting from the current flowing in the wire gives Magnetic Inductance (L_M) and is expressed as-

$$L_k M = \mu_0 / 2 \ln(y/d) \tag{14}$$

Where, 'y' is taken equal to 'h'. The Kinetic Inductance (L_k) comes from kinetic energy stored in each conducting channel of the CNT.

$$L_k = \frac{h}{2e^2 v_f} \tag{15}$$

4. Results and Discussions

The impedance parameters of copper and SWCNT bundle Interconnect are calculated from equations (1-15). Using the values obtained from these equations, resistance, capacitance and inductance are plotted at semi global and global length at 22nm technology node for both Copper and SWCNT as shown in Figure 6-8.

It is very much evident from the results that the value of resistance and inductance is higher for copper than

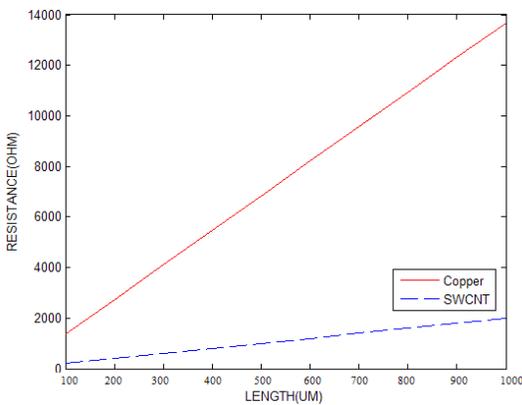


Figure 6. Comparison of Resistance between SWCNT and Copper at 22nm Technology.

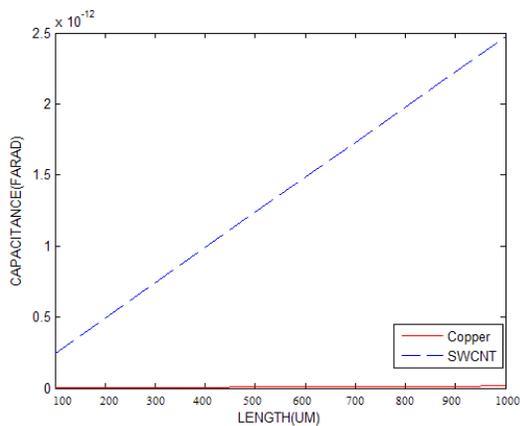


Figure 7. Comparison of Capacitance between SWCNT and Copper at 22nm Technology.

SWCNT at global length. This is due to shorter mean free path of electrons in case of copper as a result they undergo successive collisions at scaled technology lengths.

However, the value of capacitance is more for SWCNT than copper and it contributes to more Power dissipation in this case. Further RLC delay and Power analysis is done using Tanner Tool and the simulated results are shown in Figure 9-10.

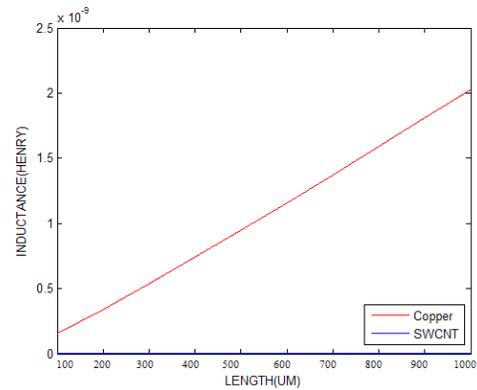


Figure 8. Comparison of Inductance between SWCNT and Copper at 22nm Technology.

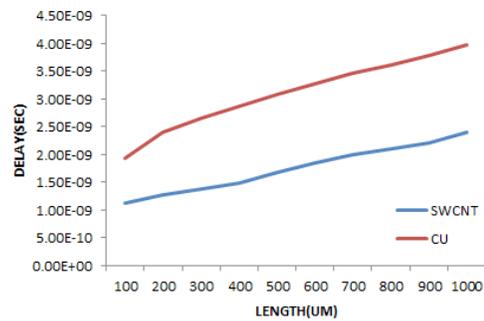


Figure 9. Delay Analysis between SWCNT and Copper at 22nm Technology.

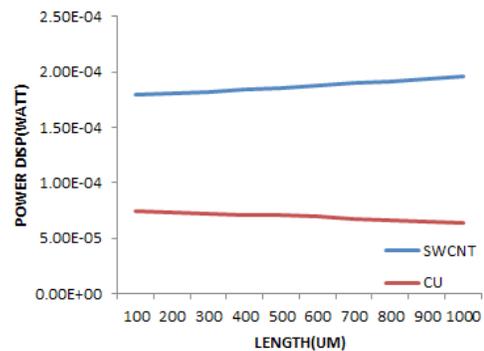


Figure 10. Power Analysis between SWCNT and Copper at 22nm Technology.

Figure 9-10 shows simulation results for delay and power comparison of copper and SWCNT at 22nm technology node. Fig.9 depicts that SWCNT exhibits lesser delay than copper at all length varying from 100um to 1000um. Thus, SWCNT is advantageous in terms of speed capability than copper.

Figure 10 presents that SWCNT undergo more power dissipation than copper due to its larger value of capacitance. However, this capacitance can be reduced to smaller value by varying other nanotube parameters like its diameter. By using large diameter SWCNT tube, its capacitance can be reduced to a smaller value. Thus, SWCNT proves to be a better material for interconnect applications in VLSI circuits at nanoscale technologies.

5. Conclusion

The comparison between copper and SWCNT as VLSI Interconnects has been studied extensively and it is found that the densely packed CNT bundle interconnects show significant improvement in performance as compared to copper interconnects, in spite of imperfect metal-nanotube contacts. The values of resistance and capacitance offered by SWCNT bundle interconnects can further affect performance parameters like delay and power dissipation. The Copper Interconnect offers a large value of resistance as compared to CNT bundle interconnects. Although the capacitance offered by SWCNT bundle is more than copper interconnect leading to more power dissipation but it can be optimized by choosing an appropriate diameter of the CNT tubes in bundle. Inductances can be ignored in the performance analysis because the resistive impedances are very much higher than the inductive impedances at any length of interconnects. Therefore, SWCNT provides an appropriate alternative to Copper Interconnects

6. References

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