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A Study of Traditional and Surrounding Gate MOSFET using TCAD Simulations

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Abstract

In this paper, Traditional and surrounding gate MOSFET are simulated using TCAD Silvaco and report the effect of multigate transistor. As the channel length of transistors is scaling down, a traditional MOSFET suffers from short channel effects and degrade the device performance. The different parameter such as threshold voltage, area, subthreshold slope, channel length modulation and leakage current are extracted for traditional and surrounding gate MOSFET. The parameters obtained from surrounding gate MOSFET is compared with a traditional MOSFET of the same dimension. The Results show that better performance was obtained for surrounding gate MOSFET. Its current drive capability is more as compared to traditional MOSFET .However, benefits of achieving superior performance with surrounding gate MOSFET reduces in terms of poor RF performance. Hence, this paper concludes that surrounding gate MOSFET have huge potential to be a promising contender to the traditional MOSFETs for making of future generation low-power high speed devices which could minimize the occupied area.

Keywords: Channel Length Modulation, Leakage Current, Subthreshold Slope, Surrounding Gate MOSFET, Threshold Voltage,

1. Introduction

The today's VLSI fulfils the demand of devices with higher speed, higher packing density, low power dissipation and energy efficient. Several short channel effect such as sub threshold swing, velocity saturation, threshold voltage roll-off (short-channel effect), hot electron effect, increase in leakage current and Drain Induced Barrier Lowering (DIBL) and Gate Induced Drain Lowering (GIDL).So it is important to take the device approaches in other ways to minimize not only the channel length of the device but also the channel width for the planar transistor to achieve higher packing density. Surrounding Gate Transistor (SGT) is a non planer device in which the channel is in the vertical direction. It is a device, whose gate electrode surrounds the silicon pillar. It reduces the area for the transistors. It increases packing density up to 50% to the surrounding gate MOSFET[1-3].

This paper is partitioned into five parts: Part-I covered the introduction of SGT, Part-II introduce devices structures of SGMOSFET and Traditional MOSFET, The analysis of electrical characteristics with the help of output drain and transfer characteristics of SGMOSFET and traditional MOSFET are described in Part-III. Part-IV includes the results and Part-V covered the conclusion and future work.

2. Device Structure

Surrounding Gate (SG) MOSFET is a device in which gate is surrounded from all the sides so increases the current driving capability. Fig 1 & Fig 2 shows the device structure of the SG MOSFET and the traditional MOSFET.

The source and drain doping concentration is about $1X10^{18}$ cm^{-3} and channel doping concentration is about $1X10^{16}$ cm^{-3}, channel length is 240 nm and with a oxide thickness of 20 nm for SG MOSFET and the traditional MOSFET.

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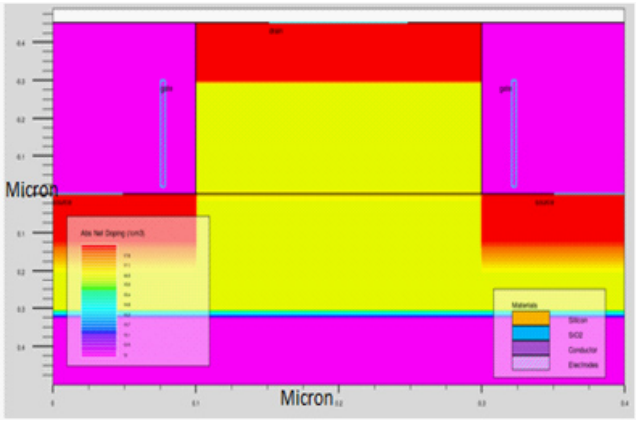

Figure 1. Device Structure of Surrounded Gate MOSFET.

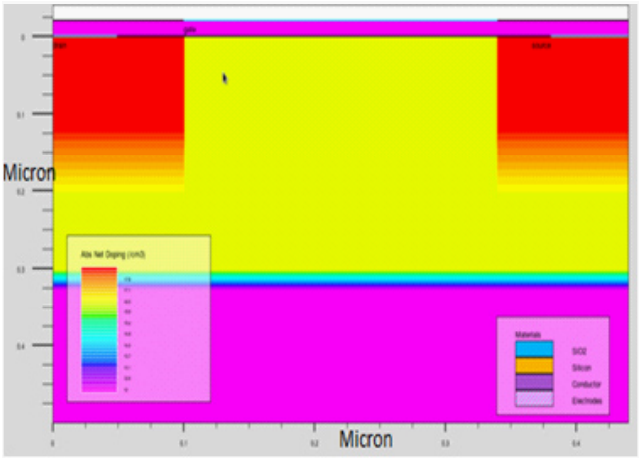

Figure 2. Device Structure of Traditional MOSFET.

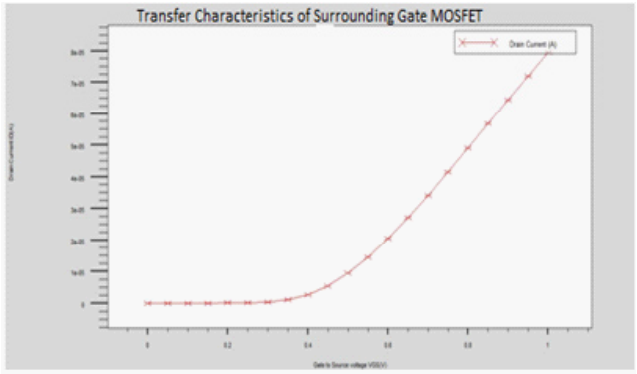

Figure 3. Transfer Characteristics of Surrounded Gate MOSFET.

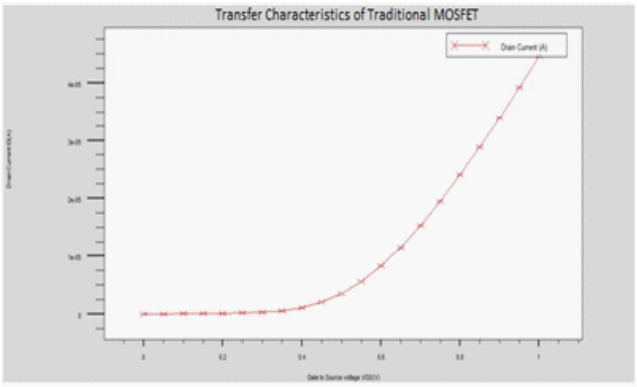

Figure 4. Transfer Characteristics of Traditional MOSFET.

3. Analysis of Electrical Characteristics

3.1 Transfer Characteristics

Fig 3 & Fig 4 shows the transfer characteristics of the SG MOSFET and the traditional MOSFET.

The SGMOSFET has a larger current driving capacity than the traditional MOSFET as demonstrates from transfer characteristics. This is mainly due to the channel is surrounded by the gate from all sides in SGMOSFET and presence of multigate in SGMOSFET. The SGMOSFET required smaller on voltage instead of the traditional MOSFET. It means that the Gate electrode has a higher control over the conducting channel in a SGMOSFET. The device performance ratio i.e. *Ion* / *Ioff* of the SGMOSFET is more as compared to traditional MOSFET[13,14]. It means leakage current is also very small in SGMOSFET and it reduces the power dissipation[4-7]. As shown in the Fig 3 & 4 that SGMOSFET has a smaller sub-threshold swing (SS) than a traditional MOSFET.

3.2 Output Characteristics

Fig 5 & Fig 6 shows the output drain characteristics of the SGMOSFET and for the traditional MOSFET are plotted with the help of TCAD silvaco[8].

The output drain characteristics are plotted between drain current and drain voltage at some constant value of the gate voltage. The output drain characteristics are very much similar in nature as that of a traditional MOSFET. The output drain characteristics revels that, the current driving capacity of SGMOSFET is larger than the traditional MOSFET. The SGMOSFET on resistance (Ron) is small in the linear region instead of a traditional MOSFET[9-11,14].

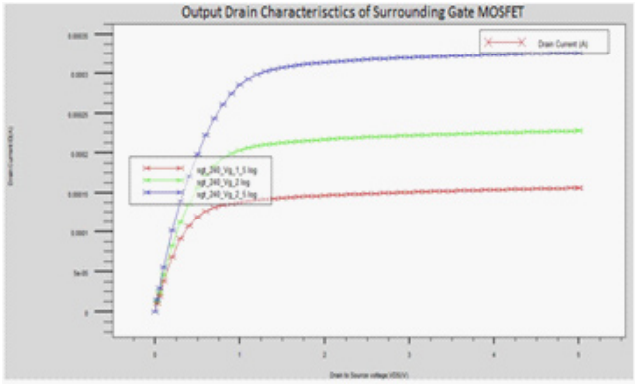

Figure 5. Output Drain Characteristics of SG MOSFET.

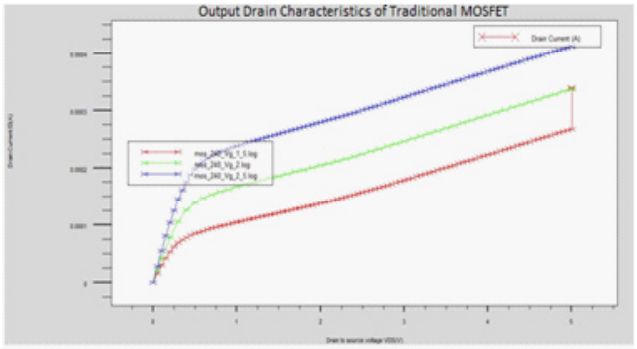

Figure 6. Output Drain Characteristics of Traditional MOSFET.

4. Results

1. Area covered by SGMOSFET =width (W), since the channel is in the vertical direction.

   Area covered by MOSFET =L*W = 240nm*W m^2

   So area on wafer can be saved using SGMOSFET, while having the same current driving capability.

2. Reduced channel length modulation

$$I_{DS1}/I_{DS2} = (1+\lambda V_{DS1})/ (1+\lambda V_{DS2})$$

The output drain characteristics of the SGMOSFET is shown by red line and the output drain characteristics of the traditional MOSFET is shown by green line as depicted in fig. 7.

As the channel length modulation (CLM) is diminished in SGT, which make it best for analog circuit design[16].

The Transfer characteristics of the SGMOSFET are shown by red line and the Transfer characteristics of the traditional MOSFET is shown by green line as depicted in Fig. 8.

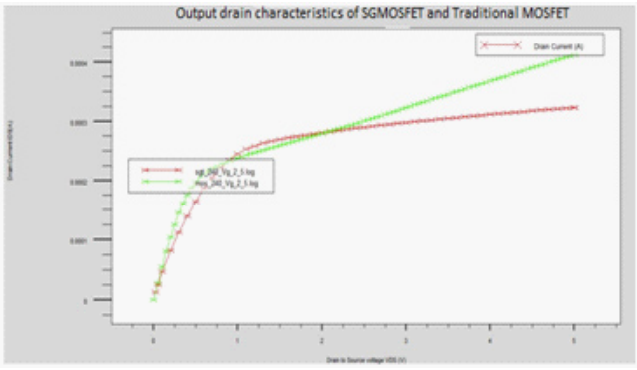

Figure 7. Output drain characteristics of SGMOSFET and Traditional MOSFET for V_{GS}=2.5V.

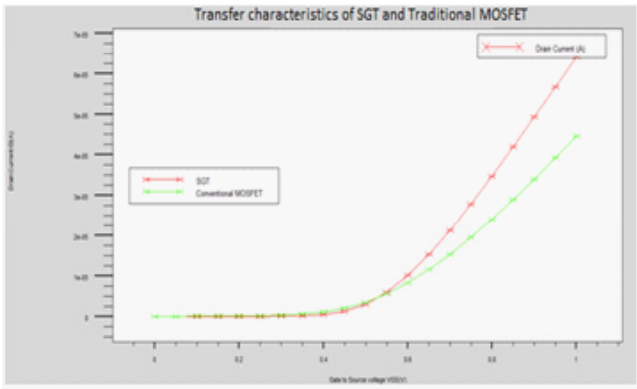

Figure 8. Transfer characteristics of SGT and Traditional MOSFET for V_{DS}=1V.

Table 1. Parameters to find Channel length modulation

Device	V_{DS}(V)	I_{DS}(A)	λ(V^{-1})
Surrounded Gate MOSFET	3	0.000295	0.06
	4	0.00031	
Traditional MOSFET	3	0.000325	0.28
	4	0.000375	

3. Threshold Voltage

Threshold voltage of Traditional MOSFET (V_T) = 0.45 V

Threshold voltage of SGT (V_T) = 0.4 V

The SGMOSFET having a smaller V_T than the traditional MOSFET as given above. It means that the

Gate electrode has a more control over the channel in a SGMOSFET[15,17].

4.Improved Sub-threshold slope and reduced leakage

Fig. 9 shows the plot between Log(I_D) Vs V_{GS} for SGMOSFET and Traditional MOSFET for V_{DS}=1V.

- Sub threshold slope (SS) = $\frac{dV_{GS}}{d(\log I_D)}$ mV/decade

  It is voltage required to change in one decade of current, so SS is less required for fast switching operation[14,15].

  SS of SGT= 90 mV/decade

  SS of planer MOSFET= 160 mV/decade

  Therefore it can be concluded that SGT is faster than traditional MOSFET.
- Leakage current[17]

  From the plot it can be seen that I_D when V_{GS}=0 V at V_{DS}=1 V is the order of 10^{-12} for SGT and 10^{-8} for MOSFET.

  So SGMOSFET required smaller area, low threshold voltage, reduced channel length modulation, Leakage current and Improved Sub-threshold slope[12].

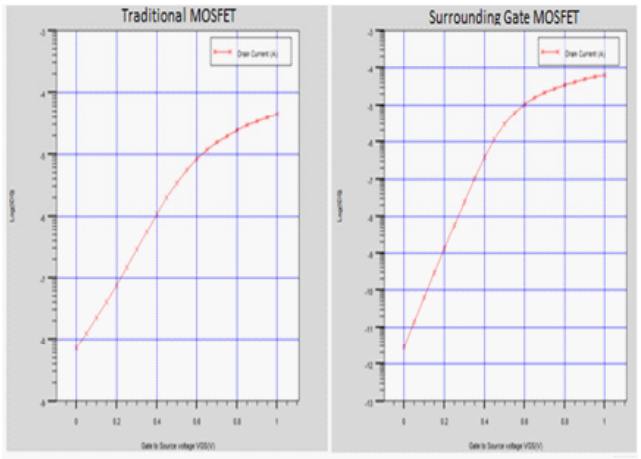

Figure 9. Log(I_D) Vs V_{GS} plot of SGMOSFET and Traditional MOSFET for V_{DS}=1V (a)MOSFET (b) SGMOSFET.

Table 2. Parameters to find Sub-threshold slope

Device	V_{GS}(V)	Log(I_{DS})	Sub-threshold slope
Surrounded Gate MOSFET	0.26	8	90 mV/decade
	0.35	7	
Traditional MOSFET	0.225	7	160 mV/decade
	0.385	6	

5. Conclusion and Future Work

SGMOSFET has been adopted for making future devices, which could minimize the occupied area and also reduce the power dissipation. As the channel is surrounded by the gate so we get better electrical control over the MOSFET which is visible through the small sub-threshold slope compare to traditional MOSFETs. There is only manufacturing complexity which increases the cost of fabrication leads another technology like FinFET which fabrication is more similar to planer process.

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