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A Novel Stochastic ADC Topology with Wide Input Range

Fadi Nessir Zghoul[1*], Suat U. Ay[2], Ismail Cevik[3], Ahmad A. Ababnah[1]
Saher A. Albatran[1] and Abdallah Y. Alma'aitah[1]

[1]Department of Electrical Engineering, Jordan University of Science and Technology, Irbid – 22110, Jordan; FRNessirZghoul@just.edu.jo, aaababnah@just.edu.jo, saalbatran@just.edu.jo, ayalmaaitah@just.edu.jo
[2]Department of Electrical and Computer Engineering, University of Idaho Moscow, ID – 83844, USA; suatay@uidaho.edu
[3]Electronics and Communication Engineering Department, Istanbul Technical University, Istanbul – 34469, Turkey ceviki@itu.edu.tr

Abstract

This paper describes a novel stochastic ADC topology with a wide input range. Stochastic ADC utilizes the randomness of process mismatch in comparators. Offset voltage which is Gaussian distributed represents the input range of stochastic ADCs. Stochastic ADCs have several limitations and drawbacks, such as limited input signal range and large number of required comparators to achieve high resolution. Some methods have been proposed to increase the input signal range at the expense of resolution. In this work we propose a novel stochastic ADC circuitry capable of increasing the input signal range without any sacrifice in the resolution. This new topology cycles the signal until it is within the offset voltage standard deviation. The Stochastic ADC is simulated using MATLAB SIMULINK.

Keywords: ADC, Data Converters, Stochastic ADC, Wide Input Range

1. Introduction

Recently, CMOS technology has been diminishing in size, and the demand for fast, accurate and less power consumption circuits has been growing rapidly. Hence, the role of digital circuits in performing discrete time domain calculations is becoming more important every day, while the challenges facing circuit designers in building Analog to Digital Converters (ADCs) to translate our analog world to digital are growing accordingly. ADCs can suffer errors related to their dynamic aspect or errors related to the DC characteristics[1].

A new method has been reported that makes use of the comparator offset voltage to increase the accuracy of the ADC[2]. Random offset voltage is Gaussian distributed around the switching voltage of the comparator. By designing a large number of comparators and connecting them in parallel, the number of comparators that evaluate "high" against the input signal will follow the Cumulative Density Function (CDF). The CDF can be used as a transfer function. By using this method the reference ladder has been eliminated in the flash ADC[2]. In 2010 the same authors[3] used two sets of comparators with two different voltage references that are 2.14σV apart. σ is the standard variation of the comparator offset. Two sets where used in order to linearize the transfer function[3]. The disadvantage is the extra number of comparators used, which is almost 48%[3]. A PDF folding method was also used by the same authors to reduce the extra number of comparators[4]. In[5] the authors used standard CMOS digital gate comparators in order to implement and synthesize the entire ADC using Verilog code.

There has been some work done on investigating the performance of stochastic ADCs by circuit simulation[6]. In 2014 Skyler and others[7] were able to fully digitally synthesize a stochastic flash ADC which was an extension to their previous work[5]. They also propose a method to correct the nonlinearity by linearizing the CDF of the Gaussian offset distribution using a piecewise inverse Gaussian CDF function[5]. Stochastic ADCs have been analysed and performance trade-offs for these ADCS have been studied where the authors focus on the relationship between the number of comparators and the effective resolution of the stochastic ADC[8].

* *Author for correspondence*

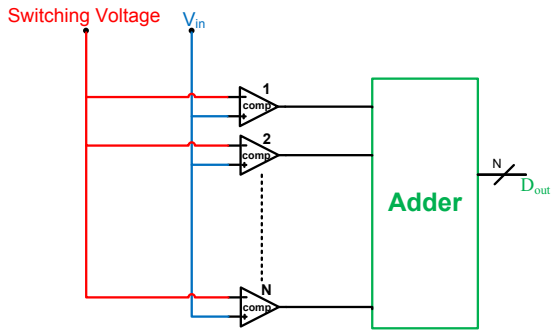
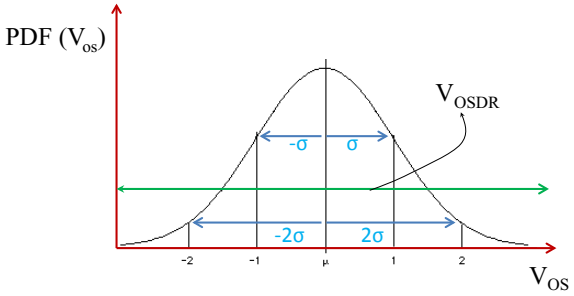
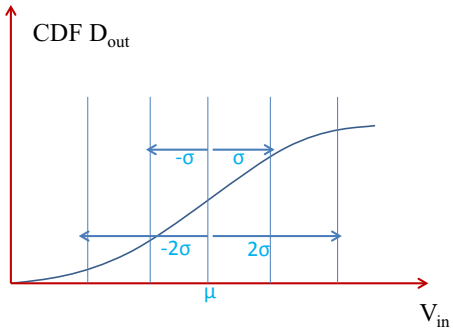


Figure 1. Traditional stochastic ADC.



(a)



(b)

Figure 2. (a) Probability density function of comparator offset voltage (b) Output of the adder as a function of Vin.

Using stochastic ADC improves the resolution with the expense of limited input signal range. The input signal has to be within the range of three sigma of the distribution mean for the offset voltage. To address this issue work has been done to connect the reference of the comparators to a noise generator and use a structure similar to SAR ADC where the noise generator changes the standard deviation of the noise in the second iteration depending on input signal voltage calculated from the first iteration[9]. In the last iteration the noise signal is disconnected and only the Gaussian distribution of the comparators offset voltage is used[9]. This method has several drawbacks, such as the complexity of the circuit used to generate the different noise signals with different standard deviation for each iteration. The noise circuitry has a string of inverters and resistors, where resistors require large area. The difficulty is in not exactly knowing the standard noise deviation introduces error into the system. The DAC used in this topology can also be a source of non- ideality if it can't achieve the same resolution of the ADC itself.

More work has been done to increase the input signal range[10] the authors used eight banks of comparators with a different voltage reference for each bank. Such approach requires eight times the number of comparators to get the same resolution. An eight level voltage regulator is used to feed each bank of comparators with a different reference voltage. The value of these voltage levels is controlled and loaded by an off chip SPI interface, which is considered a drawback[10].

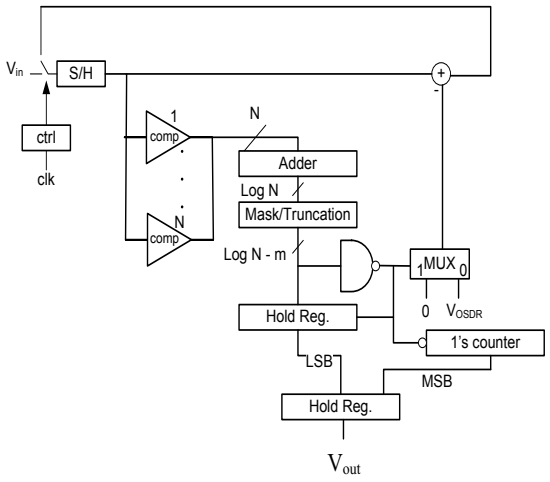


Figure 3. Block diagram of the proposed Wide input stochastic ADC WIS-ADC.

In this paper a new stochastic ADC topology is proposed that makes use of the offset voltage generated due mismatch in comparators. This new topology solves the problem of narrow input range for stochastic ADC without adding more comparator banks to the circuitry and without using off chip circuitry.

2. Offset Voltage

Mismatch between a pair of its transistors in a comparator will cause offset voltage. The output of the mismatched comparator will change status only when the difference between the two input voltages exceeds a minimum amount of voltage. This minimum amount of voltage is called input offset voltage

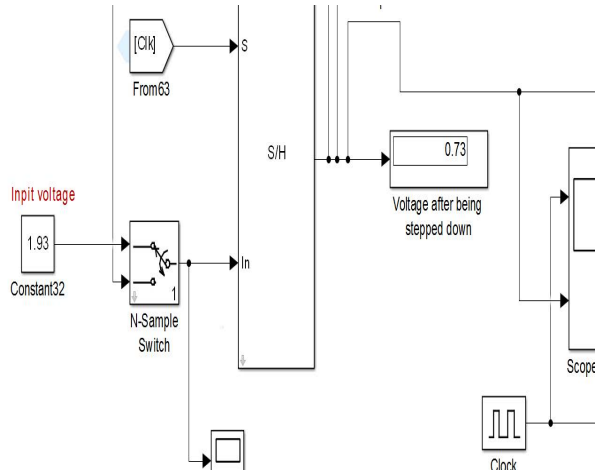


Figure 4. Display showing the input signal being stepped down from 1.93V to 0.73V.

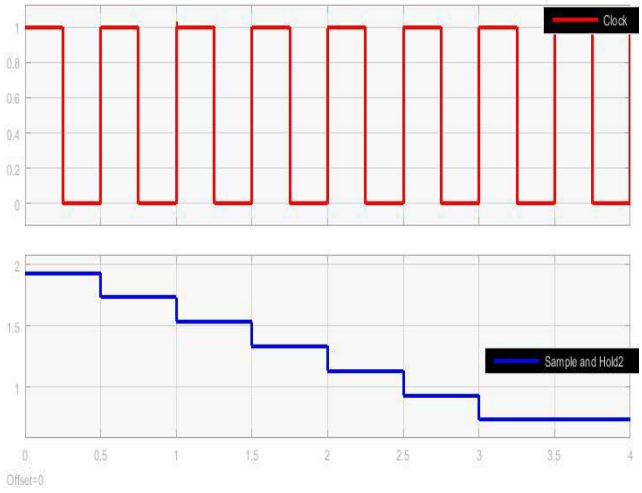
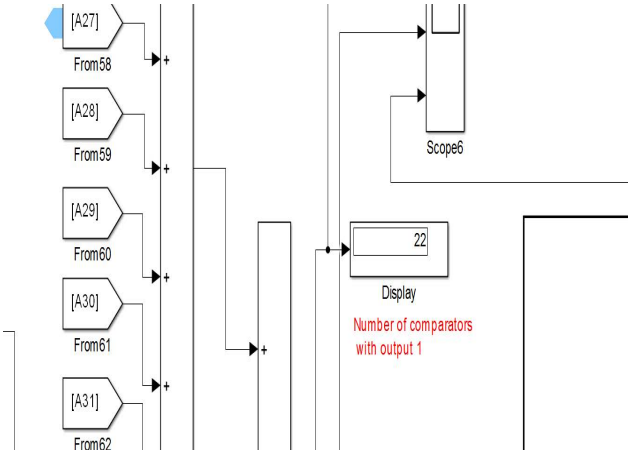


Figure 5. The scope showing the input signal being stepped down from 1.93V to 0.73V in blue, in steps of 0.2V with every clock shown in red.

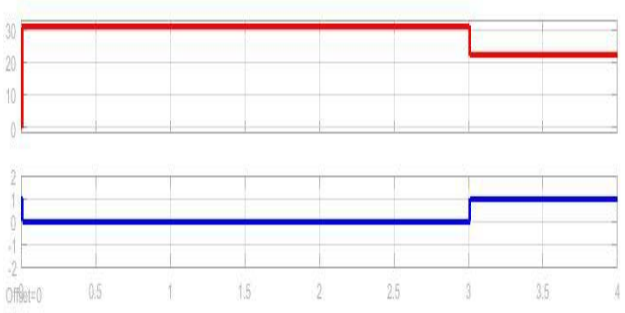
The comparator can compare two input signals and respond properly only when the difference between its two inputs is greater than the input offset voltage. Hence, the smaller the input offset voltage the more sensitive and precise the comparators will be[11]. Since the comparator is the heart of the ADC, the offset voltage error in the comparator affects the overall performance of the ADC. Increased offset error will increase the Differential Nonlinearity Error (DNL) and the Integral Nonlinearity Error (INL) depending on the architecture of the ADC.

3. Stochastic ADC

A stochastic ADC replaces one comparator with multi comparators all switching at the same voltage as seen in Figure 1. Ideally all these comparators with the same switching voltage should flip and change status at the same exact voltage. Due to offset voltage comparators switch status randomly, Gaussian distributed around the ideal switching voltage Figure 2(a). This offset voltage causes errors in traditional ADCs. On the other hand, offset errors can be put high is thirty-one for the first six cycles and it became 22 in the seventh cycle, shown in red. And it also can be seen how the output of the NAND gate was zero for the first six cycles and it became one in the seventh cycle, shown in blue, greatly minimized in stochastic ADCs. When the input voltage of the comparators is greater than the ideal switching voltage it is expected to have more comparators with output equal to one. The number of comparators equal to one will follow the CDF of the offset voltage Figure 2(b). Depending on the number of comparators equal to one compared to the total number of comparators the value of the input voltage can be known and converted to a digital value.



(a)



(b)

Figure 6. (a) Display showing number of comparators with output high (b) The number of compactors with output high shown in red. The output of the shown in blue.

4. Wide Input Stochastic ADC

One major problem in stochastic ADCs is the limited input range which is determined by the offset voltage statistical distribution range V_{OSDR} shown in Figure 2(a). As mentioned earlier, few methods were proposed to solve this problem but in all these methods the cost was high. In this paper we propose a new topology to solve this problem which is shown in Figure 3 and we will call it the Wide Input Stochastic Analog to Digital Converter (WIS-ADC).

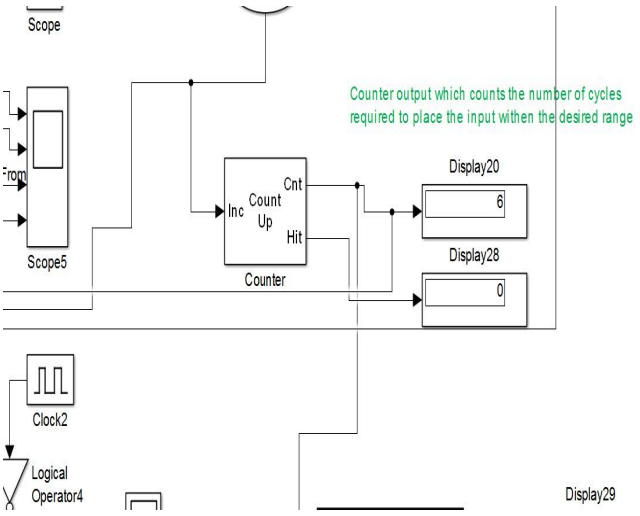


Figure 7. Display showing the output of the counter which is equal to 6.

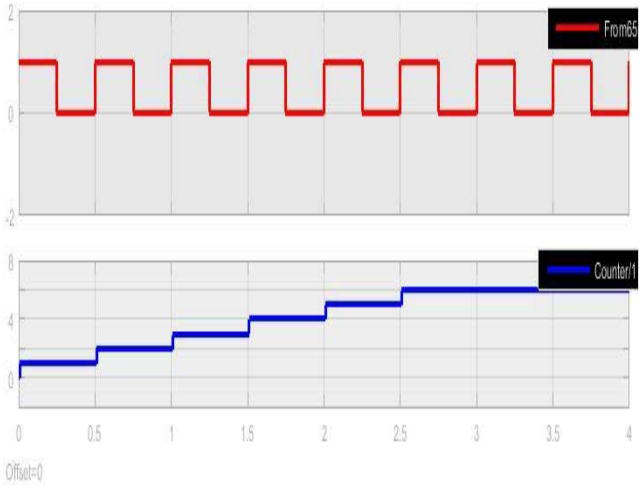


Figure 8. Scope showing the output of the counter which counts on the rising edge of the clock.

In the WIS-ADC, at the first clock, the switch connects the input signal to the sample and hold. If the signal is within V_{OSDR} the output of the comparators corresponds to the value of the input. The outputs of the comparator are added, the adder output bits will not be all "ones", since the input signal is within the V_{OSDR}. The Mask/Truncation block will cancel the first one or two LSB bits in order to linearize the CDF. The output of the NAND gate is going to be "1" since some of the NAND gate inputs are "0"s. The mux will pass the zero to the subtractor. The input signal will remain as it is since zero voltage is subtracted from it, and it will be stored in the sample and hold. At the second CLK signal, the switch will be connected to the S/H block in the feedback loop. It will be also connected to the S/H block in the feedback loop for the rest of the CLKs. The output of the Mask/Truncation block is stored in the first hold register which stores its input only when it is active high. The ones counter has three output bits since the number of cycles x = "8". These three output bits represent the three MSBs and they are stored in the second hold register at the last clock edge. The content of the first hold register is also stored in the second hold register at the last clock edge. These bits represent the LSBs.

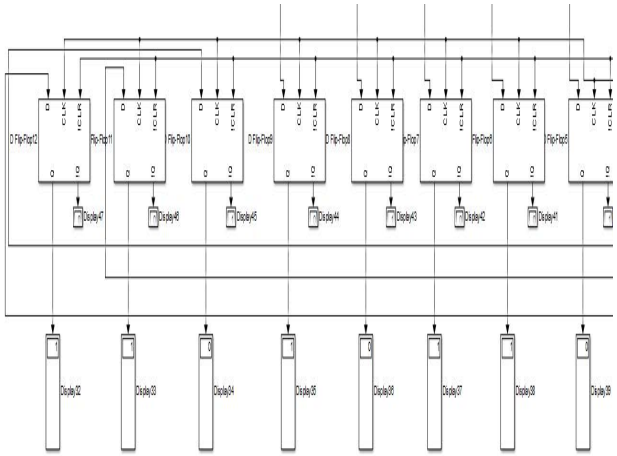


Figure 9. Eight displays showing the output of the 8-bit ADC which is 11010110 that corresponds to 1.93V.

On the other hand, If the input signal is out of range, all the adder output bits are equal to "1". In this case, the output of the NAND gate is "0". The MUX will pass the voltage V_{OSDR} which will be subtracted from the input signal and stored in the second S/H block. At the second clock it will be fed to the first S/H block. This process will keep repeating until the voltage in the first S/H is within the V_{OSDR} range. Each time the output of the NAND is zero the counter will count since its active low. If the voltage on the first S/H block is within the $ V_{OSDR} $ range after the forth clock, the output of the counter is "110" in the case of "x=8". And the first scenario is repeated for the rest of the clocks.

5. Simulation Results

The WIS-ADC behavioural response is simulated using MATLAB SIMULINK the real time delay of each block is not taken into account and the speed of the conversion does not match the real speed of the ADC built with CMOS transistors which will be developed in future work. Thirty-one comparators and eight cycles where used in this ADC, which results in an eight-bit ADC, five bits due to the thirty-one comparators and three bits due to the eight cycles. The threshold voltage for the comparators is chosen to be 0.7 volts and the offset voltage is almost ±0.1 volts, which means it is normally distributed between 0.6 and 0.8 volts. The input voltage range of the ADC is between 0.6 and 2.2 Volts. In order to increase the range of the ADC, the number of cycles can be increase since we have no control on the amount of the offset voltage.

The input voltage was chosen to be 1.93V, after 7 cycles it was stepped down to be 0.73V, 0.2V for each cycle as seen on the display shown in Figure 4. It can be also seen on the scope shown in Figure 5.

Twenty-two comparators have randomly given an output voltage "high" due to the voltage 0.73V the number of comparators is shown on the display in Figure 6(a).

In Figure 6(b), it can be seen how the number of compactors with output high is thirty-one for the first six cycles and it became 22 in the seventh cycle. And it also can be seen how the output of the NAND gate was zero for the first six cycles and it became one in the seventh cycle.

Since the circuit needs six cycles to step the input voltage in order to place it with the desired range the counter will count six times as seen on the display in Figure 7.

It can be also being shown on the scope in Figure 8; the counter counts on the rising edge.

Figure 9 shows the output of the ADC which is 11010110 that corresponds to 1.93V.

6. Conclusion

A new topology for a wide input voltage range stochastic ADC has been presented. A bank of comparators has been used eight times rather than using eight banks to design an eight-bit stochastic ADC. Thirty-one comparators and eight cycles where used in this ADC, which results in an eight-bit stochastic ADC, five bits due to the thirty-one comparators and three bits due to the eight cycles. The WIS-ADC behavior has been simulated using MATLAB SIMULINK and for future work the WIS-ADC will be designed using spice software.

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