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Multilevel Hybrid DSTATCOM Compensator for Distribution Network Load Compensation

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Abstract

Objective: The power utilized by distribution networks depends on power quality which is a function of harmonics, reactive four & power factor. The effect of harmonics was earlier reduced by passive filters. Such filters have distinct disadvantage of fixed ramp. **Statistical Analysis:** For overcoming this disadvantage, DISTATCOM components has been proposed. In this case, respective power consumption is cooperated and harmonic injection is minimized LCL based filter reduces DC link voltage rating required for component. **Finding:** The voltage profile is improved. Utilization voltage source inverter reduces the reactive power compensation. Active and reactive power are individually controlled. From the simulations results it is found that current reduction is up to 55.2% where as voltage reduction is up to 85.1%. **Application**: The proposed multilevel based VSI in the DSTSTCOM improves the overall performance to a remarkable extent. Optimization of the number of level can be taken up as an extension of this work.

Keywords: Distribution Static Compensator (DSTATCOM), Voltage Source Inverter (VSI), Passive Filter, Power Quality (PQ)

I. Introduction

Now a day's the power utilized by distribution loads going on increasing day by day. The performance of distribution loads purely depends on power quality (PQ) of supply given as an input. Here the main considering power quality issues are harmonics, reactive power and power factor. The harmonics effects winding insulation and machine temperature, increased reactive power consumption leads to increased losses and reduced performance and the power factor effects economical point of operation. The traditional passive filters can use for fixed range it was not used for wide range of operation. To overcome this disadvantage DSTATCOM was utilizing as a compensator. This will compensate reactive power consumption and reduces harmonic injection up to their range. Here LCL based DSTATCOM[1] is used as a compensator. The LCL filter will reduces stress on STATCOM[2]. The LCL components reduces DC link voltage rating required to compensate compared with same rating of DSTATCOM without LCL[3]. The DSTATCOM designed with voltage source inverter (VSI) type of topology. It will facilitate effective control on reactive power compared with other type of topologies. Generally in conventional manner two-level inverters are used, due to this some of the harmonics are generated to compensate this some passive filters are included. The passive filters required for two-level converter is high due to this losses are increases. To overcome this multilevel inverter was introduced in compensator. Here five-level diode clamped multilevel inverter was used for compensation due to this the filtering required for filter out harmonic component is less and it was used for high power ratings. The combination of multilevel inverter and passive filter overcome the disadvantages of conventional DSTATCOM. This hybrid compensator effectively improves power quality of the distribution system with less DC link voltage and reduced rating of power electronic devices. The DSTATCOM analyze percentage total harmonic distortion (THD) injected by non-linear loads and it can injected in negative direction. The LCL

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filters are tuned for selective harmonic elimination. The tuned filter is tuned to filter 5th order harmonic injected by load. This will reduces rating of DSTATCOM required for PQ improvement and it reduces stresses on power electronic devices used in VSI.

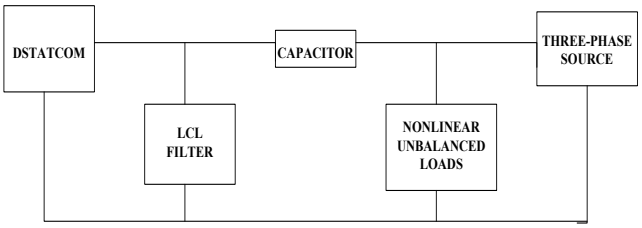


Figure 1. Proposed DSTATCOM topology for PQ improvement.

The utilization of LCL filter with multilevel VSI[4] DSTATCOM improves its range for high power applications with reduced ratings. This hybrid filters are economical and its performance is high compared to traditional two-level DSTATCOM.

2. Proposed DSTATCOM Topology

The proposed system consist of passive filter and one active filter, it has shown in Figure 1. The LCL filters places before the VSI. The LCL filter can reduces DC-link voltage and active filter rating. By using less rating power electronic devices, the compensation is performed to high level. The proposed VSI designed with multilevel convert topology. These systems are used for high power ratings, by using this topology the filtering requirement for compensating harmonics generated by active filter. The proposed system consists of one series capacitor, it is used for eliminate resonance condition caused by LCL filter. The proposed system connected at PCC to compensate reactive power consumption and to reduce harmonics induced in to source side by nonlinear loads. The five-level hybrid DSTATCOM[5] can improve system performance over two-level conventional DSTATCOM.

3. DSTATCOM Control

The main theme of the STATCOM controller[6] is to reduce the unbalance factor, harmonic reduction and reactive power compensation. This will fetch the harmonic content and particular order of the harmonic percentage from load current by sensing load current. This was injected at PCC in negative direction by these the harmonic content was reduced. It will keep the current in phase with voltage by sensing angle from grid voltage. The controlling operation can be performed by comparing measured values with reference and error will reduced using PI controllers. From these the references values are generated for pulse generation, based on this pulses are generated for VSI to compensate PQ issues.

The reference filter currents are generated from terminal voltage positive sequence component. The currents are defined as follow

$$i^{*}_{f2a} = i_{la} - i^{*}_{sa} = i_{la} - \frac{v^{+}_{ta1}}{\Delta^{+}_{1}}\left(P_{lavg} + P_{loss}\right)$$
$$i^{*}_{f2b} = i_{lb} - i^{*}_{sb} = i_{lb} - \frac{v^{+}_{tb1}}{\Delta^{+}_{1}}\left(P_{lavg} + P_{loss}\right)$$
$$i^{*}_{f2c} = i_{lc} - i^{*}_{sc} = i_{lc} - \frac{v^{+}_{tc1}}{\Delta^{+}_{1}}\left(P_{lavg} + P_{loss}\right) \quad (1)$$

Here v^{+}_{ta1}, v^{+}_{tb1}, and v^{+}_{tc1} are +ve sequence component of fundamental voltage. The average load power and power loss are calculate as:

$$P_{lavg} = \frac{1}{T}\int_{t_1-T}^{t_1}\left(v_{ta}i_{la} + v_{tb}i_{lb} + v_{tc}i_{lc}\right)dt \quad (2)$$

The VSI power loss calculations are done using equivalent circuit as shown in Figure 2 and 3.

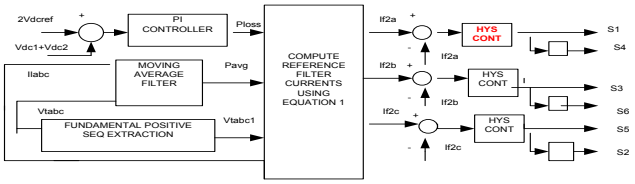


Figure 2. Controller block diagram.

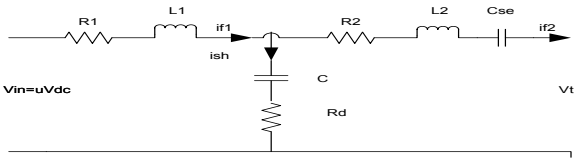


Figure 3. Single-phase circuit diagram of the passive filter.

The power loss was calculated from dc-link voltage shown in bellow equation.

$$P_{loss} = K_p e_{vdc} + K_i \int e_{vdc} dt \quad (3)$$

The measured value is compared with reference and then the error value is reduced by using PI controllers, the mitigated error was used as a reference to pulse generation.

4. DSTATCOM Parameter Design

The filter parameters are calculated based on system ratings. These are, the supply voltage is 230V, load power rating of 10KVA, the pulse generator switching frequency[7-12] of 10 kHz, 5A is the harmonic current and the dc link voltage of 520 V respectively. The reference DC-link voltage is used to supply the source to inverter to get required operation. 110V dc-link voltage taken as a reference to maintain healthy operation. The effective design/calculation of LCL filter parameters will considers cost, loss and resonance conditions. The filter current calculated as

$$L_1 \frac{di_{fi}}{dt} = -v_t - R_1 i_{fi} + V_{dcref} \tag{4}$$

Where R value is negligible, then the equation is rewritten as

$$L_1 = \frac{V_{dcref}}{(2h_a)(2f_{max})} = \frac{V_{dcref}}{4h_a f_{max}} \tag{5}$$

Here $2h_a$ is the allowable ripple content for maximum switching frequency. The series capacitor parameters are calculated for high switching frequencies. Then the system transfer function given by

$$\frac{I_{f1}(s)}{V_{inv}(s)} \frac{s^2 + 1/L_1 C}{sL_1\left(s^2 + \left((L_1 + L_2)/L_1 L_2 C\right)\right)} \tag{6}$$

$$\frac{I_{f2}(s)}{V_{inv}(s)} \frac{1/L_1 L_2 C}{s\left(s^2 + \left((L_1 + L_2)/L_1 L_2 C\right)\right)} \tag{7}$$

From (6), the resonance frequency will be

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{1+k}{kL_1 C}} \tag{8}$$

Where $k = L2/L1$. The capacitance at resonance is

$$X_{cres} = \frac{1}{2\pi f_{res} C} \tag{9}$$

The power losses in the damping resistor will be

$$P_{loss} = 3 * R_d * \sum_{h=1}^{n} I_{sh}^2 \tag{10}$$

Here h is the order of harmonic in current flowing in R_d, the current supplied by filter is

$$I_f^1 = \frac{V_{inv1} - V_{t1}}{R_f + j(X_{f12} - X_{se1})} \tag{11}$$

Where $R_f = R_1 + R_2$, $Xf_{12} = \omega_1(L_1 + L_2)$, $X_{se1} = \omega_1 C_{se1}$, the inverter voltage is

$$V_{inv1} = \frac{V_{dc}}{\sqrt{2}} \tag{12}$$

After simplification, (11) becomes

$$I_f^1 = \frac{(V_{inv1} - V_{t1})R_f - j(V_{inv1} - V_{t1})(X_{f12} - X_{sc1})}{R_f^2 + (X_{f12} - X_{sc1})^2} \tag{13}$$

By neglecting interfacing resistances due to its small value, the imaginary part magnitude of $I1f$ will be

$$I_m\left[I_f^1\right] = -\frac{V_{inv1} - V_{t1}}{X_{f12} - X_{se1}} \tag{14}$$

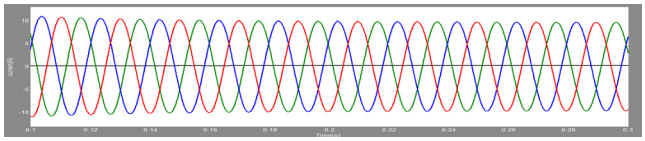
The maximum current drawn by the load is

$$I_{1max} = \frac{V_{t1}}{R_{1min} + X_{1min}} \tag{15}$$

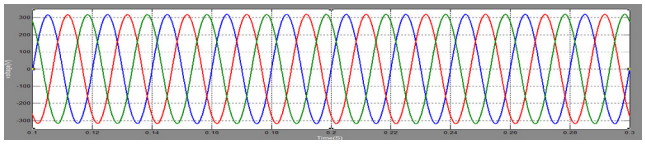
$$\frac{V_{t1} X_{lmin}}{Z_{lmin}^2} = \frac{V_{inv1} - V_{t1}}{X_{f12} - X_{sc1}} \tag{16}$$

$$I_{lmax}\sqrt{1 - pf_{lmin}^2} = \frac{V_{inv1} - V_{t1}}{X_{f12} - X_{sc1}} \tag{17}$$

$$X_{sc1} = X_{f12} - \frac{V_{inv1} - V_{t1}}{I_{lmax}\sqrt{1 - pf_{lmin}^2}} \tag{18}$$



(a)



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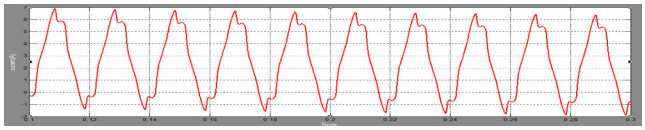

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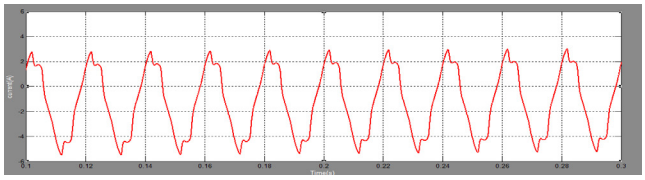

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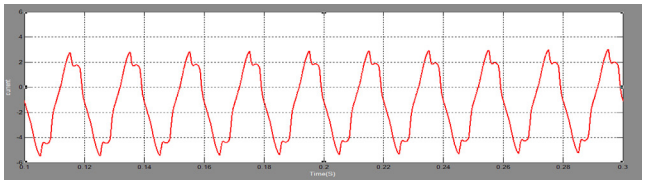

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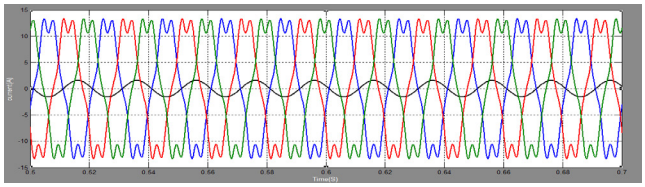
(f)



(g)

Figure 4. Simulation results for proposed system (a) Source Current, (b) pcc voltages (c),(d),(e) Filter Current (f) Voltage across dc-link(V_{dc1}+V_{dc2}) (g) Load currents.

Table 1. Simulation Parameters

System quantities	values
source voltage	230V rms line to neutral,50HZ
Feeder impedance	Z_s=1+j3.14Ω
Linear load	Z_{la}=30+j62.8,Z_{lb}=40+j78.5, Z_{lc}=50+j50.24
RC type nonlinear load	R_l=50Ω,C_l=1000μF
VSI parameters (traditional)	V_{dc}=520v,C_{dc}=3000μF, L_f=26mH
VSI parameter (LCL based)	V_{dcref}=520v,C_{dc}=3000μF, R_1=R_2=0.05Ω,C=10μF, (L_1,L_2=6.5,1)mH
Multilevel parameters (proposed)	V_{dcref}=110v,C_{dc}=3000μF,R_d=15Ω R_1=R_2=0.05Ω,(C,C_{se}=10,50)μF (L_1,L_2=1.5,0.6)mH
Five level diode clamped multilevel inverter	MOSFET resistance=0.1Ω Internal diode resistance=0.01Ω

5. Simulation Results

The proposed system can improve the performance of the system. Basically multilevel converters are used for high power ratings. The proposed system used for high power ratings as a compensator with reduced DTATCOM ratings. The power losses are reduced, the percentage THD injected by load in to source current is reduced to small value and cost of filtering required for compensate harmonic injected by DSTATCOM is less compared to conventional two level compensator. The parameters of proposed system as shown in Table-1. Are observed the variations in Figure 4.

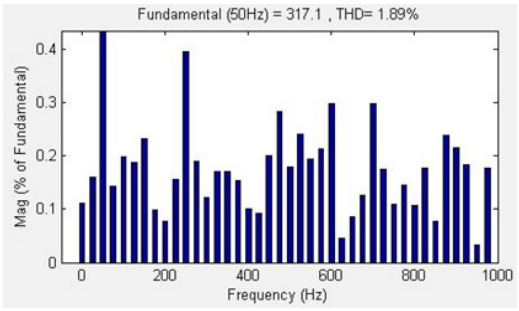


Figure 5. FFT analysis for PCC voltage in traditional method.

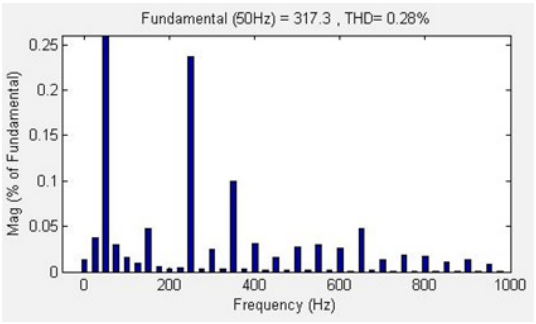


Figure 6. FFT analysis PCC voltage in proposed method.

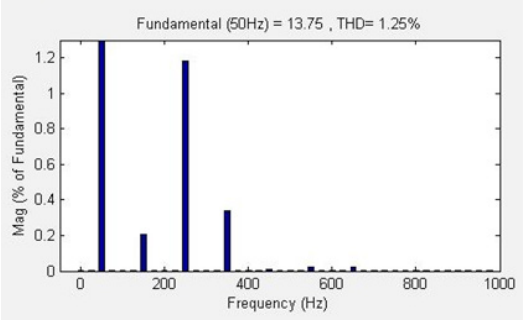


Figure 7. FFT analysis for source current in traditional method.

Table 2. Percentage THDs in source currents and pcc voltages

THD	Traditional method	Proposed method	reduced
current	1.25%	0.56%	55.2%
voltage	1.89%	0.28%	85.1%

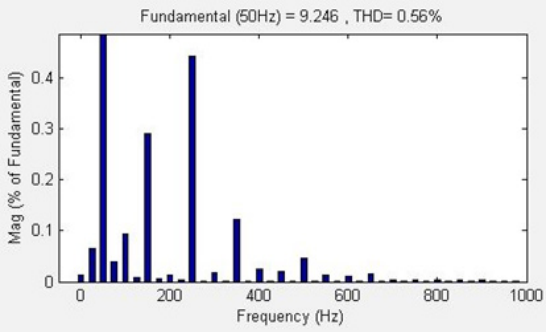


Figure 8. FFT analysis for source current in proposed method.

The proposed system performance is analyzed under non-linear load conditions. The combination of nonlinear and unbalanced loads in distribution system will injects harmonics. The proposed DSTSTCOM will injects this harmonics in negative direction to load harmonics. The results of the Figure 5,6,7,8 are significant about the FFT of difference variation in DSTSTCOM performance. The resultant of these to be reduces the harmonic percentage injection in to source side.

7. Conclusion

This paper proposes a multilevel inverter based hybrid DSTSTCOM topology to reduce cost of converter filters, to reduce rating of compensator to meet high power requirements, harmonic reduction and reactive power compensation. The hybrid system consists of passive filter and series capacitor. This combination and the variations are observed in Table 2 to reduce DC-link voltage requirement and mitigates stresses on power electronic devices in the converter. The proposed multilevel VSI used in high power applications due to its reduced losses. Due to these advantages the proposed DSTSTCOM improves system performance to a greater extent than conventional compensator.

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