

## REVIEW ARTICLE



# A comprehensive review of parallel concatenation of LDPC code techniques

S Chaitra<sup>1</sup>, V Rekha<sup>2\*</sup>, A M Harisha<sup>3</sup>, T A Madhu<sup>4</sup>, S Mallikarjunaswamy<sup>5</sup>,  
N Sharmila<sup>6</sup>, H N Mahendra<sup>5</sup>

<sup>1</sup> Dept of ECE, Vivartana Technologies, Bangalore, 560041, Karnataka, India

<sup>2</sup> Dept of CSE, SOET, Chirst (Deemed to be University), Bangalore, 560074, Karnataka, India

<sup>3</sup> Dept of ECE, Xolcano Technologies, Bangalore, 560040, Karnataka, India

<sup>4</sup> Dept of EEE, Sri Jayachamrajendra College of Engineering, Mysore, 570006, Karnataka, India

<sup>5</sup> Dept of ECE, JSS Academy of Technical Education, Bangalore, 560060, Karnataka, India

<sup>6</sup> Dept of EEE, RNS Institute of Technology, Bangalore, 560060, Karnataka, India



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\* **Corresponding author.**

[rekha.v@christuniversity.in](mailto:rekha.v@christuniversity.in)

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## Abstract

**Objective:** In the code theory, parallel concatenation of codes becomes more popular after the introduction of turbo codes. In recent years, the Low Density Parity Check (LDPC) code has found remarkable advancement and has seen them outshine turbo codes in terms of performance especially in the error floor and higher code rate. The main objective of this paper is to address the various techniques of a parallel concatenation of LDPC code in code theory.

**Method/Finding:** To reduce the complexity of encoding and decoding for longer codes various parallel concatenation of LDPC coding methods were introduced and the performance was compared with other work. **Novelty:** When a longer block length is used, the parallel LDPC decoder is suffered from the complexity of prohibitive implementation. To overcome this issue and to achieve the best performance for longer codes, the different methods for parallel concatenation of LDPC codes were introduced with reduced complexity. This will helps to break the long and complex LDPC code into less complex and smaller LDPC to distribute the decoding and encoding load. Also, this will provides scalability and scope for improving the performance of LDPC codes in practical delay-sensitive and energy-aware applications.

**Keywords:** Parallel concatenation; LowDensity ParityCheck (LDPC); turbo codes; Parallel Concatenated Gallager Codes (PCGC)

## 1 Introduction

The Low-density parity-check (LDPC) codes were first introduced by Robert Gallager in his research work in 1962<sup>(1-3)</sup>. This introduced code will fit in a class of linear block code. But due to implementation complexity, LDPC codes were not suitable for many applications. Later, in 1995 these codes are modified by D. MacKay and R. Neal after the discovery of turbo codes by Berrou in 1993. In their work, prove that LDPC codes gain good performance in code theory. After modified in LDPC codes, it provides relatively low decoding complexity and a high degree of parallelism, hence it becomes a more attractive solution for error correction of codes. However, encoding complexity

in LDPC codes increases with block length and for longer block length it will become relatively high. On the other hand, the decoder of fully parallel LDPC is suffering from the complexity in implementation of the longer block length. The insensitive application may limit the use of LDPC codes. Therefore, LDPC codes with the parallel concatenation of different methods were introduced for longer codes to get better performance. Also, parallel concatenation reduces the encoding complexity for long LDPC codes.

Code concatenation of binary irregular LDPC codes is studied before<sup>(3-5)</sup>. Original parallel concatenated LDPC codes, called Parallel Concatenated Gallager Codes (PCGCs), were proposed in<sup>(5)</sup> in which they showed how different component codes with different parameters affect the overall performance in a Gaussian Channel. They restricted their description of PCGC to rate 1/3 codes constructed by combining two rates 1/2 binary irregular LDPC codes without an interleaver.

The authors in<sup>(6)</sup> showed that the interleaver is not needed for their proposed code. Also, they predicted that the conclusions are easily extended to the case where three or more codes are used, as introduced in<sup>(7)</sup> in which a serial concatenated irregular LDPC codes, without interleaver, is introduced. In<sup>(8)</sup> a PCGC was modified to use an interleaver. The interleaver swaps the element positions of the code; i.e.it changes the weight distribution of the code. Thus, it helps increase the minimum distance of the code. Also, the authors in<sup>(9)</sup> showed that high performance could be obtained, while fewer requirements of iterations, with a serial concatenated of two binary irregular LDPC codes, with an interleaver. In<sup>(8)</sup> non-binary LDPC codes were applied in a serial concatenation scheme with an interleaver. The authors in<sup>(9)</sup> showed that the proposed code scheme outperforms a single nonbinary LDPC code. A serial concatenation of nonbinary LDPC codes is proposed in<sup>(9)</sup>. In this paper, we present the different methods of LDPC codes with parallel concatenation.

The rest of this paper is organized as follows: Overview about Parallel Concatenated Gallager Codes (PCGC) is presented in section II, followed by PCGC structured as presented in section III. PCGC with the sets of two source bits, is presented in section IV. Single encoder PCGC is presented in section VI. The modified PCGC is presented in section IV. PCGC with interleaver is presented in section VII. At last conclusion is presented in section VIII.

## 2 Conventional PCGC

The Parallel Concatenated Gallager Codes (PCGC) is the class of concatenated codes<sup>(4)(5)</sup>. It allows to concatenate the two LDPC encoders in parallel without using an interleaver between them. The PCGC conventional with concatenated codeword and encoder structure is shown in Figure 1. The idea behind the development of PCGCs was to include the principle of turbo-encoding in LDPC codes. In the long LDPC code, the complexity in decoding and encoding is divided into lower complexity steps of decoding and encoding. Also, at the same time maintain the flow of information between decoder components and reduces the information loss during the decoding steps. The component codes are selected based on the Mean Column Weight (MCW) of the code's parity-check matrix. MCW is the average column weight over all columns in the parity check matrix. It has been found that by choosing low MCW code as the first component code and high MCW code as the second component code, performance is improved. Figure 2 shows the effect of MCW on the extrinsic information in PCGC conventional encoder for the various signal-to-noise range.

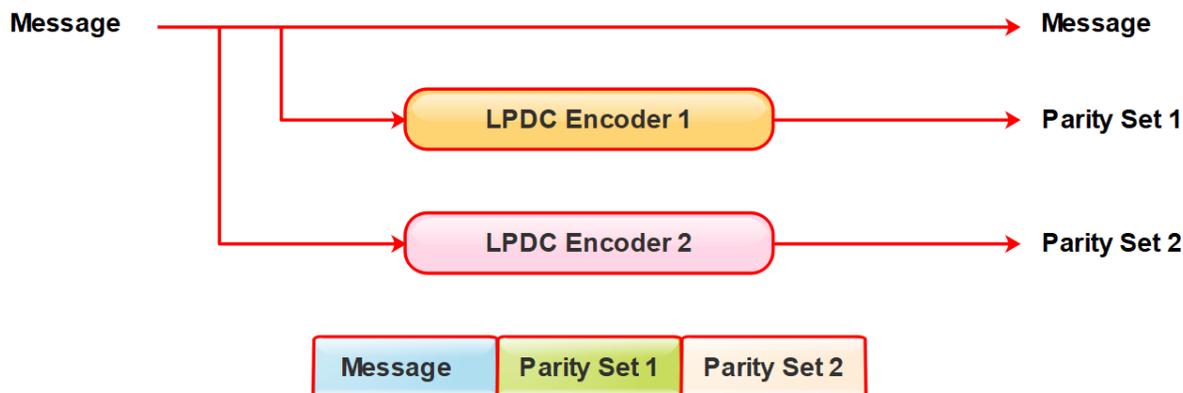


Fig 1. PCGC conventional encoder and structure of concatenated codeword

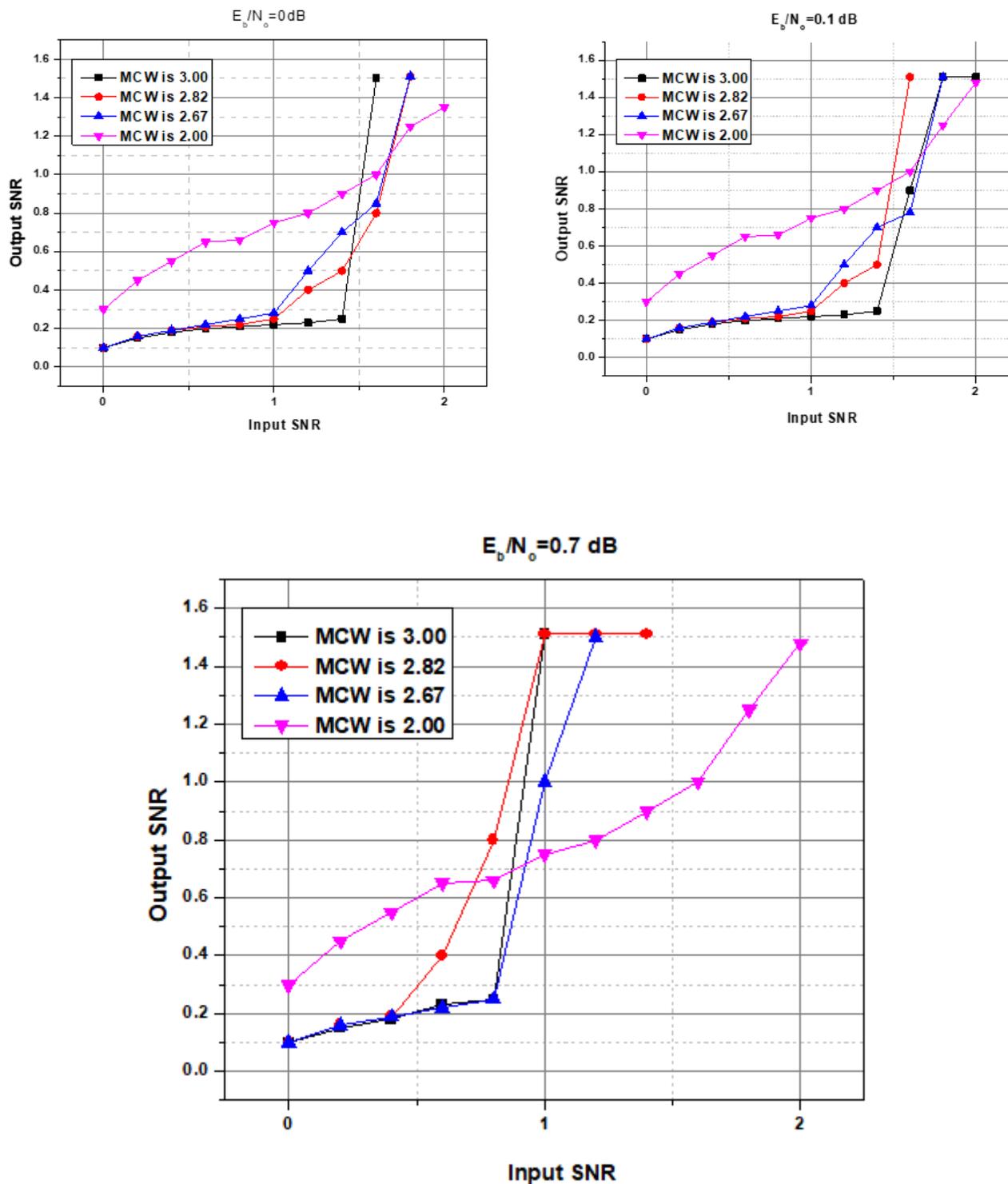


Fig 2. Effect of MCW on the extrinsic information SNR in PCGC conventional encoder

The PCGCs decoding procedure is very similar to the turbo code decoding and no interleave between decoder components. The Conventional PCGC decoder is shown in Figure 3. A posteriori probability is computed by each component of LPDC decoder during the process of decoding as per<sup>(6)</sup> using a modified sum-product algorithm<sup>(3)</sup>. LDPC codes decoding is

an iterative process and this process will exchange the information between the decoder components. The LPDC decoder component performs the algorithm of the sum-product in one complete cycle, which is referred to as local iteration. Any information passing between decoder components, the local iterations must be performed by decoder components, and this process called super iteration. The information exchange process between decoder components remains to continue till valid codeword converges by both decoders. In the latter case, the output from the second component decoder is declared as the best estimate of the transmitted sequence.

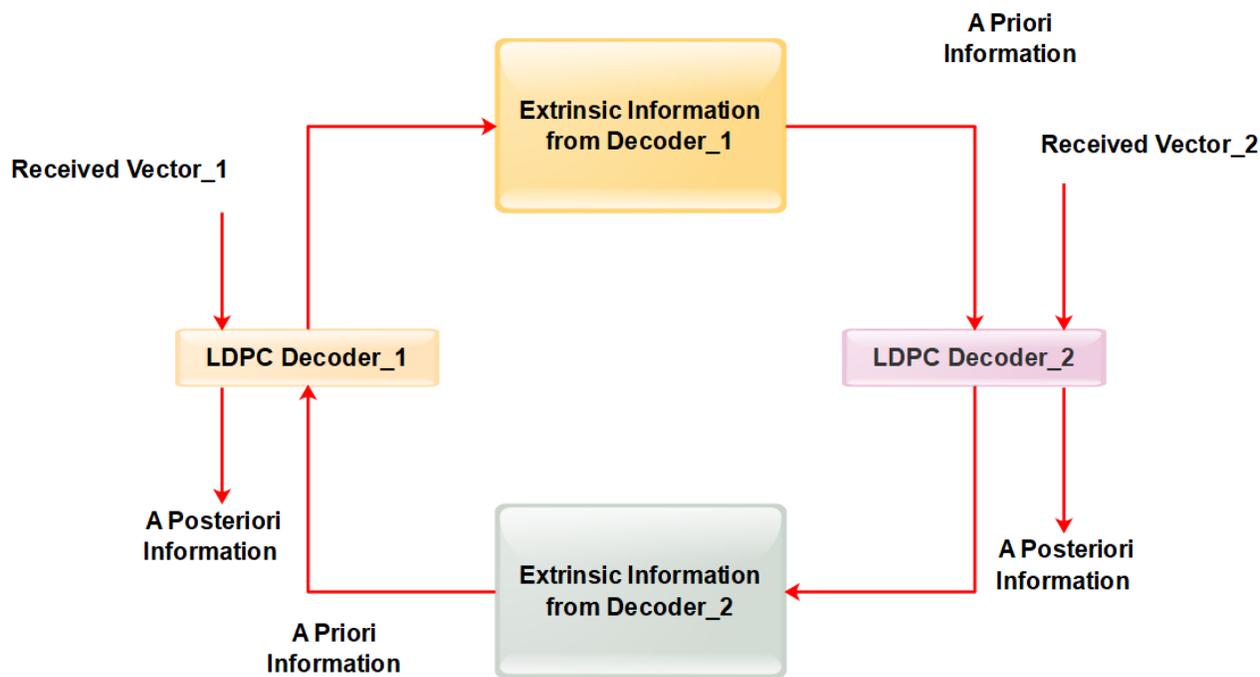


Fig 3. PGC conventional decoder

In conventional PGC procedure, there are some limitations are reported. In each decoder component after performing a fixed number of local iterations, the reliability i.e. log-likelihood ratio magnitudes of the systematic message bits are increased, so it becomes difficult for the next component decoder to correct a maximum number of errors. Hence, coding gain provided by concatenation of codes cannot be achieved. Further, local iterations perform by one decoder component, at the same time other decoder component remains idle. After the fixed numbers of local iterations, information exchange may take place. Therefore, in conventional PGC delay in the decoding process is more. An “extensive computer search” was required to select the component codes with different MCWs. As such, the efficacy of the scheme depends mainly on the complementary behaviors of the individual LDPC codes.

### 2.1 Multiple PGC

The generalization of PGCs codes are from the Multiple Parallel Concatenated Gallager Codes [MPCGC]<sup>(7)</sup>. The encoder for MPCGC is shown in Figure 4. Multiple LDPC encoders are connected in parallel in the structure of MPCGC instead of only two encoder components in conventional PGC. The LPDC component parity check matrices are constructed based on the MCW and also make sure that in parity check matrices weights of the row must be uniform. In order to reduce the complexity of MPCGC decoding and encoding, divide the long LPDC code into small subcodes, without compromising in performance. The encoding complexity of conventional LDPC code is quadratic to the block length which is comparatively higher than the sum of the complexities of the individual shorter component codes making up the MPCGC.

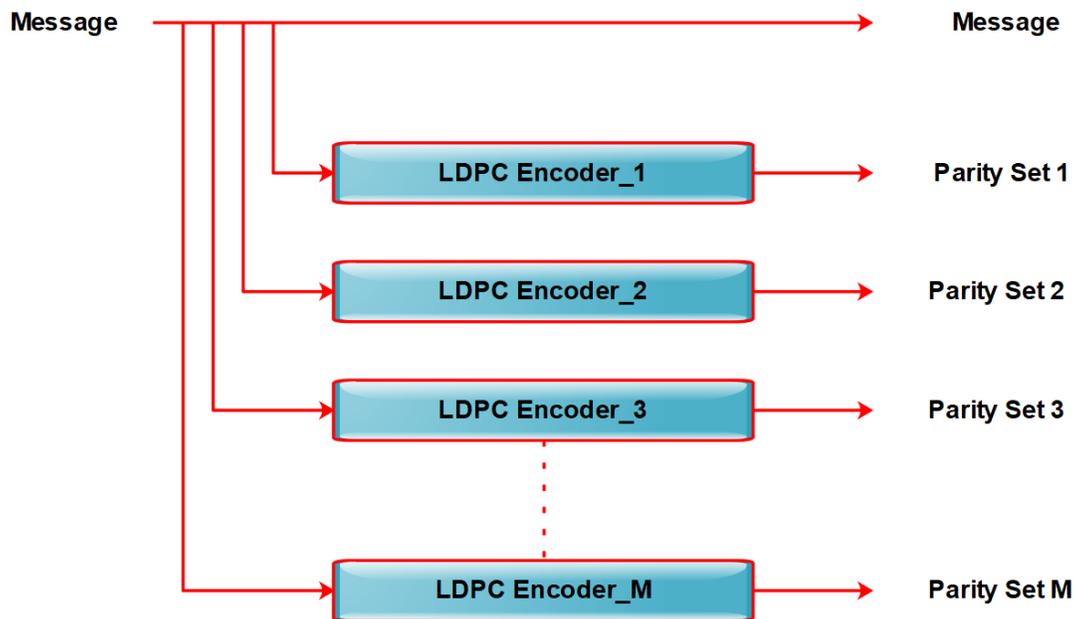


Fig 4. Multiple PCGC encoders

In terms of code parameters, the architecture of MPCGC has got flexibility in the greater potential to achieve the different code rates using different subsets of component codes. In order to adapt to different channel conditions, it is also possible to switch to different decoder configurations. This makes the architecture a desirable one for various applications.

It is observed that, with low MCWs, LDPC codes outperform, and with high MCWs at low to moderate SNR, while they exhibit low-grade performance at high SNR.<sup>(8)</sup> Based on this statement MPCGC is designed to combine the codes of MCW LPDC with low strength to a region of moderate SNR. The good design of MPCGC depends mainly on the choosing component codes in design parameters. An “extensive computer search” option was used to obtain relatively higher, moderate, and low LDPC codes.

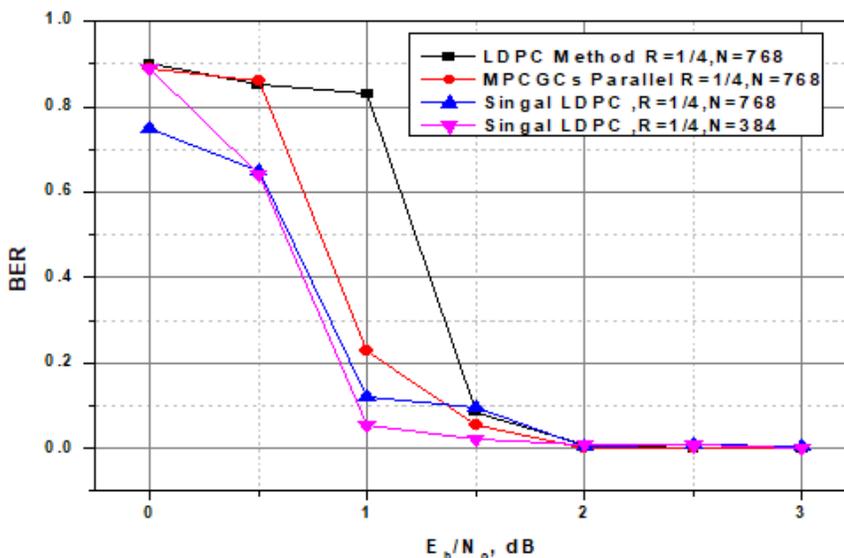


Fig 5. Effect of Bit error rate with respect to the code rate

Figure 5 shows the effect of MCW on the extrinsic information in PCGC conventional encoder for the various signal-to-noise range.

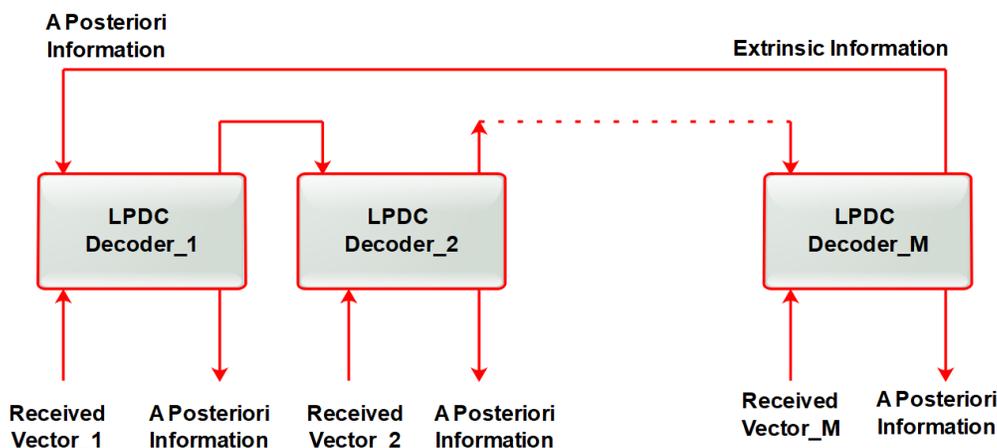


Fig 6. Serial Decoder of MPCGC

The serial decoder structure of the MPCGC is shown in Figure 6. The process of decoding in the serial decoder of MPCGC is similar to conventional PCGC, except that serial combinations of M component decoder are used. This serial process will lead to more delay in producing the required results. Therefore, parallel decoding process is presented in (9) and the corresponding structure of the MPCGC parallel decoder is shown in Figure 7. The decoding delay in the parallel decoding process is significantly reduced by performing an operation in parallel by all M decoders. From the analysis, it was found that at low SNR it is beneficial to increase the number of local iterations and decrease the number of super iterations. While at moderate to high SNR, a few local iterations and more super iterations are recommended (10).

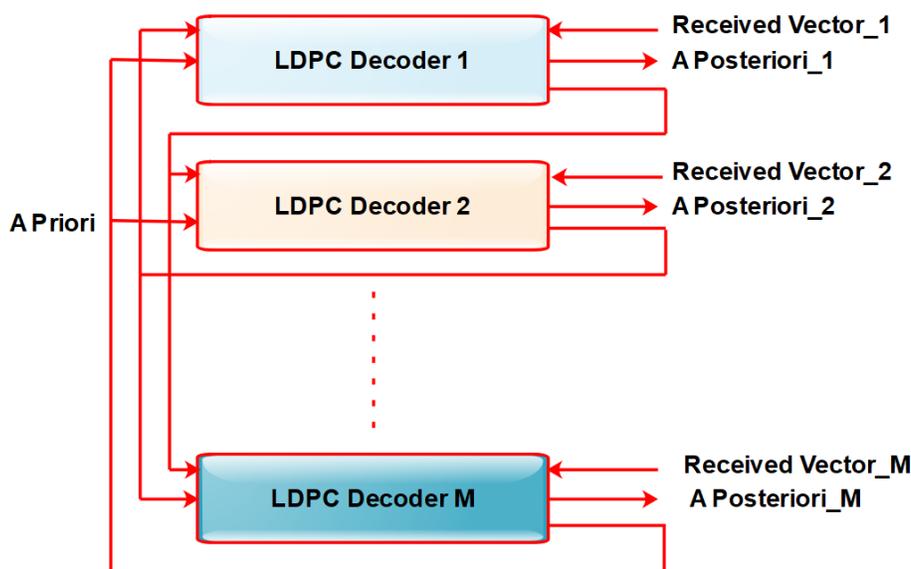


Fig 7. The parallel decoder of MPCGC

The main drawback of the parallel decoding process was that combination of high, medium, and low MCW LDPC were essential as component codes. Therefore, this scheme's efficiency is rested with the individual LDPC codes complementary behavior.

### 3 PCGC structure

The study shows that excellent bit-error rate (BER) performance can be obtained for large block lengths with the randomly constructed LPDC codes. But in hardware implementation, the memory required for non-zero elements representation for random matrix becomes more challenging. For the purpose of encoding and decoding the structured LDPC codes provides simpler implementations. The effectiveness of the decoding algorithms for LPDC codes is characterized by the parameter called Girth and it regulates the number of independent iterations. In the Tanner graph, the shortest cycle length is the parity check matrix or Girth of the LDPC code. The performance of the LDPC decoders degrades in the Tanner graph due to the short cycle having low girth because iterative decoding affects the exchange of extrinsic information<sup>(11)</sup>. Hence, LDPC code design with a large girth is of great interest. The construction methods of structured LDPC, the main objective is to maintain girth as high as possible in design LDPC codes. Based on Graphical models and Cayley graphs, the performance of half-rate, two structured, and parallel concatenated LDPC codes are evaluated<sup>(12)</sup>. The performance is obtained through well-structured procedures of two concatenated LDPC codes and compared with the same length of two randomly created LDPC components of conventional PCGC.

This method is less attractive for long block lengths because, as the length of the individual codes increases the SNR value at which they will be outperformed by the parallel concatenated code is increased. Therefore, it can be concluded that this method is a very good option only for short block lengths and high SNR values. Also, it could replace a single LDPC code of the same length.

### 4 Two sets of source bits of PCGC

The two sets of source bits structure has got better performance compared to conventional PCGC because it depends on the architecture of concatenation<sup>(13)</sup>. The code selection of distinct components is not required for this method and used two different parity check matrices<sup>(14-16)</sup>. The data interleaving between decoders component needs to be ensured, because of using parity check matrices of two different. At the side of the transmission, this structure has two copies of the source message bits, therefore, channel information is needed not be removed from the posterior metrics. Also, during extrinsic information computing, this information was shared between the two decoder components and prior information was removed. The two copies of source message bits are transmitted because one decoder component received information is different, hence source bit information received independently by the other decoder component.

First, at the transmitting side duplicate the message bits and then different generator matrices are used to encode the set message bits to develop the set of two codewords, which are then concatenated. The structure of the concatenated codeword at the transmitting side is shown in Figure 8. The resulting code is modulated further using binary phase-shift keying (BPSK) and is then sent through the additive white Gaussian noise (AWGN) channel.

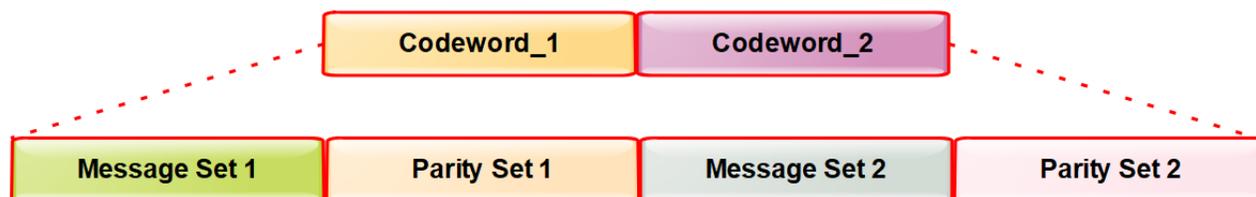


Fig 8. Structure of PCGC concatenated code word with two sets of source bits

The PCGC decoder architecture with source bits of two sets is shown in Figure 9. At the side of the receiving link, the received packet of the first set is assigned to the first decoder, and vectors of the second set are assigned to the second decoder.

The extrinsic information is shared between the systematic message bits of the two-component decoders.

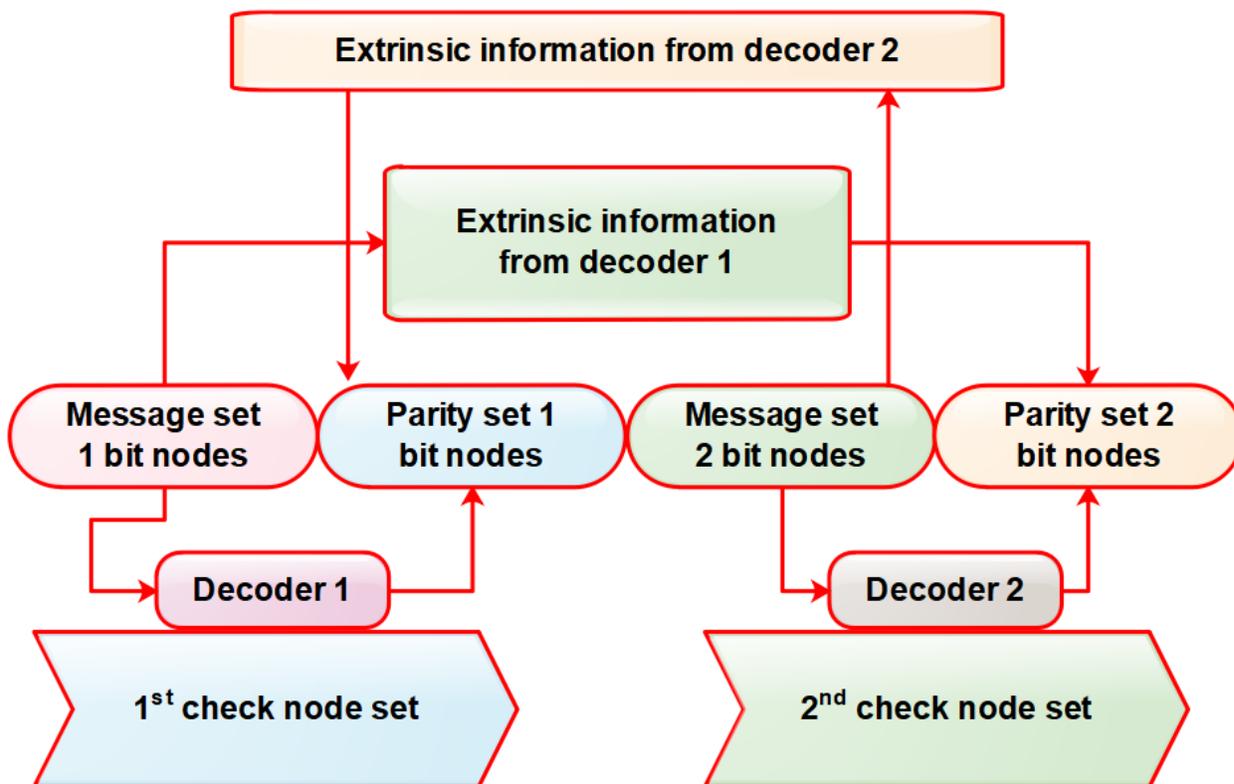


Fig 9. PCGC architecture of decoder with source bits of two sets

### 5 Single encoder PCGC

Only a single component LDPC code with  $MCW > 2.5$  is used in a single encoder PCGC<sup>(17)</sup>. The message bits corresponding same parity bits are transmitted twice. A single encoder PCGC structure with concatenated codeword and encoder is shown in Figure 10. In this structure complexity of encoding is significantly reduced and is less compared to the other parallel concatenation techniques.

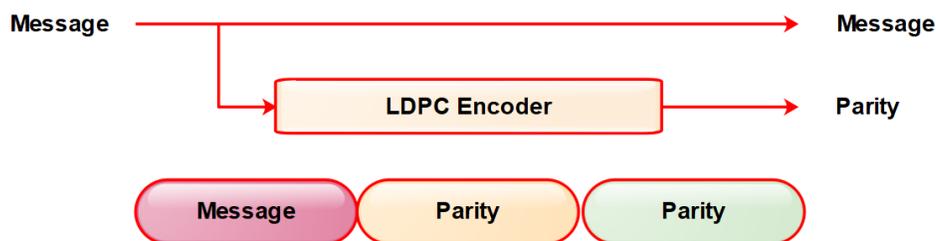


Fig 10. A single encoder PCGC structure with concatenated codeword and encoder

The decoder for PCGC with a single encoder is shown in Figure 11. At the side of the decoding two-component decoders are connected in parallel by using check nodes called the interconnecting check node. Each interconnecting check node corresponds to one parity-check equation of the corresponding parity-check matrix and an edge joins an interconnecting check node and a bit node of each component decoder if that particular bit is involved in the corresponding parity-check equation. In the first step of the super iteration, both component decoders will independently and simultaneously perform one local iteration of the iterative decoding i.e. the intrinsic information from bit nodes are transferred to the check nodes of the corresponding decoder, and bit nodes are updated based on the extrinsic message available from the check nodes.

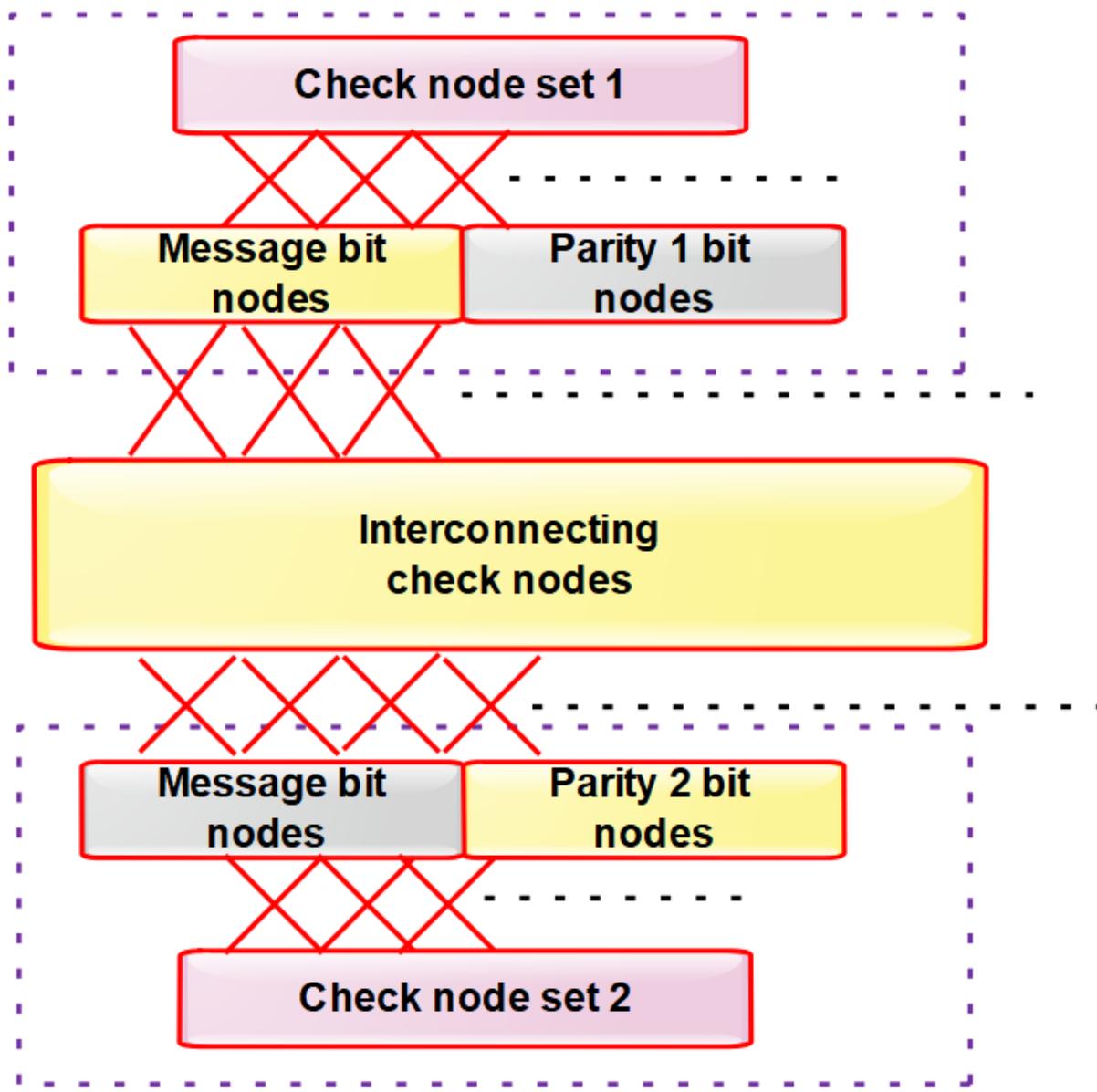


Fig 11. PCGC decoder with a single encoder

Further, in the next step decoder component, each bit is updated first (i.e. modified value likelihood ratio) by using intrinsic information of the second decoder component. Similarly, in the second decoder component, each bit is updated by using intrinsic information of the first decoder component. Until one of the decoders converges to a valid codeword this process

will continue or a maximum number of super iterations are over.

## 6 Modified PCGC

In the modified PCGC structure, two different sets of parity bits are transmitted for the same information block<sup>(18-21)</sup>. The zero syndrome criteria satisfy by parity bits of one set and non-zero syndrome criteria satisfy another set of parity bits. At the starting of the message block a '1' is added to generate the non-zero syndrome parity set from the second decoder. The performance can be slightly increased compared to PCGC with a single encoder, due to the increase in minimum distance for the carefully chosen syndrome vector, without any change in the complexity of the decoder.

The modified PCGC structure with concatenated codeword and encoder is shown in Figure 12.

Encoder for modified PCGC consists of a pair of simple LDPC encoders, one for obtaining code word that satisfies zero syndrome criteria and the other for obtaining code word that satisfies non-zero syndrome criteria.

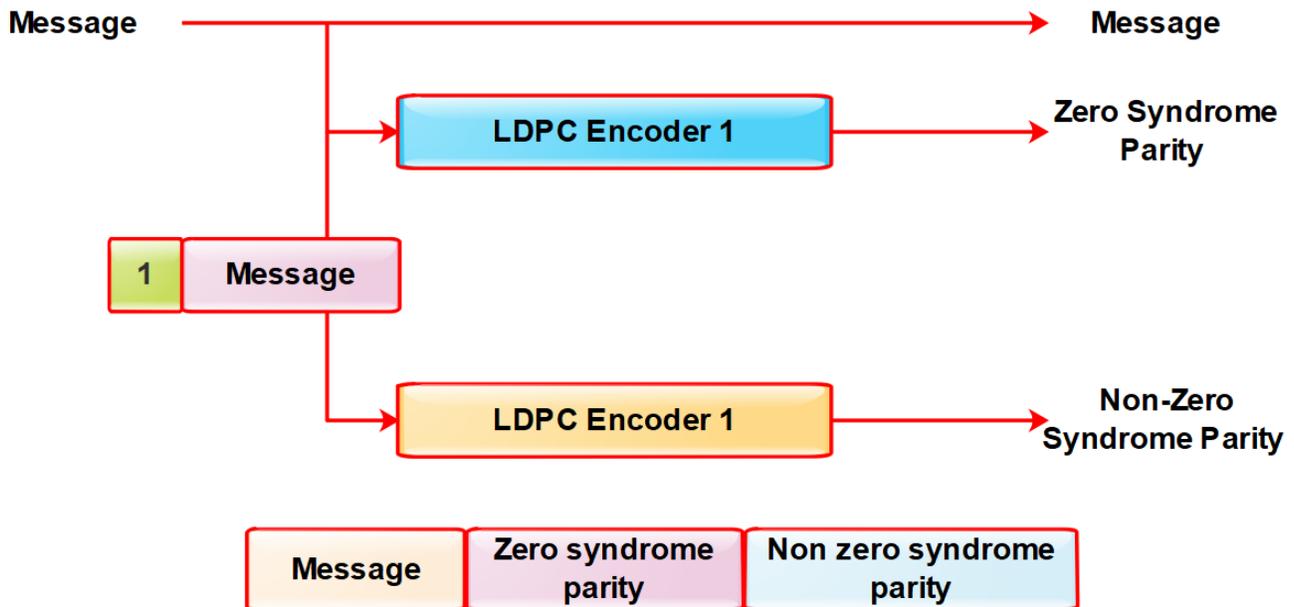


Fig 12. Modified PCGC structure with concatenated codeword and encoder.

For decoding, message-passing algorithm needed slight modifications to accommodate the non-zero syndrome criteria. Bit flipping algorithm is used for decoding. In the first step of the super iteration, the decoder will perform a local iteration with code word satisfying zero syndrome criteria. In the second step, the decoder will perform a local iteration with code word satisfying non-zero syndrome criteria. In the third step, intrinsic information is updated using the extrinsic information that each bit node received from the check nodes. Bit nodes corresponding to parity bits and systematic message bits are updated separately. This process of super iteration continues until one of the decoders converges to a valid codeword or a maximum number of super iterations are over.

The structure of the modified PCGC also has some limitations. The extrinsic messages received by each bit node during a super iteration are not fully independent and are correlated, which worsens the performance of the iterative decoding. It is because if there is a bit in error, then there is a possibility that the messages received by the bit nodes from the check nodes will be contradictory. So as to have improved performance, all the information received by a bit node has to be independent. Other demerits include its applicability only in Binary Symmetric Channel (BSC) and random selection of non-zero syndrome vector<sup>(22)</sup>.

## 7 PCGC with Interleaver

An interleaver is used, to make PCGC to be independent, when nodes received the extrinsic messages bit by bit. In PCGC with interleaver, nodes will receive the messages independently, because the parity equations will become entirely different by using an interleaver and this will make to improve the performance<sup>(23-26)</sup>. An interleaver PCGC structure with concatenated codeword and encoder is shown in Figure 13. In this interleaver structure message bits of parity, sets are provided by the first encoder, and message bits for interleaved parity set are provided by the second encoder. Here syndrome criteria are satisfied by both parity bits. The message bits randomly permutes by using a random interleaver. Because of the use of interleaver, the complexity of the structure is increased and this becomes the main drawback of this structure.

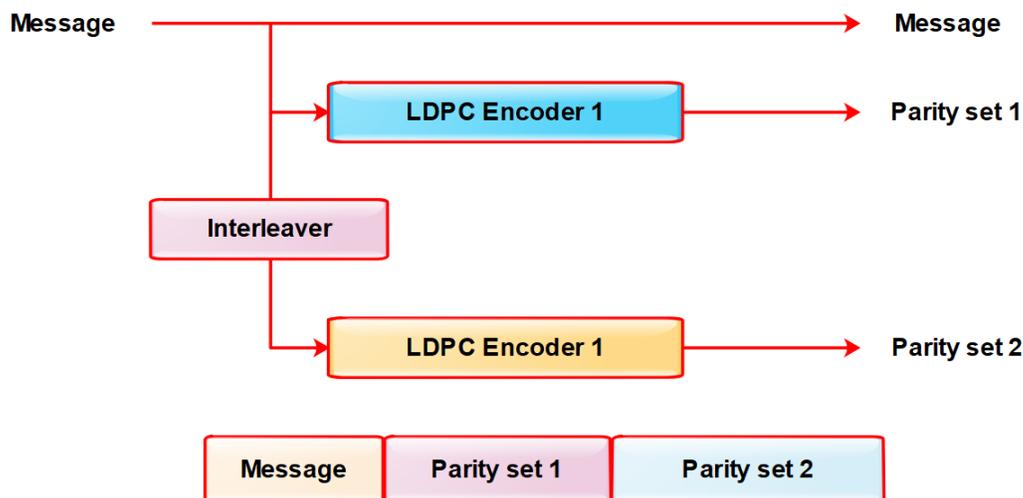


Fig 13. Interleaver PCGC structure with concatenated codeword and encoder

The decoder for PCGC with interleaver is shown in Figure 14. A simple LDPC decoder is used to decode both the codeword. It also consists of a register block, a random interleaver, and a de- interleaver.

In the structure of decoder for PCGC with interleaver contains two registers set Reg1 and Reg 2 to store code word. Also, total extrinsic information and intrinsic information is stored in these registers of a corresponding codeword of each bit. Decoder outputs the total extrinsic message for each bit after a local iteration. Decoder is connected directly as well as through interleaver and de-interleaver to register block. De-interleaver does the reverse operation of interleaver. Complexity and decoding delay will be more compared with other techniques due to the presence of interleaver and de-interleaver. Decoding delay can be reduced by using parallel set of decoders.

The algorithm called Bit flipping is used for the purpose of decoding. In the super iteration first step decoder performs a local iteration with the first codeword and the total extrinsic information is sent back to the Reg1 of the register block. The intrinsic information of message bits and parity bits are taken directly to decoder and total extrinsic information of the message bits and parity bits are transferred directly to the Reg1. In the second step of the super iteration, decoder performs a local iteration with permuted codeword and the total extrinsic information is sent back to the Reg2 of the register. Here the intrinsic information of message bits is taken to decoder through interleaver and that of parity bits are taken directly. While the total extrinsic message corresponding to parity bits is sent back through the direct path and the total extrinsic message corresponding to message bits is sent back through the de-interleaver. In the third step of the super iteration, intrinsic information in the register block (Reg1 and Reg2) is updated using the total extrinsic information received from the decoder. But the parity bits and the systematic message bits are updated separately. This process of super iteration continues until one of the decoder converges to a valid codeword or a maximum number of super iterations are over.

The performance of PCGC with interleaver is compared with modified PCGC in BSC<sup>(27-30)</sup> and results show PCGC with interleaver has better performance. In an AWGN channel, the performance of PCGC with interleaver is increased by a factor, which is the indirect increase of column-weight. This is because there is an indirect increase in the number of check nodes connected to each bit node without changing the number of bit nodes connected to each check node. Hence, this scheme of

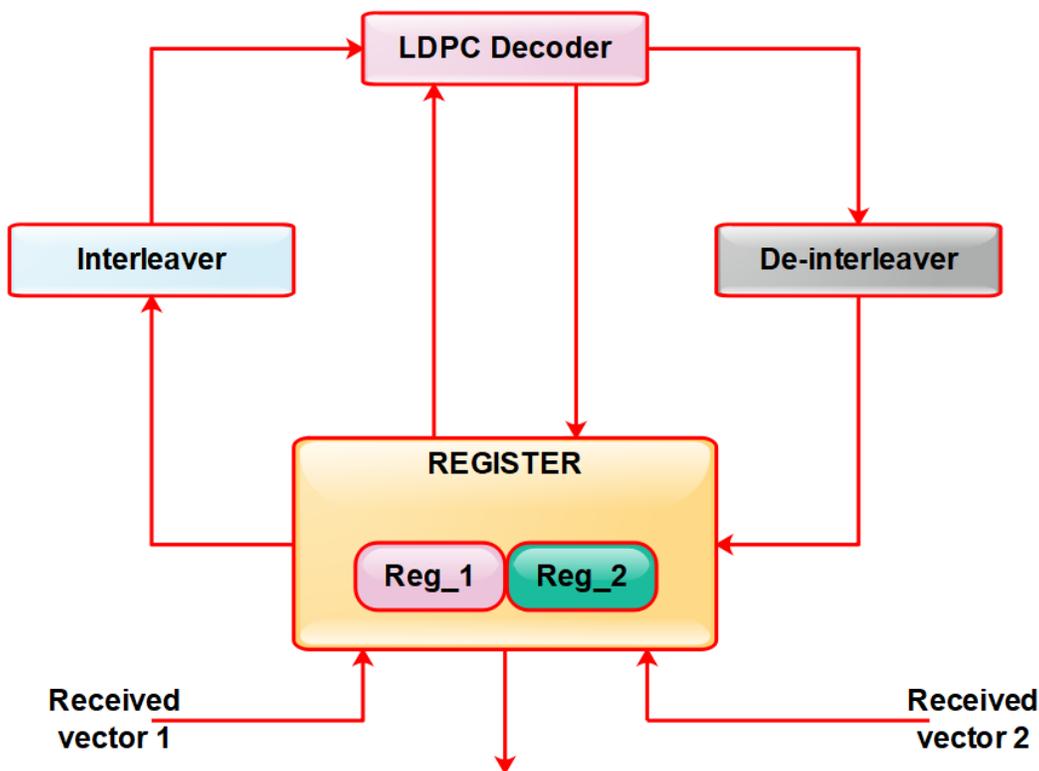


Fig 14. Decoder for PCGC with interleaver

concatenation provides the better performance as good a dedicated LDPC but with increased complexity due to deployment of an interleaver. The implementation problem associated with a longer block length iterative decoder is solved with PCGC with interleaver without much compromise in the performance.

### 8 Conclusion

The parallel concatenation of multiple LDPC codes is evaluated based on different decoding techniques. By breaking a long, high-complexity single LDPC code into multiple lower-complexity LDPC codes and appropriately exchanging extrinsic information among the component decoders, it is shown that a competitive BER performance can be achieved while still maintaining the low complexity and flexibility attributes of these strategies. By optimizing the construction of the component LDPC codes, the performance of MPCGC can be significantly improved and the complexity can be further reduced. MPCGC strategies can be attractive in applications where an on-line trade-off of resource vs coding performance is required; these are also advocated for the emerging multicore processing platform.

This study provides complete fundamental details of the design and implementation of LDPC codes by considering forward error corrections, error floor, and higher code rate for performance analysis. In recent years, the Low Density Parity Check (LDPC) code has found remarkable advancement and has seen them outshine turbo codes in terms of performance especially in the error floor and higher code rate. The performance and other inherent advantages make the LDPC codes the best choice for error-correction. However, complexity in the implementation of longer block length code is the main shortcoming of this code. In many practical applications, the LDPC codes outperform the turbo codes, therefore over turbo codes, the LPDC codes are not preferred because of this drawback. In terms of performance, parallel concatenation with interleaver structure is a good choice than the existing structure. However, the presence of interleaver makes this structure more complex.

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