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RESEARCH ARTICLE

Low Power PPN inverter based 10T SRAM Cell

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Abstract

Objectives: In the present power-hungry world, the objective of this paper is to design a system that helps in the reduction of power consumption of systems. A memory cell, more specifically an SRAM cell being the major contributor to the increased power becomes an important unit to be considered in such systems for reducing power. This paper presents an improved single-ended PPN inverter based 10T SRAM cell. **Methods:** The proposed cell makes use of PPN-inverters. The CMOS inverter is replaced by the PPN-inverter in the conventional 8T SRAM cell giving an improved single-ended PPN-based 10T SRAM cell. **Findings:** The proposed work is compared with other SRAM cells based on delay, power dissipation, and power delay product (PDP). The proposed cell is designed and simulated on Cadence Virtuoso EDA tool version IC6.1.7 at a standard CMOS 45nm technology. The simulation results show that the proposed SRAM cell consumes lesser power and hence lower PDP compared to conventional 8T SRAM cell as well as other SRAM cells and with the use of high threshold voltage transistors in the read circuit a further decrease in the power consumption is observed. So, by use of PPN inverter in 8T SRAM cell a new design for low power consuming SRAM cell is achieved. **Novelty:** The proposed cell is optimized in terms of power dissipation making it more efficient for use in portable battery-operated devices.

Keywords: 10T SRAM cell; Low power; PPN inverter; Static RandomAccess Memory (SRAM)

1 Introduction

Power dissipation has become a major concern in applications where high performance is required. With the increase in the scale of integration, the applicability of circuits becomes limited due to the high increase in power and area consumption. The present demand and popularity of portable battery-operated devices such as mobile phones, laptops, and tablets, has made the designing of low power and efficient systems a necessity. These embedded systems require repeated charging so, the reduction in power leads to longer and better usability of these devices since many times these systems may not have regular access for battery recharging. Also, these embedded systems require

large memory which mainly consists of static random-access memory (SRAM) for storing data. Therefore, the designing of a power-efficient SRAM cell is an important concern, and reducing the power of even a single cell can further reduce the power of large systems and will help in improving the system power efficiency.

The conventional SRAM cell [1] comprises six MOSFETs, out of which four transistors (2 PMOS and 2 NMOS) form the two cross-coupled inverters, which are the storage units of the cell (that stores the logic "0" and logic "1"). And the rest two transistors (NMOS) are access transistors that provide access to a storage cell during the SRAM cell operations. With the increased technology scaling, the conventional SRAM cell suffers from read and write instability and also increased leakage power. For applications like portable battery-operated devices (that needs to be small and power-efficient) where regular recharging of batteries is not possible, lower power consumption is a major requirement along with small size. Thus, the power increase with the scaling down of technology becomes a major concern for such applications. To overcome the area issue and get a smaller size SRAM cell, 4T cell [2,3] is also possible but at the cost of increased static power. A 5T cell [4–6] also provides a significant reduction in area. With the increased need for low power, researchers moved to cell designs with more transistors (more area) compromising on the area aspect to design SRAM cells with lower power consumption as well as better cell operation. Many efforts have been made in the recent years for designing power-efficient SRAM cells [7–15] such as 8T [7], 9T [8], DE PPN10T [9], ST1 [10], ST2 [11], ST11T [12], SE PPN10T [13].

Out of these cells, DE PPN10T, SE PPN10T, ST1, and ST2 consist of 10 transistors each, and ST11T consists of 11 transistors. DE PPN10T (Differential-ended PPN10T) and SE PPN10T (Single-ended PPN10T) are PPN inverter based SRAM cells, and ST1, ST2, and ST11T are Schmitt-trigger-inverter [16] based SRAM cells. 4T cell consists of 4 NMOS and two resistors (in place two PMOS). Because of the lesser number of transistors, this cell has a size advantage over 6T cell, but, due to the presence of resistances (that needs to be high enough to minimize current value), it also is sensitive to noise and soft error and is slower as compared to 6T cell. The 5T cell is obtained by removing one access transistor from the conventional 6T SRAM cell. Although this cell allows for significant area savings and power reduction compared to the 6T cell, this cell suffers from difficulty in write '1' operation. 8T cell [17,18] that uses a separate read circuit provides better results in terms of stability, but this read circuit increases the area of the cell. A different read configuration with better power and data stability at the cost of increased area and read access time is given by the 9T cell [8]. DE PPN10T cell [9] uses an extra signal VGND that is attached to GND only during read operation else it is attached to V_{DD}, thus providing a separate read path resulting in better read stability but suffers from degradation in write stability. For better stability, other SRAM cells based on Schmitt trigger inverter (ST1, ST2, ST11T) are also designed. A Schmitt trigger is a circuit that increases or decreases the switching threshold of an inverter depending on the direction of the input change [19]. Schmitt trigger inverter offers a high static noise margin due to the presence of a feedback path. ST1 [20] and ST2 are differential 10T cells. ST1 comprises feedback transistors in its pull-down network and has better SNM but has the read-upset issue. To remove this read-upset issue, stronger feedback is created in the ST2 cell by the use of an additional control signal. This architecture results in a higher load on BLs, thus increasing read access time. A single-ended ST-inverter based cell, i.e., ST11T is also designed that uses a separate read circuit and has reduced leakage current. But this cell suffers from failure in the write '1' operation and higher write access time [21]. SE PPN10T cell that uses single-ended read operation and has a separate read circuit eliminates the need for VGND signal that is required by DE PPN10T cell and gives better power and stability results. Figures 1, 2, 3, 4, 5, 6, 7, 8, 9 and 10 shows different SRAM cells.

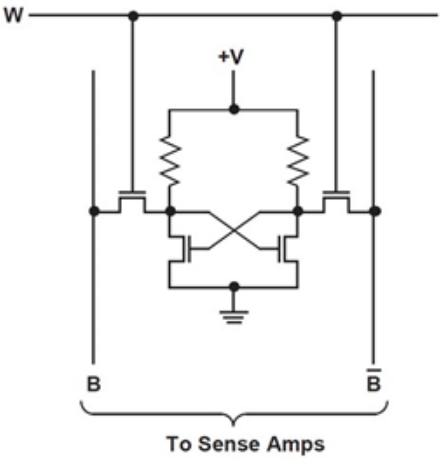

Fig 1. 4T SRAM Cell Schematic [2]

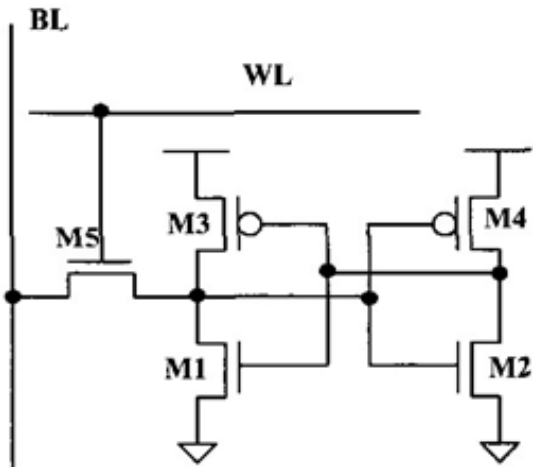

Fig 2. 5T SRAM Cell Schematic [5]

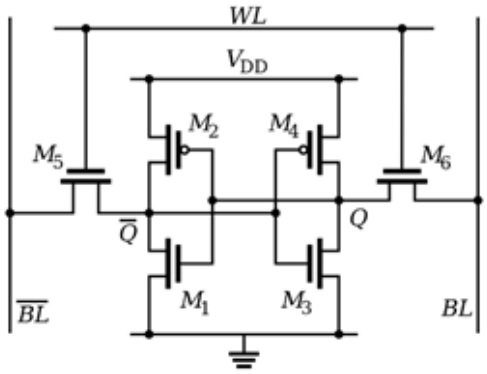

Fig 3. Conventional 6T SRAM Cell [1]

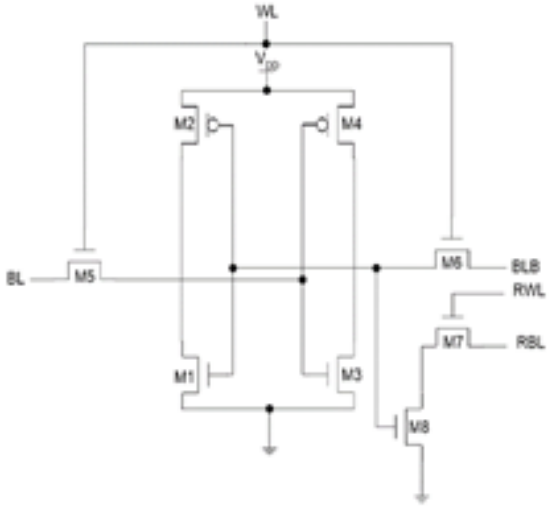

Fig 4. Conventional 8T SRAM Cell Schematic [7]

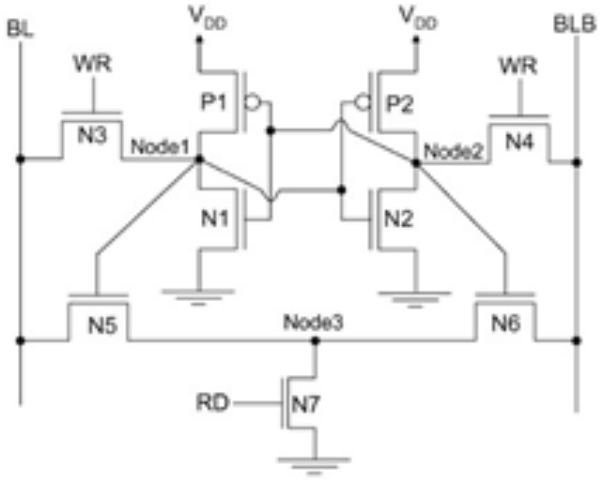

Fig 5. Schematic of 9T SRAM Cell [8]

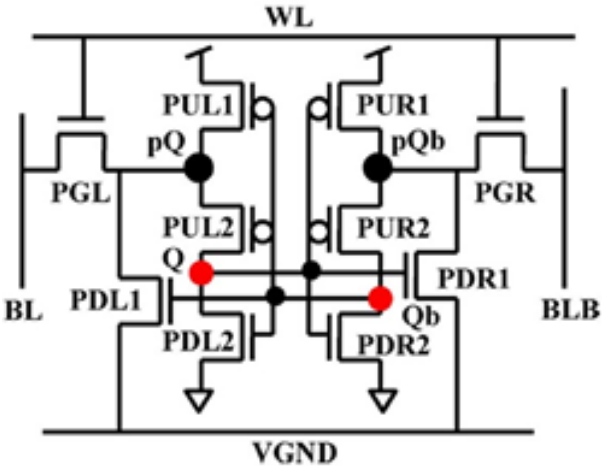

Fig 6. DE PPN10T SRAM Cell [9]

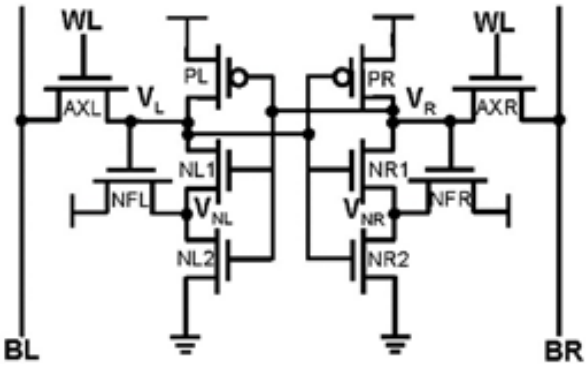

Fig 7. ST1 SRAM Cell [20]

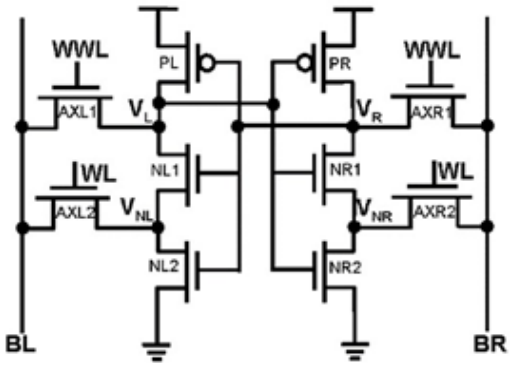

Fig 8. ST2 SRAM Cell Configuration [11]

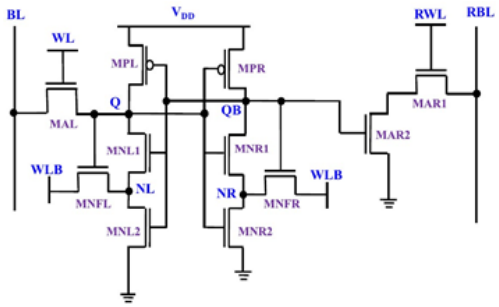

Fig 9. Single-Ended ST11T SRAM Cell [12]

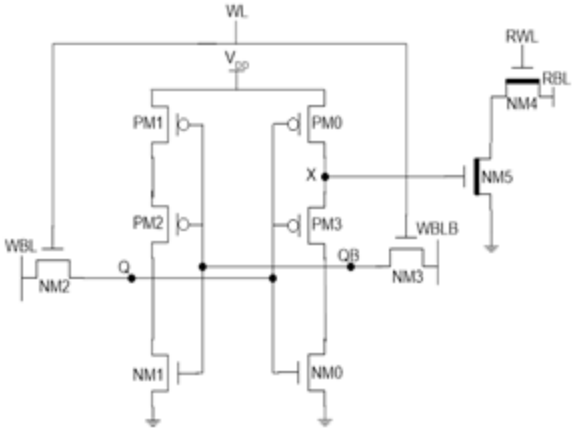

Fig 10. Reference SE PPN10T SRAM Cell [13]

*bold lines in NM4 and NM5 is to show hvt transistors

In this study, the main focus is on the reduction of power consumption of the SRAM cell. This paper presents a PPN inverter based SRAM cell consisting of 10 transistors that shows better result in terms of power consumption as compared to other SRAM cells. Rest of this paper is organized as follows: section 2 consists of description about the proposed SRAM cell and its working. Section 3 shows the simulation results and an analysis of results and finally section 4 presents the conclusion.

2 Materials and Methods

For power reduction, a new SRAM cell is proposed. Figure 11 shows the proposed PPN10T SRAM cell. The proposed cell is a PPN based cell because the proposed cell is designed by making use of PPN inverters as shown in Figure 12(a). A PPN inverter is a 3-transistor inverter where the transistors are cascaded in a PMOS-PMOS-NMOS sequence from top to bottom. The proposed cell consists of two cross-coupled PPN inverters. The PPN inverter is chosen for use in the proposed cell since PPN based SRAM cell has shown better result in terms of power consumption. The CMOS inverter is replaced by the PPN inverter in the conventional 8T SRAM cell as shown in Figure 12(b) resulting in an improved low power single-ended PPN based 10T SRAM cell, i.e., the proposed circuit. For designing of the proposed cell, transistor sizing considered is the minimum size for all the transistors (i.e. 120nm) except PMOS M2 and M5 that are taken as 240nm. The different SRAM operations, i.e., the read, write, and hold operations are performed by the turning ON and OFF of different transistors that take place by controlling different signals WL, BL, BLB, RWL, and RBL.

The proposed cell is further designed by using the dual threshold voltage technique to achieve a further power reduction. The dual threshold voltage technique is the use of transistors with different threshold voltages in the same circuit. Here, in the proposed cell, high threshold voltage transistors are used in the read circuitry of the proposed cell and regular or standard threshold voltage transistors in the remaining circuitry. The schematic remains the same as in Figure 11.

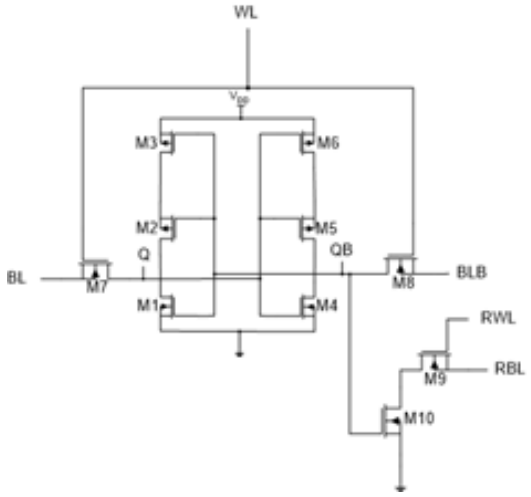

Fig 11. Schematic of Proposed low power PPN10T SRAM Cell

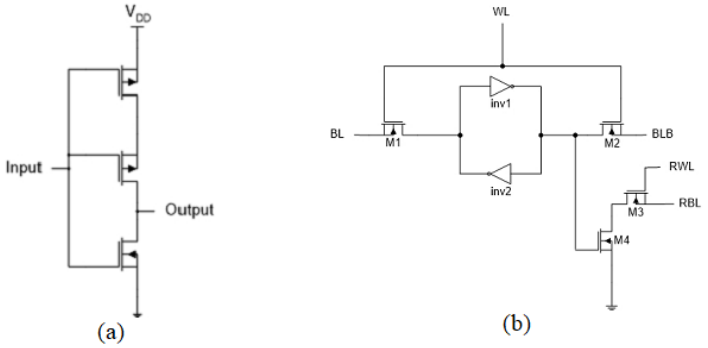

Fig 12. (a) Schematic of PPN inverter (b) Conventional 8T SRAM Cell Schematic with inverter symbol

2.1 Read Operation

The read operation in the proposed SRAM cell is performed by controlling the signals read word line (RWL) and read bit line (RBL). The read operation is performed by a separate circuitry consisting of transistors NM4 and NM5. The read operation is single-ended and read access transistor NM4 is controlled by RWL. For the read operation, RBL is charged to V_{DD}, WL is disabled (low), and RWL is enabled (high). With WL disabled, the write bit lines WBL and WBLB are completely isolated from the storage nodes Q and QB. This isolation helps in improvement of data stability. Figure 13 shows the transistor states during the read operation of the proposed cell.

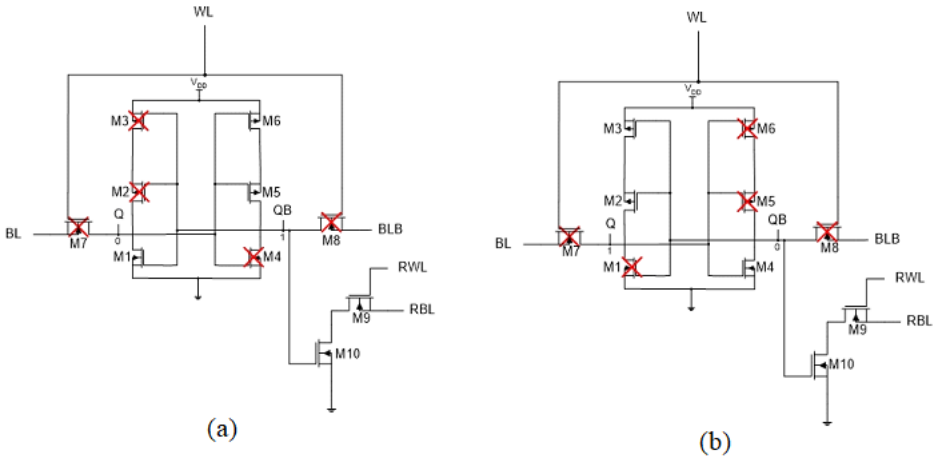

Fig 13. Proposed Cell Read operation (a) Read '0' operation (b) Read '1' operation

2.2 Write Operation

The write operation in the proposed SRAM cell is performed by activating the word line WL that turns ON the write access transistors M7 and M8. The bit lines (BL and BLB) are set or reset depending upon the data to be written to the cell, and transistors M7 and M8 facilitate the transfer of data from these bit lines to the storage nodes Q and QB. For the write operation, RWL is disabled, and RBL is precharged to V_{DD}. The write operation here is a differential process so, both the bit lines BL and BLB are assigned values depending on the data to be written. Figure 14 shows the transistor states during the write operation.

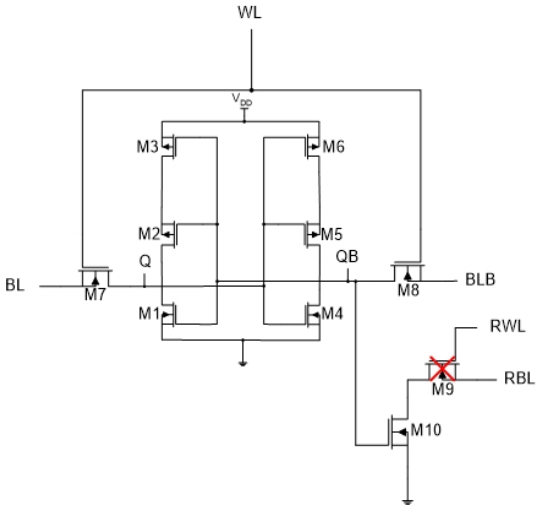

Fig 14. Proposed Cell Write operation

2.3 Hold Operation

During the hold mode, the data is neither written to the cell nor read from the cell. The cell stays in an idle state holding the data already stored in it. In this mode, both the word lines, i.e., the read word line (RWL) and the write word line (WL), are disabled which put the access transistors M7 and M8 in a cut-off state. As a result, bit lines BL and BLB are isolated from the PPN inverters, and no operation (read and write) takes place. Figure 15 shows the transistor states during the hold operation.

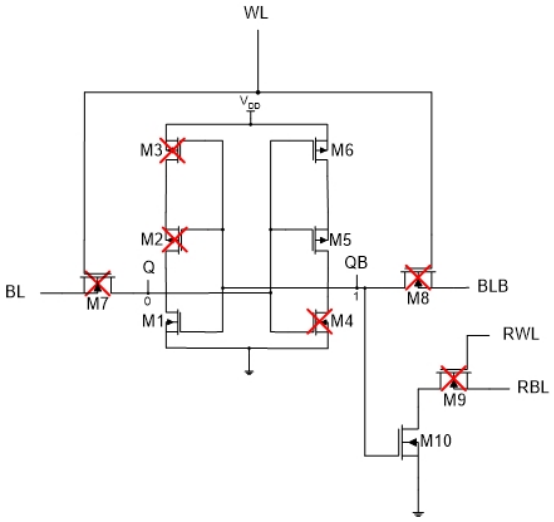

Fig 15. Proposed Cell Hold operation

This circuit has the advantage of PPN inverter like isolation of storage nodes, better write ability due to differential operation as well as low power and separate read operation of conventional 8T cell.

In conventional 8T cell schematic, use of transistors M3 and M4 makes a separate circuit — read decouple (RD) circuit used for improvement in stability of read operation. Addition of these transistors to the conventional 6T SRAM cell results in conventional 8T SRAM cell and helps in improvement of read stability and reduction of power consumption.

In the proposed circuit with PPN inverter, this read circuit transistors namely M9 and M10 are first designed by regular threshold voltage (rvt) NMOS. Regular (or rvt) transistors are nothing but normal threshold voltage transistors (operates at threshold voltage that a particular technology works at). The circuit with rvt transistors is simulated and analyzed to see the performance.

The same proposed circuit is again designed with change of transistors type, now the read circuit has been designed with hvt NMOS transistors to achieve further reduction in power. Hvt or high threshold voltage transistors are transistors that has slightly higher threshold voltage as compared to the normal threshold voltage transistors. The use of hvt transistors helps in reduction in leakage current and hence a decline in power consumption can be seen. This circuit with hvt transistors is also simulated and analyzed.

3 Results and Discussion

The proposed SRAM cell is designed and simulated in Cadence Virtuoso gpdk 45nm technology with a 1V supply voltage. Figure 16 shows the schematic of the proposed SRAM cell in Cadence Virtuoso.

For comparison, the proposed SRAM cell is compared with different SRAM cells based on power consumption, delay, and PDP. The different cells that are used for comparison are also designed in Cadence Virtuoso using similar technology and specifications as the proposed SRAM cell. The comparison of cells at room temperature (T=27°C) is presented in Table 1.

From Table 1 , we can see that proposed cell consumes less power as compared to conventional 8T SRAM cell, other 10T SRAM cells as well as reference circuit (SEPPN10T SRAM cell). Both the reference and proposed circuits contain same number of transistors (10T). The proposed design with hvt transistors in the read circuitry is also simulated and observed. We can see that use of hvt transistors helps in further decrease of power consumption and hence power delay product making it more energy efficient.

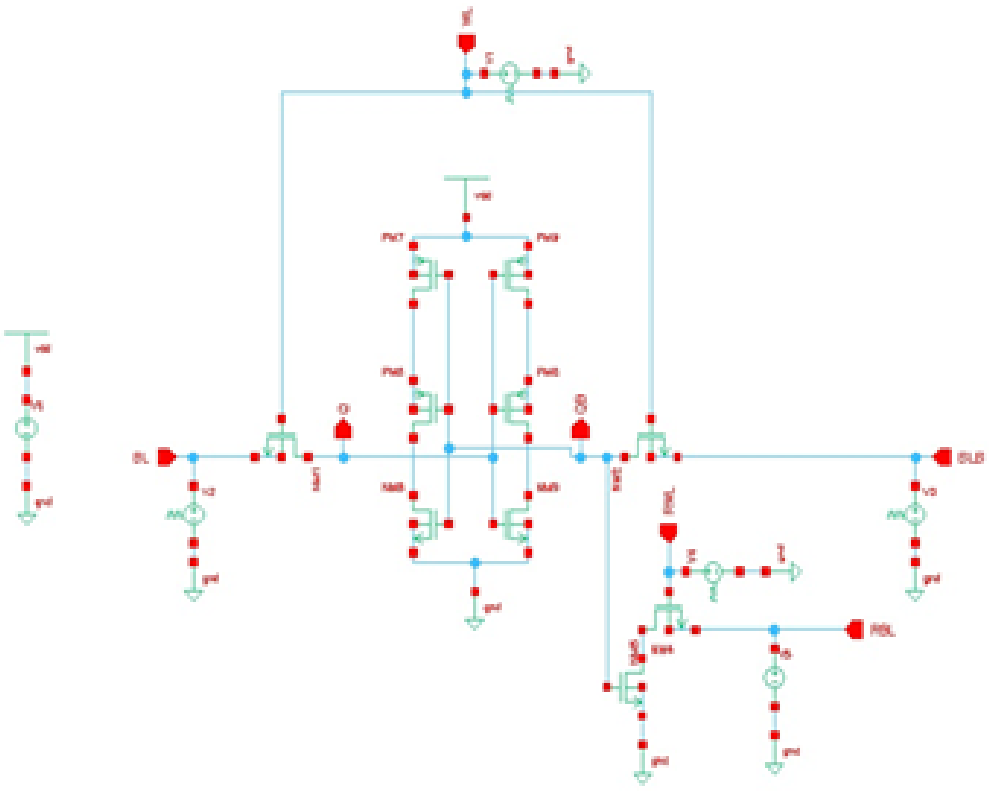

Fig 16. Cadence Virtuoso Schematic of Proposed low power PPN10T SRAM Cell

Table 1. Comparison between different 10T and proposed SRAM Cells at T=27°C

SRAM CELL TYPE	ST1	ST2	ST11T	DE PPN10T	Reference Circuit SE PPN10T	Conventional 8T SRAM Cell	Proposed PPN10T SRAM Cell	Proposed Cell with hvt transistors
TRANSISTOR COUNT	10	10	11	10	10	8	10	10
POWER (μW)	30.49	16.83	47.61	11.25	12.77	6.07	2.12	0.91
DELAY (ns)	20.30	20.29	19.86	40.46	20.27	20.26	20.27	20.29
PDP (fJ)	618.94	341.48	945.53	454.77	258.84	122.97	43.13	18.58

The temperature analysis of cells for temperature range of 25-50°C is also done, and a comparison between different cells is shown in Figure 17 (power comparison), Figure 18 (delay comparison), and Figure 19 (PDP comparison).

The temperature analysis of the cells over a temperature range of 25-50°C also show that the proposed design has better performance as compared to previous SRAM cell designs.

The proposed cells' power consumption with increasing temperature is compared to reference circuit and it is observed that a significant reduction is obtained in the proposed cell.

For all the cells involved, the power consumption and delay are calculated considering all the possible combinations of control signals. The power here is the average transient (dynamic) power during write operation. The power delay product (PDP) is then calculated by multiplying the power and delay of the cell. Lower the power and delay, lower is the power delay product and better is the circuit performance.

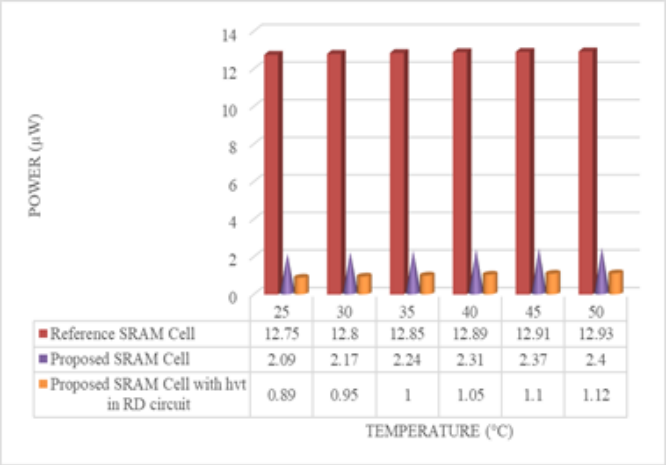

Fig 17. Power consumption of reference and proposed SRAM cells at varying temperature

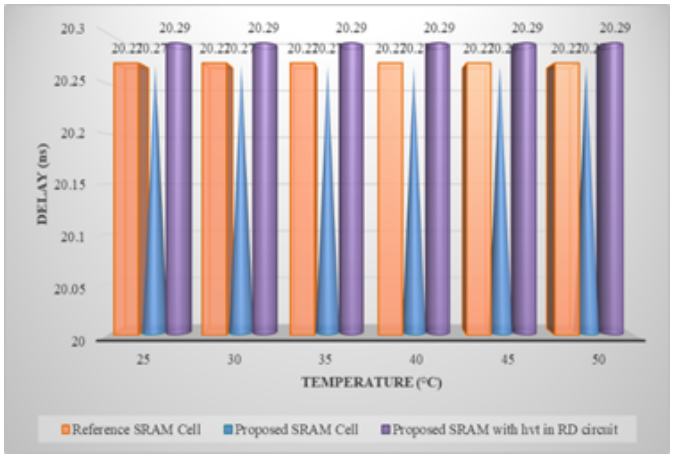

Fig 18. Delay of reference and proposed SRAM cells at varying temperature

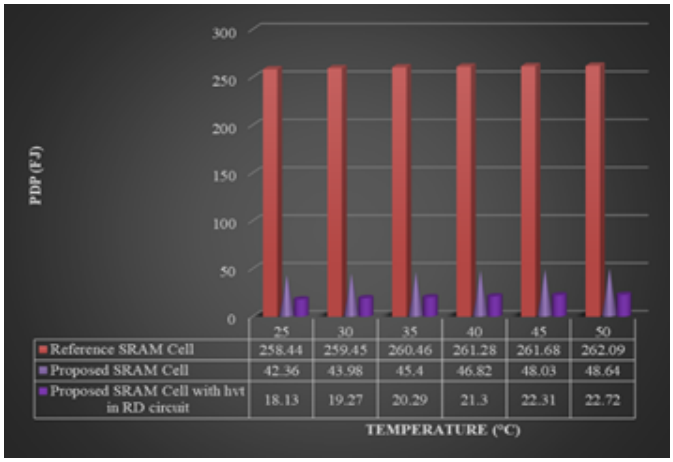

Fig 19. PDP of reference and proposed SRAM cells at varying temperature

4 Conclusion

The various SRAM cells have been designed in Cadence using gpdk 45nm technology, and a comparison is made between different SRAM cells and the proposed cell.

From the comparison, it is observed that the proposed cell 14x, 8x, 5x, 6x less power compared to ST1, ST2, DE PPN10T, reference SE PPN10T cells respectively, and 14x, 8x, 10x, 6x less PDP compared to ST1, ST2, DE PPN10T, reference SE PPN10T cells respectively.

The design using hvt transistors in read circuitry of the proposed circuit has a further power reduction, and it has 33x, 18x, 12x, 13x less power compared to ST1, ST2, DE PPN10T, reference SE PPN10T cells respectively, and 33x, 18x, 24x, 14x less PDP compared to ST1, ST2, DE PPN10T, reference SE PPN10T cells respectively.

The proposed 10T SRAM circuit designed using PPN inverter in the conventional 8T SRAM cell has the least power and PDP and is thus more power-efficient compared to other 10T SRAM cells and can be suitable for lower power applications. A few applications include cache memory, Internet of Things (IoT) applications, portable battery-operated devices such as mobile phones, laptops, and tablets, etc. and other devices that require lower power and repeated charging.

Limitations and Recommendations

The proposed SRAM cell with PPN inverter is designed using 10 MOS transistors, so as compared to previous cells there is no area reduction.

Further, the proposed cell can be analyzed for other SRAM performance parameters like RSNM, WSNM, voltage analysis, etc. Other than cell analysis, architecture level and device level techniques can be applied to enhance reduction.

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