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RESEARCH ARTICLE

Design and Analysis of Wideband PNP Sziklai Common Collector Amplifier with High Current Gain

Sachchidanand Shukla[1]*, Syed Shamroz Arshad[2], Pratima Soni[2], Aditya Kumar Sharma[2], Geetika Srivastava[2]

1 Professor, Department of Physics and Electronics, Dr. Ram Manohar Lohia Avadh University, Ayodhya, 224001, India
2 Department of Physics and Electronics, Dr. Ram Manohar Lohia Avadh University, Ayodhya, 224001, India

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* **Corresponding author**.

sachida.shukla@gmail.com

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Abstract

Objective: Objective of the manuscript is to introduce a novel idea of designing a small-signal common collector (emitter follower) amplifier with user-defined PSpice model of PNP Sziklai pair. **Method:** A circuit simulation program is developed on the PSpice simulation platform to design and study the proposed amplifier circuit. Small-signal AC equivalent circuit analysis authenticates the proposed amplifier design and selection of biasing components. The proposed amplifier is also implemented on Cadence Virtuoso Simulation software at 180nm technology to validate the design by performing its layout and post-layout simulation. **Findings:** The proposed circuit gives high current gain and smaller gain fluctuations (β) due to environmental parameter variations. The effect of variation in stage current gain of Sziklai pair components is observed under different operating conditions. Equivalent circuit analysis, noise performance, and the effect of temperature on the performance of the proposed circuit are widely discussed. Other possible circuit structures with a similar concept of design are also discussed as special cases. Highly stable amplifier current gain as well as device current gain, high amplifier voltage gain, device voltage gains below unity, and low harmonic distortion are prime features of proposed circuit. The problem of finding a matched pair of BJTs for the Sziklai pair is also addressed in the proposed design. The linear distortion-less operation of this circuit, combined with its very high current gain, makes it a suitable candidate for instrumentation amplifiers with wide operating frequency range. The proposed amplifier takes up (10.105 x 10.055) μm^2 of area at 180nm technology. The results of pre-layout and post-layout AC responses show that there is a close resemblance between the parameters before and after the layout, which promotes the usability and design of the proposed amplifier. **Novelty:** The idea explored in the manuscript is entirely new and first time announced by authors.

Keywords: PNP Sziklai Pair; Common Collector Amplifier; Current Gain; Small Signal Amplifier; Cadence Virtuoso

1 Introduction

Among three fundamental biasing concepts, Common-Collector (CC) configuration holds the highest input impedance[1]. It is generally a feedback circuit which is degenerative at low frequencies, but in the presence of drive inductance and load capacitance this becomes regenerative at high frequencies. Conventional CC amplifiers produce large current gain because the load resistor in the device configuration receives both the collector and base currents[2]. High level of negative feedback imposed by emitter biasing resistance in the CC amplifier results in less distortion in the amplified output. To avoid distortion in the amplified output signal, the transistor current gain β should not vary with either the collector voltage V_C or the collector current I_C. Common-Collector amplifiers have relatively better frequency response and less distortion in comparison to Common-Emitter and Common-Base amplifier circuits but sometimes it suffers from the higher gain fluctuation due to environmental parameter variation[3].

As a distinguishing feature, the CC amplifiers realize nearly unit voltage gain, high current gain and an input impedance much higher than output impedance. Due to unit voltage gain and high input impedance CC amplifier circuit is frequently employed as a voltage buffer and used for impedance matching in CRO, video stage of television receiver and voltage regulator in power supplies[3].

Variety of small-signal CC amplifiers using single BJT or paired BJTs like Darlington pair are being used by the electronics industry but use of Sziklai pair to design and study small-signal CC amplifier is attempted first time in the present manuscript[4,5]. The amplifier design, herein proposed for discussion, uses PNP Sziklai pair under CC configuration to develop a high-current-gain-wide-band small-signal amplifier.

A Sziklai pair, also known as Complementary Darlington pair, comprises two BJTs of opposite polarity and their basic advantage is lower base turn-ON voltage (∼625mV) which is almost half as compared to Darlington pair (∼1.36 Volts)[6]. The current gain factor of Sziklai pair ($\beta_{sziklai}=\beta_{Q1}\beta_{Q2}+\beta_{Q1}$) is slightly less than that of Darlington pair ($\beta_{darlington}=\beta_{Q1}\beta_{Q2}+\beta_{Q1}+\beta_{Q2}$) due to small amount of in-built negative feedback but for higher β values, current gain factor of both the devices are treated identical[7]. Sziklai pair is much thermal stable than Darlington pair due to lower quiescent current (10mA-100mA). Sziklai pair also shows better linear operations than Darlington pair[8].

Sziklai pairs, in electronic industry, are normally used to design quasi-complementary symmetry push-pull Class B power amplifier whereas Darlington pair has proved to be a suitable candidate for small-signal as well as the power amplifier designs[9]. In recent years attempts have also been made to develop small-signal amplifiers with Sziklai pair topology using CE configuration[10]. However, the present attempt is the first to use CC configuration in order to develop Sziklai pair topology based small-signal amplifier with matched BJTs of opposite polarity.

2 Circuit Details

The proposed CC small-signal amplifier circuit accommodates a Sziklai pair as amplifying device consisting user defined PSpice model of matched BJTs of opposite polarity. Respective BJT pair uses PNP transistor at driver position and NPN transistor at follower position, hence the device topology is said to hold PNP Sziklai pair structure[11]. Figure 1 shows the proposed circuit design of the amplifier under discussion with respective values of biasing resistors and capacitors.

The proposed circuit (Figure 1), biased with +18V DC supply, uses voltage divider biasing methodology. The reported observations are received by the aid of PSpice simulation and recorded for the input AC signal of 10mV, 1KHz provided to the

proposed circuit for amplification. User defined PSpice parameters used to design Sziklai pair of the proposed circuit are described in Table 1, which further clarifies that the Sziklai pair uses the matched BJTs of opposite polarity in the device structure.

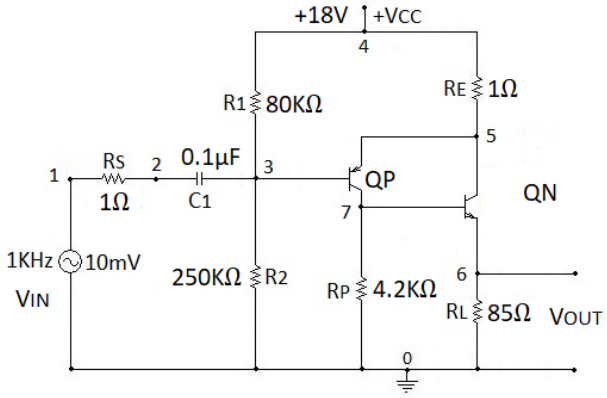

Fig 1. Proposed design of Common Collector Amplifier with PNP Sziklai Pair

Table 1. User Defined Model Parameters for the PNP and NPN BJTs used to constitute Sziklai pair in the circuit of proposed amplifier

Parameter Description	BJT Models with Respective Parameter Values	
	QP (PNP BJT)	QN (NPN BJT)
IS (p-n saturation current)	200.00E-18	200.00E-18
BF (Ideal maximum forward beta)	100	100
NF (Forward current emission coefficient)	1	1
BR (Ideal maximum reverse beta)	1	1
NR (Reverse current emission coefficient)	1	1
RB (Zero-bios (maximum) base resistance)	5	5
RC (Collector ohmic resistance)	0	0
RE (Emitter Ohmic resistance)	0	0
TF (Ideal forward transit time)	200.00E-12	200.00E-12
TR (Ideal reverse transit time)	5.00E-09	5.00E-09

3 Results and Discussion

3.1 Qualitative Performance

The proposed amplifier with biasing parameters and AC signal source as depicted in Figure 1 is capable to produce the Amplifier Current Gain A_{IGA}=3115, AC Current Gain of the Amplifier $A_{IGA-RMS}$=3115, Device Current Gain A_{IGD}=3280, Amplifier Voltage Gain A_{VGA}=73.121, AC Voltage Gain of the Amplifier $A_{VGA-RMS}$=73.111, Device Voltage Gain A_{VGD}=0.878, Bandwidth B_W=204.474MHz (with Lower Cut-off Frequency F_L=441.105Hz and Higher Cut-off Frequency F_H=204.475MHz), Power Gain P_G=53.557dB-Watt, and Total Harmonic Distortion THD=2.88%. It is to mention that Amplifier Current Gain is a measure of the ratio of the currents passing through load resistance R_L and input resistance R_S whereas device current gain is a measure of the ratio of I_{CQ2} and I_{BQ1}. However, the amplifier voltage gain is a measure of the ratio of the voltages at node 6 and node 1 whereas device voltage gain is a measure of the ratio of the voltages at node 5 and node 3. In addition, AC gain measures the ratio of RMS value of output to input voltages/currents [12].

The present topology of the small-signal CC amplifier with user defined PSpice model of Sziklai pair is also tested with unmatched BJTs under three conditions. These conditions and the basic behaviour of respective amplifiers are mentioned below as Case-1, Case-2 and Case-3.

Case-1: The Case-1 circuit design uses unmatched commercial PNP (Q2N2907A) and NPN (Q2N2222) transistors in the device configuration of Sziklai pair with biasing components R_S=100Ω, R_1=90K Ω, R_2=250KΩ, R_E=12Ω, R_P=2.7KΩ, R_L=100Ω, C_1=0.1μF, V_{CC}=+18V and is fed with the 10mV,1KHz AC signal source. Case-1 amplifier at room temperature provides seamless performance with A_{IGA}=301.05, $A_{IGA-RMS}$=301.05, A_{VGA}=7.6077, $A_{VGA-RMS}$=7.5938, B_W=3.9960MHz, P_G=33.598dB-Watt, A_{IGD}=316.01, A_{VGD}=0.977 and THD=5.71%.

Case-2: The Case-2 circuit design uses commercial PNP (Q2N2907A) transistor with user defined NPN transistor QN in the device configuration of Sziklai pair with biasing components R_S=100Ω, R_1=90K Ω, R_2=250KΩ, R_E=1Ω, R_P=2.7KΩ, R_L=31Ω, C_1=0.1μF, V_{CC}=+18V and is driven with 10mV,1KHz AC signal source. Respective circuit, at room temperature, amplifies input signal with A_{IGA}=1918.8, $A_{IGA-RMS}$=1918.8, A_{VGA}=27.213, $A_{VGA-RMS}$=27.079, B_W=1.5324MHz, P_G=47.17dB-Watt, A_{IGD}=1961.1, A_{VGD}=0.939 and THD=9.65%.

Case-3: The Case-3 circuit design accommodates user defined PNP transistor QP with commercial NPN transistor Q2N2222 in the device configuration of Sziklai pair with biasing components R_S=100Ω, R_1=90K Ω, R_2=250KΩ, R_E=1Ω, R_P=2.7KΩ, R_L=100Ω, C_1=0.1μF, V_{CC}=+18V and realizes 10mV,1KHz input AC signal source for amplification. Respective amplifier at room temperature provides seamless performance with A_{IGA}=2074, $A_{IGA-RMS}$=2074, A_{VGA}=78.953, $A_{VGA-RMS}$=78.140, B_W=44.666MHz, P_G=52.139dB-Watt, A_{IGD}=2138.8, A_{VGD}=0.832 and THD=3.00%.

It is also to note that due to the presence of in-built negative feedback, current gain factor of Sziklai pair is generally reduced but in the present paper, proposed amplifier provides high level of negative feedback imposed by R_E which results in less distortion and high current gain in the amplified output [13].

Coupling Capacitor (C_1=0.1μF) is used to pass only AC signal and block the DC signal from entering the base of PNP transistor. It is found that the variation in C_1 does not cause any change in amplifier current gain A_{IGA} while amplifier voltage gain A_{VGA} changes from 73.126 to 68.401 and bandwidth changes from 147.574 MHz (F_H=147.576 MHz, F_L=234.12 Hz) to 205.957 MHz (F_H=147.576 MHz) when C_1 is varied within the range 100pF$\leq C_1 \leq$100Mf [14].

Conclusively, the proposed circuit design with Sziklai pair obeys all the requisites of small-signal CC amplifier with matched or unmatched BJTs in the device configuration [15]. Case-1 and Case-3 circuits amplifies the signal with permissible limit of the THD than Case-2 circuit. However, the proposed amplifier along with Case-1, Case-2 and Case-3 circuits provide high current gains and wide band response. Respective findings clearly indicates that the small-signal CC amplifier circuit with wide application area in electronic communication can be successfully raised if BJTs in the device configuration of Sziklai pair are appropriately designed [16].

3.2 Qualitative Comparison with Other Configurations

A close comparison of the proposed amplifier with Small-signal CC Darlington pair amplifier and Small-signal CC BJT amplifier is also furnished under similar circuit environment ofFigure 1 and with the user defined model of PNP BJT of Table 1 [17] . The o only alteration in biasing component of the respective circuits is made with R_L, which is chosen 10Ω for both the situations. Respective observations, representing the basic performance of all the three amplifiers with the nomenclature Circuit-1, Circuit-2 and Circuit-3, are listed in Table 2.

Circuit-1 represents the proposed CC amplifier with user defined PSpice model of opposite polarity matched BJTs under Sziklai pair topology. Circuit-2 is the small-signal CC amplifier user defined PSpice model of matched PNP transistors under Darlington pair topology whereas Circuit-3 is small-signal CC amplifier with user defined PSpice model of PNP transistor [18].

Table 2 suggests that compared to Circuit-2 and Circuit-3 amplifiers the proposed amplifier (Circuit-1)provides higher Amplifier Voltage Gain, Device Voltage Gain and Power Gain. The proposed amplifier with less environmental fluctuations can be preferred over Darlington pair amplifier (Circuit-2) wherever amplification in wider-band is needed with high power gain.

Table 2. Comparison of the Performance Parameters for Circuit-1, Circuit-2 and Circuit-3

Performance Parameters	Circuit-1	Circuit-2	Circuit-3
A_{VGA}	73.121	8.4114	1.8202
F_L	441.105 Hz	157.816 Hz	2.8964 KHz
F_H	204.475 MHz	73.551 MHz	615.675 MHz
B_W	204.474 MHz	73.550 MHz	615.674 MHz
$A_{VGA-RMS}$	73.111	8.4102	1.8197
A_{VGD}	.878	0.843	.184
$A_{VGD-RMS}$	.878	0.843	.184
A_{IGA}	3115.0	8482.8	98.870

Continued on next page

Table 2 continued

$A_{IGA-RMS}$	3115.0	8482.8	98.870
A_{IGD}	3280.1	1010.0	100
$A_{IGD-RMS}$	3280.1	1010.0	100
P_G	53.557 dB-Watt	48.53 dB-Watt	22.52 dB-Watt
THD	2.88%	2.0%	3.20%

3.3 Small-signal Analysis

The small signal AC equivalent circuit of the proposed amplifier with matched BJTs of opposite polarity in Sziklai pair structure is shown in Figure 2.

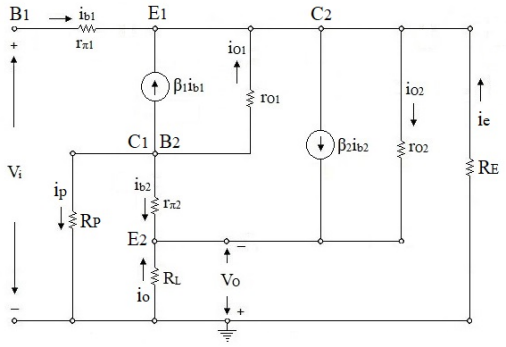

Fig 2. Small signal AC equivalent circuit of the proposed amplifier

For the present case, the current gain factors of the respective BJTs in Sziklai pair of the proposed amplifier are chosen to be β_1=100 and β_2=100 and therefore the simulation of the circuit provides Small-Signal AC Base Emitter Resistances $r_{\pi\,1}$=4.64x10^2 and $r_{\pi\,2}$=1.47x10^1 and Small Signal AC Collector Emitter Resistances r_{o1}=1.00x10^{12} and r_{o2}=1.00x10^{12}. Thus, the excessively high values of r_{o1} and r_{o2}, suggests to treat these resistances as open circuit and therefore to reduce the equivalent circuit as depicted in Figure 3.

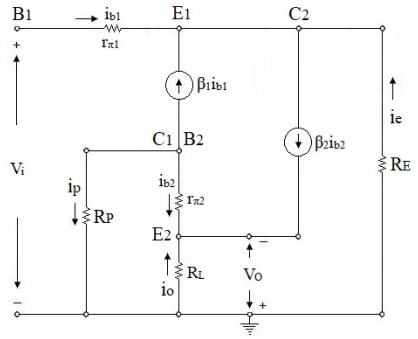

Fig 3. Reduced AC equivalent circuit of the proposed amplifier

Analysis of the equivalent circuit of Figure 3 provides the expression for the AC voltage gain of the proposed amplifier as –

$$A_V = \frac{V_O}{V_i} = \frac{-\beta_1(1+\beta_2)R_P R_L}{[\{(1+\beta_2)R_L - R_P - r_{\pi 2}\}\{r_{\pi 1} + (1+\beta_1)R_E\} + \beta_1\beta_2 R_E R_P]}$$

And the expression for the AC Current gain can be obtained as equal to –

$$A_I = \frac{i_O}{i_{b1}} = \frac{-\beta_1(1+\beta_2)R_P}{[(1+\beta_2)R_L - R_P - r_{\pi 2}]}$$

If the values of observed simulation parameters β_1, β_2, $r_{\pi\,1}$, $r_{\pi\,2}$ and R_E, R_P and R_L are placed in above expressions, the voltage gain is received below unity whereas current gain is found approximately equal to 9706. These observations clearly define the role of proposed circuit, with user defined PSpice models of matched BJTs of opposite polarity in Sziklai pair structure, as current amplifier with high power gain. The respective expressions also indicates that AC voltage and current gain of the proposed amplifier highly depends on additional biasing resistance R_P. It is observed that increase in R_P causes simultaneous increase in base voltage to NPN transistor Q2. This causes current through R_E to increase and current through R_L and therefore A_{VG} to reduce [19].

3.4 Effect of β Variation

Records in Tables 3, 4 and 5 depict the variation of performance parameters with different values of β for both the BJTs in the device structure of Sziklai pair.

Table 3 shows the status of performance parameters of the proposed amplifier at identical values ofβ_1 and β_2.However, performance parameters at different values of β_2,keeping β_1 fixed, are recorded in Table 4 and at various values of β_1,keeping β_2 fixed, are listed in Table 5.

Respective tables also mention 'percentage variation of A_{IGD}' which measures 'how much percentage of Actual A_{IGD} is less than the Theoretical A_{IGD}'.

In connection to Table 3, just to observe a quick comparison of the amplifier performance at identical values of β, response curves related to the amplifier and device current and voltage gains are sketched in Figures 4, 5, 6 and 7. Respective tables and the response curves of Figures 4, 5, 6 and 7 clearly suggests that the performance of the proposed amplifier with considered β values of the Sziklai pair structure are adequately in accordance of the amplifiers of this class [20,21].

Table 3. Performance parameters of the proposed amplifier at identical β values

Performance Parameters	$\beta_1=\beta_2$=5	$\beta_1=\beta_2$=10	$\beta_1=\beta_2$=15	$\beta_1=\beta_2$=25	$\beta_1=\beta_2$=50	$\beta_1=\beta_2$=100
A_{IGA}	25.263	87.783	177.718	417.481	1216.5	3115.0
A_{IGD} (Actual)	21.213	80.501	168.327	407.231	1226.7	3280.1
A_{IGD} (Theoretical) ($\beta_1.\beta_2$)	25	100	225	625	2500	10000
% Variation of A_{IGD}	15.148	19.499	25.188	34.843	50.932	67.199
A_{VGA}	4.6612	14.175	24.393	41.009	61.462	73.121
A_{VGD}	0.058	0.172	0.295	0.494	0.738	0.878
F_L	3.453KHz	3.032KHz	2.552KHz	1.843KHz	957.627Hz	441.105Hz
F_H (MHz)	201.462	115.850	95.350	90.428	117.908	204.475
B_W (MHz)	201.461	115.849	95.349	90.427	117.907	204.474
THD	3.01%	3.20%	3.41%	3.84%	3.189%	2.88%

Refer Table 3 As an obvious fact for small-signal BJT amplifiers, voltage and current gain of the proposed amplifier increases with rising values of identical β [3]. Records showing '% variation of A_{IGD}', suggests that the amplifier obeys more idealistic behaviour at lower values of β. Decrement in Bandwidth and increment in THD with rising β up to $\beta1=\beta2=25$ is also observed whereas bandwidth increases and THD decreases at higher β values.

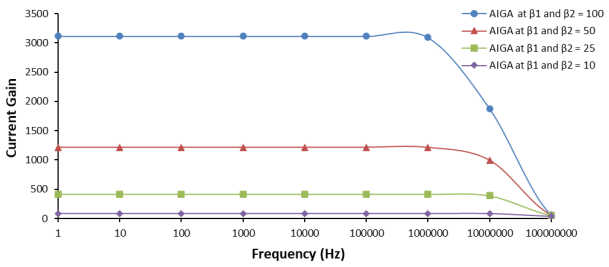

Fig 4. Distribution of Amplifier Current Gain on Frequency scale at identical values of $\beta1$ and β_2

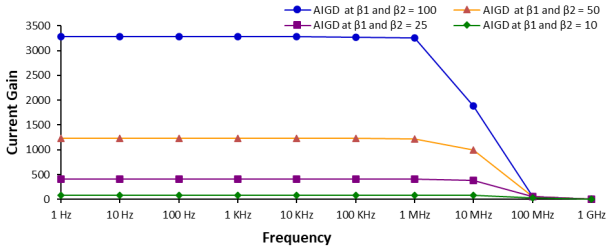

Fig 5. Distribution of Device Current Gain on Frequency scale at identical values of β_1 and β_2

Refer Figures 4 and 5 the nature of frequency response curves related to Amplifier Current Gain (Figure 4) and Device Current Gain (Figure 5) are almost similar and indicating amplifier's response in almost similar range of frequency at different β values for $\beta_1 = \beta_2$.

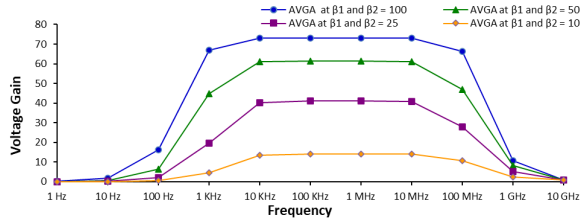

Fig 6. Distribution of Amplifier Voltage Gain on Frequency scale at identical values of β_1 and β_2

Refer Figures 6 and 7 the nature of frequency response curves related to Amplifier Voltage Gain (Figure 6) and Device Voltage Gain (Figure 7) are different but the upper cut-off frequency is almost similar for every condition and therefore indicating that device is responding in the range extended from extremely low to highest permissible frequency whereas the amplifier responds only in the frequency range limits between lower to upper cut-off frequency.

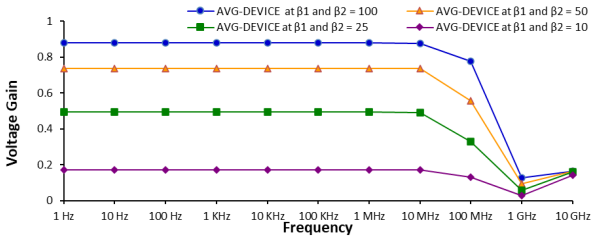

Fig 7. Distribution of Device Voltage Gain on Frequency scale at identical values of β_1 and β_2

Table 4. Performance parameters of the proposed amplifier at varying β_2 and fixed β_1

Performance Parameters	**β_1= 25 β_2=2**	**β_1= 25 β_2=5**	**β_1= 25 β_2=10**	**β_1= 25 β_2=15**	**β_1= 25 β_2=20**	**β_1= 25 β_2=25**
A_{IGA}	25.263	131.724	221.185	296.768	361.469	417.481
A_{IGD} (Actual)	69.703	110.818	203.305	281.664	348.903	407.231
A_{IGD} (Theoretical) ($\beta_1.\beta_2$)	50	125	250	375	500	625
% Variation of AIGD	39.40*	11.345	18.678	24.889	30.219	34.843
A_{VGA}	11.597	19.503	28.26	33.983	38.014	41.009
A_{VGD}	0.141	0.236	0.341	0.409	0.458	0.494
F_L (KHz)	3.1189	2.7940	2.3960	2.1449	1.9693	1.8434

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Table 4 continued

F_H (MHz)	521.813	232.637	143.138	114.315	100.726	90.428
B_W (MHz)	521.812	232.636	143.137	114.314	100.725	90.427
THD	3.21%	3.19%	3.32%	3.20%	3.20%	3.84%

Refer Table 4. When $\beta 1$ is kept fixed at 25 and $\beta 2$ is varied up to 25, value of THD changes in zig-zag manner whereas bandwidth decreases and current gain and voltage gain increases non-linearly. Record showing percentage variation of A_{IGD} verifies that the amplifier obeys more idealistic behaviour at lower values of β whereas, for β_1=25 and β_2=2, the actual current gain of the device is observed to be more than the theoretical value.

Table 5. Performance parameters of the proposed amplifier at varyingβ_1 and fixed β_2

Performance Parameters	**β_1=2 β_2= 25**	**β_1=5 β_2= 25**	**β_1=10 β_2= 25**	**β_1=15 β_2= 25**	**β_1=20 β_2= 25**	**β_1=25 β_2= 25**
A_{IGA}	0.022	80.133	165.999	250.208	333.99	417.481
A_{IGD} (Actual)	0.021	77.712	161.224	243.363	325.32	407.231
A_{IGD} (Theoretical) ($\beta_1.\beta_2$)	50	125	250	375	500	625
% Variation of AIGD	99.958	37.830	35.510	35.103	34.936	34.843
A_{VGA}	D	13.189	23.283	30.684	36.421	41.009
A_{VGD}	0.006	0.161	0.281	0.37	0.439	0.494
F_L (KHz)	D	3.0645	2.6300	2.3188	2.0527	1.8434
F_H (MHz)	D	58.699	66.185	73.534	82.769	90.428
B_W (MHz)	D	58.698	66.184	73.533	82.768	90.427
THD	41.48%	3.10%	3.19%	3.19%	3.20%	3.84%

D=Distortion

Refer Table 5. When β_1 is lowered to 2, keeping β_2 fixed at 25, all the response curves of amplifier circuit distorted sharply with very high value of THD whereas the percentage deviation of A_{IGD} of the Sziklai pair from it theoretical value reaches as high as to 99%. For higher values of β_1 under this situation, the percentage deviation of A_{IGD} of the Sziklai pair from its theoretical value gradually decreases.

Figures 4, 5, 6 and 7 also indicate that the poor response problem appears in conventional small-signal Darlington pair amplifier at higher frequencies is not observed for the proposed amplifier.

Hence the overall property is that β_1 is not to be selected below 5 to receive seamless outcome from the proposed amplifier. Moreover, the amplifier in discussion provides almost idealistic behavior for both the β values below 25 because when β_1 and β_2 increases up to 25, decrement in bandwidth and increment in THD is observed as usually seen in Small Signal amplifier, however at higher β values, performance of the proposed amplifier deteriorates as bandwidth increases and THD decreases [22,23].

3.5 Temperature Effect

Table 6 refers the status of performance parameters at different environmental temperatures for the amplifier under discussion. It is observed that the bandwidth and the amplifier as well as the device voltage and current gains decrease almost linearly with temperature elevation whereas THD almost remains constant. The grade of decrement in amplifier and device current gains is considerably low. Similar situation is also with device voltage gain [24].

Table 6. Performance parameters of the proposed amplifier at variable Environmental Temperature

Performance	**Environmental Temperature (^{O} C) for the Proposed Amplifier Circuit**							
Parameters	**-30**	**-20**	**-10**	**0**	**10**	**20**	**27**	**50**
A_{IGA}	3119.5	3118.7	3117.9	3117.1	3116.3	3115.5	3115.0	3113.2
A_{IGD}	3280.7	3280.9	3280.5	3280.4	3280.2	3280.1	3280.1	3279.8
A_{VGA}	74.683	74.119	74.119	73.844	73.573	73.306	73.121	72.528
A_{VGD}	0.897	0.890	0.890	0.886	0.883	0.880	0.878	0.871
F_L (Hz)	451.753	448.267	446.005	446.311	446.210	441.903	441.105	437.525

Continued on next page

Table 6 continued

F_H (MHz)	251.118	244.429	229.616	226.295	219.884	210.336	204.475	193.221
B_W (MHz)	251.117	244.428	229.615	226.294	219.883	210.335	204.474	193.220
THD	2.89%	2.89%	2.89%	2.89%	2.89%	2.88%	2.88%	2.88%

It is to note that small-signal Common Collector amplifier with single BJT suffers from the higher gain fluctuations due to environmental parameter variation [4]. However, the change in environmental temperature in the range of -30°C $\leq$ T $\leq$ +50°C does not seriously affects the performance parameters of the proposed circuit having Sziklai pair with user defined model of matched BJTs of opposite polarity and therefore the proposed amplifier is said to be almost free from higher gain fluctuation due to environmental parameter variation.

3.6 Noise Performance

Input and output noises for the circuit under consideration have also been figured out at operational frequency 1KHz and other frequencies 100Hz, 100KHz and 100MHz above and below to the operational frequency and respective findings are recorded in the Table 7. Basically, during the amplification process, active and passive components of the circuit generate noise and interrupts the usual operation of the circuit as well. However, Table 7 clarifies that both input/output noises increase with temperature elevation which authenticate the noise sensitivity of the proposed circuit with temperature. It can also be observed that the respective noises reduce with frequency elevation within the response region (441.105Hz to 204.475MHz) of the proposed amplifier whereas noises become higher below this region at 100Hz.

Table 7. Input and Output Noises for proposed amplifier at different Frequencies and Temperatures

Temp (° C)	Noises at 100Hz		Noises at 1KHz		Noises at 100KHz		Noises at 100MHz	
	Out noise (V/Hz)x10^{-6}	In noise (V/Hz)x10^{-9}	Out noise (V/Hz)x10^{-9}	In noise (V/Hz)x10^{-9}	Out noise (V/Hz)x10^{-9}	In noise (V/Hz)x10^{-12}	Out noise (V/Hz)x10^{-9}	In noise (V/Hz)x10^{-12}
-30	1.0973	67.482	460.52	6.757	27.411	367.037	26.882	381.24
-20	1.099	67.616	459.9	6.771	27.974	376.01	27.279	391.173
-10	1.1007	67.751	459.47	6.785	28.528	384.897	27.661	401.023
0	1.1025	67.886	458.97	6.799	29.072	393.703	28.029	410.794
10	1.1042	68.022	458.49	6.813	29.608	402.431	28.383	420.489
20	1.106	68.158	458.03	6.827	30.135	411.085	28.725	430.113
27	1.1072	68.254	457.718	6.8377	30.499	417.101	28.957	436.808
50	1.1113	68.57	456.739	6.8705	31.668	436.637	29.682	458.58

3.7 Comparative Study of the State-Of-The-Art Small Signal Amplifier Designs with the Proposed Amplifier

Table 8 shows the performance of the proposed amplifiers with the similar designs reported recently. It is clear that the proposed amplifier produces higher voltage gain and lower output referred noise than earlier researchers [1–4,10] with high current gain and acceptable range of THD.

Table 8. Comparison of the Proposed work with the recently reported design

References	[1]	[2]	[3]	[4]	[10]	**This Work**	**Unit**
Design Strategy	Digital CMOS	Analog CMOS	Analog CMOS	Digital CMOS	Analog CMOS	Analog BJT	—
Year	2022	2021	2020	2023	2022	—-	—-
Technology	180	28	180	22 nm FDSOI	65	—	nm
Supply Voltage	0.4	1.0	±0.45	—	1.2	+18	Volts
Area	0.02	0.04	—	0.293	1.17	—–	mm^2
Voltage gain	35 dB	39.5 dB	30 dB	17 dB	22.8 dB	73.121	—
Band-Width	0.000001	0.001	9.53	9000	10600	204.474	MHz
Current Gain	—	—	—	—	—	3115	Mag

Continued on next page

Table 8 continued

Power Gain	—	—	—	—	—	53.557	dB-Watt
Slew Rate	—	—	—	—	—	—	V/ms
Input Referred Noise	395	2150	341	250	—	457.718	nV/$\sqrt{}$Hz
Output Referred Noise	—-	—-	—	—	—	6.8377	nV/$\sqrt{}$Hz
Total Power Consumption	0.000095	0.00071	0.81	28.8	15.5	—	mW
THD	1.8	—	—	—	—	2.88	%

3.8 Implementation of the Proposed Amplifier at 180nm Technology using Cadence Virtuoso Simulation Software

Proposed designs are also implemented and simulated using Cadence Virtuoso and Spectre simulation software at 180nm technology at room temperature and respective performances are tabularized in Table 9[25]. Refer Table 9 Proposed amplifier in Cadence virtuoso software uses additional biasing resistance R_P between collector of PNP transistor and supply voltage with the similar biasing parameters as shown in Figure 1. Under this condition, proposed amplifier produces higher voltage gain, higher current gain, lower input and output noise, lower THD, higher power gain at the cost the narrow bandwidth than the amplifier implemented in PSpice software. It must be noted that proposed design also works effectively without any biasing resistance. If R_P is removed from this design, current gain almost remains constant however voltage shift down from 111.37 to 67.04 with narrow band signal. However, in present investigation, biasing resistance R_P of 1Ω is used to preserve its voltage amplification property and to enhance the frequency band[18–20].

Table 9. Performance of the Proposed Amplifier at 180nm Technology (Pre-Layout)

Performance Parameters	Proposed Design at 180nm Technology
Amplifier Voltage Gain A_{VGA}	111.37
Upper Cut Off Frequency F_H (for A_{VGA})	35.4035 MHz
Lower Cut Off Frequency F_L (for A_{VGA})	9.1709 Hz
Band-Width B_W (for A_{VGA})	35.4034 MHz
Unity Gain Band-Width (for A_{VGA})	8.0028 GHz
Amplifier Current Gain A_{IGA}	2.3287 K
Device Voltage Gain A_{VGD}	0.655
Device Current Gain A_{IGD}	1.2151K
Power Gain P_A (in dB-Watt)	54.1388
Output Voltage Phase Difference θ^O	-179.489
Phase Margin θ_M of Voltage gain	-120.759
Total Harmonic Distortion THD	12.157E-6%
Total Power Consumption, P_W	2.9083 W
Input Signal Voltage	1 mV at 1KHz
Permissible Range of Input Signal Voltage	1μV-100 mV
Slew rate of output voltage	4.4483 V/us
Current across Source Resistance I_{RS}	553.235 nA
Current across Load Resistance I_{RL}	164.1382 mA
Voltage across source resistance V_{RS}	1 mV
Voltage across load resistance V_{RL}	13.95 V
Power Spectral Density	3.8235 fV^2/Hz
Input Noise	555.25 pV/sqrt(Hz)
Output Noise	61.8352 nV/sqrt(Hz)
Transfer Function	111.369 V/V

Figure 9 represents the voltage gain and current gain of the proposed amplifier with respect to frequency at 180nm technology under Cadence Virtuoso and Spectre Simulation Software. It is found that the response curves related to voltage and current gain of this amplifier is similar to the amplifier implemented in PSpice (Figure 1) with improved gain and bandwidth[21].

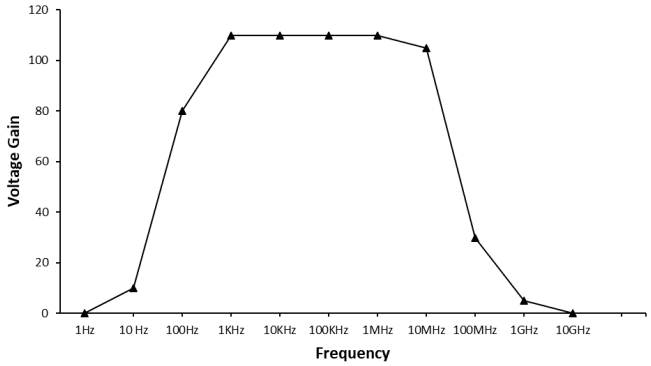

Fig 8. Distribution of Voltage Gain on Frequency scale

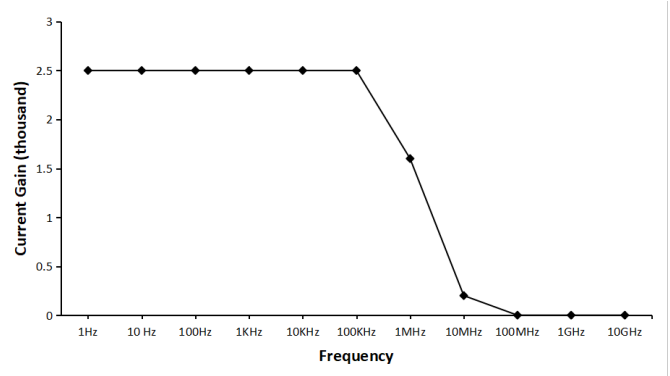

Fig 9. Distribution of Current Gain on Frequency scale

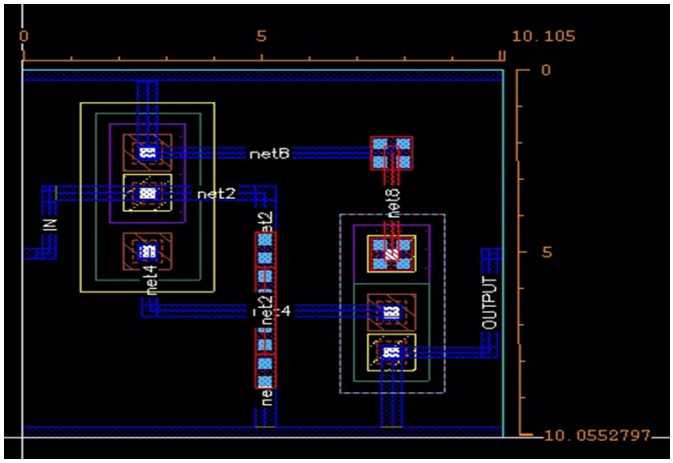

Fig 10. Layout of the proposed design

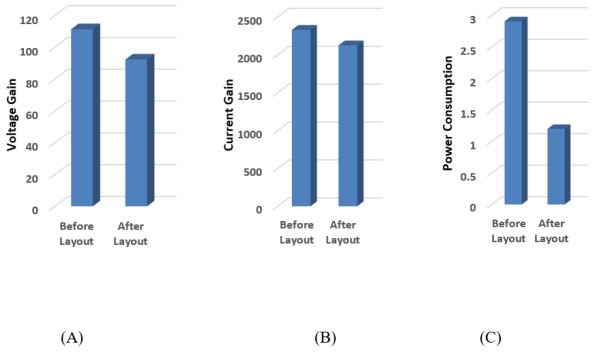

Fig 11. Variation of (A) voltage gain, (B) Current gain and (C) Power consumption before and after layout

Figure 10 depicts the layout of the proposed amplifier. The proposed amplifier takes up (10.105 x 10.055) μm^2 area, excluding the area of the compensation capacitor [25]. The simulation out-comes of post-layout express that the voltage gain, current gain and total power consumption are 92.281, 2.123K, and 1.2W respectively. The results of pre-layout and post-layout AC responses shows that there is a close resemblance of the parameters before and after layout. This resemblance promotes the usability and design of the proposed amplifier.

Statistical representation of variation of voltage gain, current gain and power consumption before and after layout is shown in Figure 11 (A), (B), and (C) respectively.

4 Conclusion

Sziklai pair topology is normally used to design quasi-complimentary symmetry push-pull Class B power amplifier. However, Sziklai pair with user defined PSpice models of matched BJTs of opposite polarity is being used first time in the present manuscript to develop a high-current-gain-wide-band small-signal CC amplifier. The proposed amplifier with modeled Sziklai pair effectively removes the problem of poor response of conventional small signal Darlington pair amplifier at higher frequencies and therefore the proposed model of Sziklai pair may be a good replacement of Darlington pair to design small-signal amplifiers. The proposed amplifier gives nearly ideal characteristics with high amplifier current gain and device current gains along with high amplifier voltage gain and a device voltage gain below unity. A highly stable current gain of more than 3000 is obtained with distortion free amplification of small signal AC input for wide frequency range. The linear distortion less operation of this circuit combined with very high current gain proves its suitability in instrumentation amplifier for a wide operating frequency range. The problem of finding matched pair of BJTs for Sziklai pair is also addressed in proposed design as the common collector amplifier design requires higher current gain of first stage and lower current gain for following stage. Not much work is reported on Sziklai pair based amplifier and this paper presents a genuine effort bring forward the high gain and wide frequency band suitability of Sziklai pair.

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