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RESEARCH ARTICLE

A Low Power Shift Register Based on Pulsed Latch

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Abstract

Objectives: To solve timing and power consumption issues in digital circuit design by creating a Low-Power Shift Register Based on Pulsed Latch (LPSR-PL). Targeting IoT sensors and portable devices for low-power operation, increase energy efficiency in shift registers by using numerous non-overlapping delayed pulsed clock signals, decoder-enabled design, and gated clock circuits. **Methods:** The work uses a unique strategy that decreases power consumption and timing difficulties by employing numerous non-overlapping delayed pulsed clock signals in the LPSR-PL. To improve data synchronisation, it combines latches into temporary store latches. The study uses a decoder-enabled design to compress control logic and simplify clock-pulse circuitry, resulting in power reductions. In addition, a gated clock circuit is designed to save energy by preventing pointless clock pulses during times of inactivity or static operation. **Findings :** The LPSR-PL is a good choice for contemporary digital circuit design as it efficiently addresses timing problems and reduces shift register power consumption. The employment of several non-overlapping delayed pulsed clock signals improves operating efficiency and data synchronisation. The employment of gated clock circuits, decoder-enabled architecture, and non-overlapping clock signals has led to significant advancements in low-power shift register designs. For applications where energy conservation is crucial, such as Internet of Things sensors and portable devices, this technology provides a more energy-efficient option. The suggested model performs very well with a much reduced power usage of 0.502 μW. **Novelty:** Power consumption and timing accuracy have been problems with conventional shift registers for a very long time. Conventional methods' dependence on a single pulsed clock signal often produced inefficiencies and subpar results. The LPSR-PL, however, has altered the rules of the competition today by offering multiple non-overlapping delayed pulsed clock signals that signify a new era in digital circuits.

Keywords: Pulsed latch; Flip flop; Shift register; Xilinx ISE; Decoder

1 Introduction

A shift register is an essential part of digital design that is used for data retrieval and storage. The shift register's conventional Serial-In Parallel-Out (SIPO) version is well-known for being straightforward and user-friendly [1]. However, the sequential flow of data bits across the full register causes delays, which is one of the main temporal restrictions of the SIPO design. Because of this flaw, SIPO is less appropriate for applications that need to analyse data quickly and in real time. Some of these restrictions are lifted by the Universal Shift Register (USR), which allows for both serial and parallel data shifting. Although its adaptability is a benefit, the USR paradigm adds complexity to control logic in order to handle the various data processing capacities [2].

Different shift register architectures in the field of digital circuits are designed to address different issues. An example of a time integrator with low power consumption and dynamic element matching is shown. It consists of a 9-stage bi-directional gated ring oscillator and a 16-stage bi-directional shift register [3]. By allowing bidirectional data shifting, the Johnson Counter Shift Register (JCSR) creatively addresses predictability problems with existing shift registers. This enhancement necessitates complicated control circuits, but at the expense of reduced energy efficiency.

In addition, innovations such as the pulse-coupled shift register (PCSR), delay flip-flop shift register (DFFSR), and low-power linear feedback shift register (LFSR) are attempts to improve power efficiency. Although these designs provide new methods, they still have difficulties meeting the very low power requirements of contemporary applications. Other strategies try to reconcile power optimisation with practical limitations. Examples include phase-based processing, delayed reset methods, and the usage of pulsed latches [4].

The invention of a novel 4-bit and 8-bit multi-bit shift register with parallel-in parallel-out (PIPO) operation demonstrates the ongoing quest of energy-efficient choices [5]. On the other hand, the pipelined 8-bit form's added complexity highlights the continuous difficulties in obtaining both fast speed and low power. Likewise, the recommendation to use pulsed latches as an energy- and space-efficient substitute adds complexity to the design and raises the need for temporary storage [6].

In order to increase power economy in digital circuits, the Pulse-Coupled Shift Register (PCSR) intentionally exploits the synchronisation of data transmission using pulsed signals. This novel strategy, nevertheless, faces a serious disadvantage. PCSR encounters significant timing difficulties since it is difficult to maintain exact synchronisation in dynamic applications. Additionally, despite its efforts to increase power efficiency, PCSR often achieves less significant total power reductions than projected. These restrictions emphasise how difficult it is to strike a balance between synchronisation and power optimisation in realistic, real-world situations, underscoring the continuous search for more durable solutions for energy-efficient digital circuitry [7]. PLR divides data processing into phases, boosting parallelism and maybe enhancing performance. The delay added between stages, on the other hand, limits its use for real-time applications needing low-latency data manipulation. By using delayed reset techniques to save power during times of inactivity, DRSR provides a distinctive strategy. However, it lacks the cutting-edge decoder-enabled design and non-overlapping clock signals that may further improve energy efficiency [8]. This study introduces a unique 4-bit and 8-bit multi-bit shift register with parallel-in parallel-out (PIPO) operation that operates at high speed, low power, and temperature tolerance. However, the pipelined 8-bit form adds complexity [6]. The Suggestion pulsed latches as a space-saving and energy-efficient replacement for conventional shift registers. Although this method uses non-overlapping pulsed clock signals to overcome timing concerns, it has downsides, such as greater design complexity brought on by the need of several sub shifter registers and an increased need for temporary storage [9].

With regard to these ten shift register types that are now in use, it is evident that each has a unique set of shortcomings that make them unsuitable for dealing with the pressing issues of modern electrical design. The ground-breaking Low-Power Shift Register Based on Pulsed Latch (LPSR-PL), a revolutionary strategy that overcomes the drawbacks of its forebears while promising unmatched improvements in energy economy and performance, will be unveiled in the pages that follow.

The main contributions of this paper are;

- This study introduces a revolutionary Low-Power Shift Register Based on Pulsed Latch (LPSR-PL) to handle shift registers' timing and power consumption issues.
- This study aims to solve timing problems and lessen overall power consumption by employing several non-overlapping delayed pulsed clock signals. These signals are used in combination with sub shifter registers and latches for temporary storage.
- Decoder-Enabled architecture streamlines the design's control logic and clock-pulse hardware. This simplifies things and makes them more efficient with electricity.
- It provides a gated clock circuit that reduces power consumption by eliminating unnecessary pulse production while data is not changing.

2 Methodology

A. Shift Registers

One of the most fundamental components of a VLSI circuit is the shift register[10]. Many electronic devices rely on shift registers, including digital filters, communiqué receivers, and image processing integrated circuits. The need for more picture data to be processed by image processing ICs has led to an increase in the word length of the shifter register in recent years. A 4Kbit shift register is used in a VLSI image-extractor and vector-generator processor. A 2K-bit shift register is used by a register rises. In order to save space and power, the shift register can make use of the slightest flip-flop possible. Since a pulsed latch is substantially more compact than a flip-flop, it has lately taken its place in many applications that formerly used flip-flops[10]. However, since pulsed latches have a timing issue with one another, they can't be employed in a shift register.

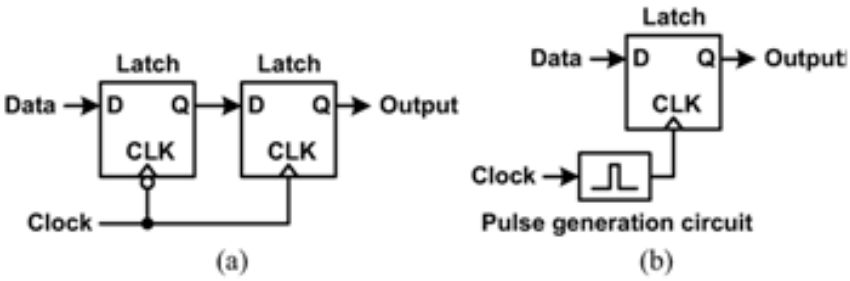

Fig 1. (a) Master-slave (b) Pulsed latch

This study suggests a shift register that uses pulsed latches to conserve power and space. The shift register eliminates the need for a single pulsed clock signal by generating frequent pulsed clock signals with delays that do not overlap. By clustering the latches into numerous sub shifter registers and making use of latches, the shift register makes efficient use of a relatively small number of the pulsed clock signals[11]. The inputs and outputs of shift registers can be either parallel or serial. parallel-in, serial-out (PISO) configurations are common for these. Types with serial input and types with parallel output are also available. Bidirectional shift registers can be used to move in either the directions. Connecting a shift register's serial input to its final output makes what is known as a "circular shift register." Measurements of energy use in the past frequently relied on a small sample of data patterns and clock switches at regular intervals. However, in reality, there is significant fluctuation in clock and data activity between various TE occurrences. Many TEs in low-power microprocessors, for instance, have input data transitions that dominate their energy usage, rather than clock transitions. The data input activity of other TEs is extremely low, yet they are nonetheless timed every cycle. Sequential logic includes shift registers in the same way that counters do. In contrast to combinational logic, the past has an effect on sequential reasoning in addition to the current inputs. Simply said, sequential logic may recall previous steps. An edge-triggered architectures to provide a brief transparent period. Unlike the master-slave flip-flops seen in Figure 1, pulsed latches may borrow time between clock cycles and only need one latch stage each cycle. In addition to being more vulnerable to timing risks, local clock pulse generators in pulsed latch designs waste energy.

B. Pulsed Latch Technique

The most frequent type of sequencer is the flip-flop. High sequencing causes delays, power consumption, and floor space that outweigh the benefits of synchronising flip-flops with the clock edge, which is commonly employed since it is compatible with static timing investigation. In comparison to the power used by a flip-flop, the latch uses very little energy while performing its function. However, due to the data transparent behaviour of latches, static time analysis might be tricky to use during design. A latch can store information for the length of time specified by the frequency of the clock signal. This is a very delicate operating window[12].

A pulse clock waveform can be used to activate a latch. Since edges of a pulse clock are almost equal in time, a latch that is synchronised by a pulse clock has behaviour that is comparable to an edge-triggered flip-flop. Setup durations of a pulsed latch are indicated relative to the increasing edge of the pulse clock, whereas hold times are uttered relative pulse clock in a pulsed latch approach. In this way, the pulsed latch's timing models are equivalent to those of the flip-flop[13].

Figure 2 depicts the use of two D latches to create a D flip-flop. The basic components of the pulsed latch approach are a pulse generator and a latch.

In Figure 3, we see a pulsed latch that, in terms of its functionality, is equivalent to a D flip-flop. One D latch and a simple pulse generator make up circuit, which is functionally equivalent to a D flip-flop. One of the best things about the pulse latch approach is that it works with any master-slave flip-flop setup by eliminating one latch per cycle and the clock's complement. Using the

pulse latch approach also has the additional benefit of increasing the efficiency of preexisting designs without necessitating any aesthetic changes.

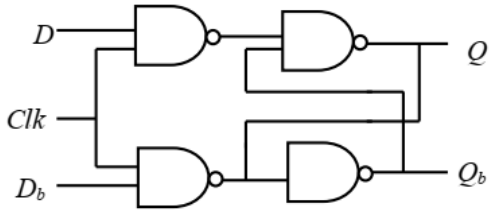

Fig 2. NAND based D latch

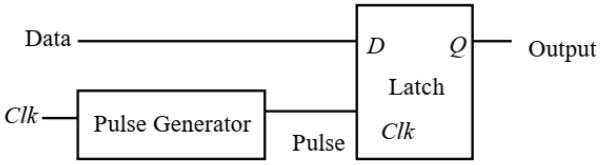

Fig 3. Pulsed latch technique

A pulsed latch's timing models are comparable to those of an edge-triggered flip-flop. The AND gate and NOT gate that make up the pulse generator are shown in Figure 4. It takes a source clock input and produces a pulse clock. It is possible to modify the pulse width of the produced pulse clock by using a NOT gate or by connecting the NOT gate. Latch receives the produced pulse clock. By connecting the pulse generator's output pulse clock to the latch, we can get the same results as a flip-flop.

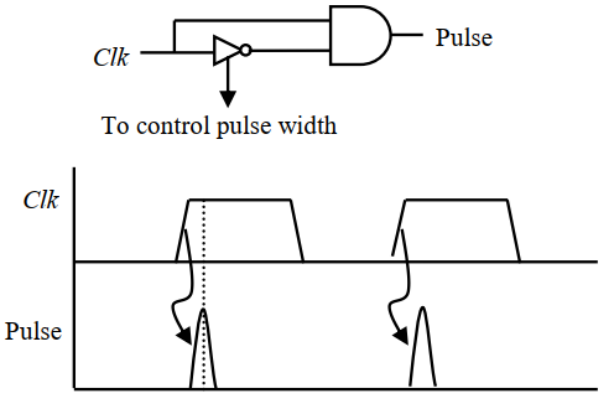

Fig 4. Pulse Producer and its waveform

The setup time of a pulsed latch is measured in clock cycles beginning with edge of the pulse clock, whereas the hold time is measured from the falling edge clock. This indicates that the pulsed latch follows a flip-flop-like timing paradigm. It doesn't matter if the flip-flop's latch is set up as a master or a slave; a pulsed latch will always remove one latch from each flip-flops is roughly double that of latches. Its timing analysis is made more difficult by the fact that it may borrow time and by the fact that non-overlapping clocking is used in the flip-flop. Furthermore, due to the length of time that data is held in a flip-flop, hold time violations are more likely to occur. While the timing model of pulsed latches can be simplified with a smaller pulse width and more time borrowing capacity. When compared to flip-flops, the sequencing overhead of pulsed latches is much smaller. As a result, a pulsed latch may be thought of as a quicker and more compact flip-flop with some of the benefits of both types of devices.

- **Area optimization:** When the tour areas are normalised using a latch, the areas of the latch clock pulsed circuit are 1 and correspondingly, allowing for straightforward optimisation of the aforementioned. The entire region expanded to (αA$\times$(k+1)+N+(1+1/k), the optimal (k= $\sqrt{N/\alpha a}$) for equation.

Where;

α- A constant or scaling factor that determines the entire area.
A- Circuit's initial area.
K- It seems to be a parameter that influences area optimisation.
N- Another parameter or variable.

- **Power optimization:** Latch and clocked/clock-pulse circuits account for the vast majority of power usage, hence power optimisation is quite comparable to area optimisation. Power is used to transfer data and load clocks into each latch. The power clock circuit is normalised when the powers are normalised using a latch.

C. Delayed pulsed clock generator

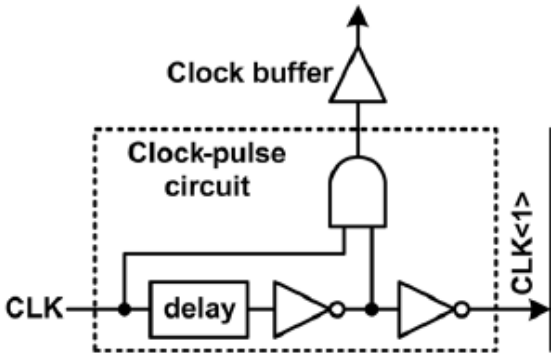

Fig 5. Delayed pulsed clock producer

- – Since each sharp pulsed clock signal in generator depicted in Figure 6 is formed from an AND gate and two late signals, the pulsed width may be less than the total of the rising and falling periods.
  – Since short pulsed clock signals are well-suited to the generator,
- **Decoder**

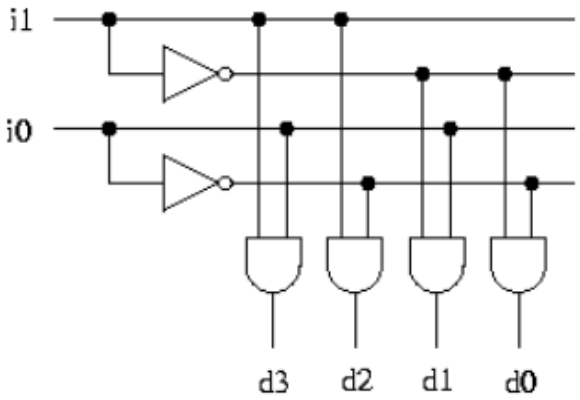

Fig 6. Decoder

- – As can be seen in Figure 6, a 1-of-n binary decoder has n output bits, with the "address" or bit number of the desired output bit being determined by the integer input bits.

- For each possible combination of input bit states, this sort of decoder either asserts one of its n output bits or none of them.
- When a certain integer value is fed into the inputs, just that matching output bit will be ”on”.

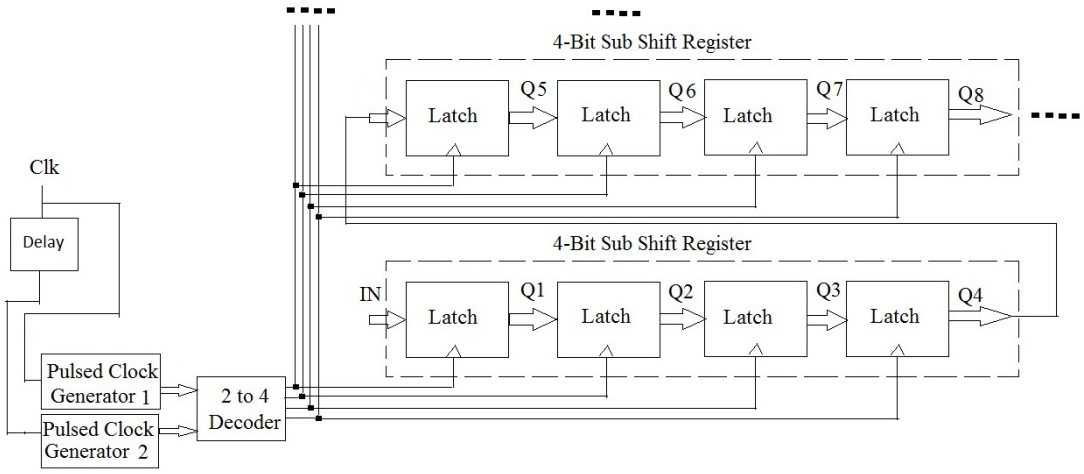

Fig 7. Proposed Method

3 Results and Discussion

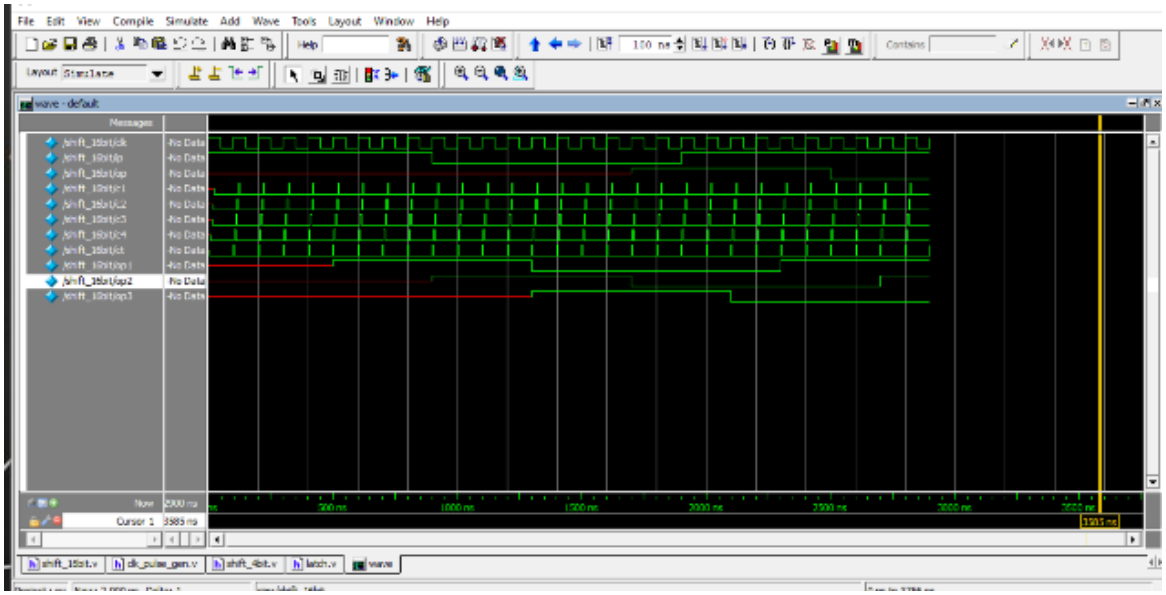

Fig 8. Output of 16- bit shift register with latch

The structure cycle significant pre-creation check stage. Due to the cost related with the manufacture step, exact check is critical to effective plan. The job of EDA device is to help structure and confirm a circuit's activity by numerically explaining the differential conditions portraying the circuit. These reproduction results permit circuit fashioners to check and adjust plans before submitting them for creation. Twofold edge activating implies that a flip-flop reaction for both positive (0 to 1 change) and negative (1 to 0) edges brings about cutting the recurrence of the clock by one half. In this paper the subsequent technique twofold edge activating is proposed to execute clock branch sharing-understood heartbeat (CBS_ip) conspire flip-failure and

make examination investigation with the current twofold edge activating flip-flops.

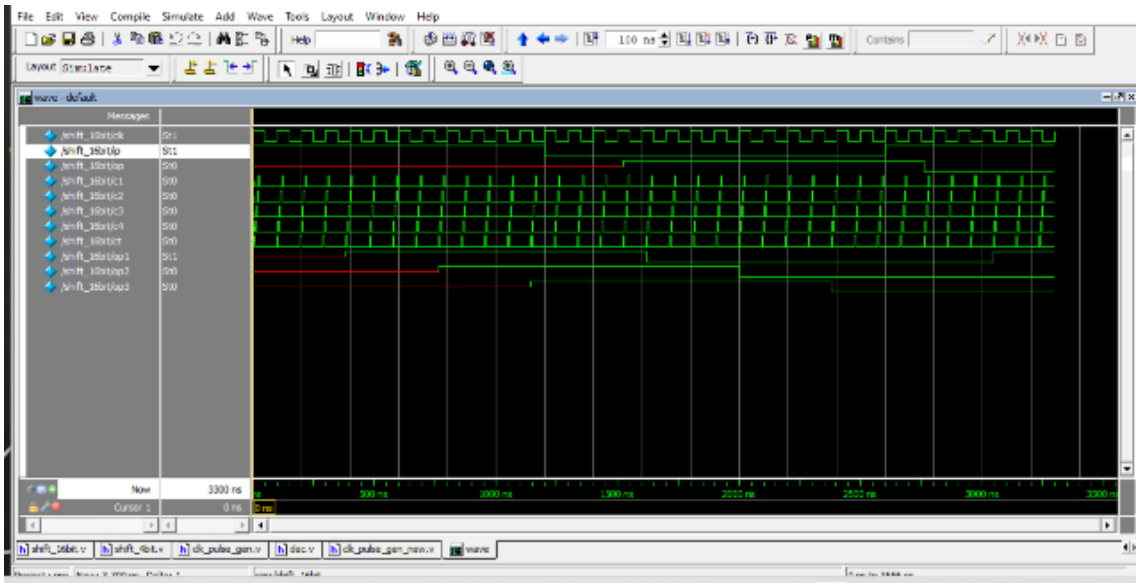

Fig 9. Proposed shift register with latch

The flip-flops (FF) in the proposed move register are organized using clock branch-sharing certain beat scheme (CBS_ip). The diverse existing twofold edge initiated flip-flops are transmission-entryway snare MUX, C2MOS Latch-MUX, Dual-edge transmission-passage beat lock (DE-TGPL). The essential part of the clock branch sharing arrangement is to diminish the amount of checked transistors in the structure as differentiated and existing two fold edge enacting flip-flops. When diverged from the other top tier twofold edge enacted flip-flop structures, this CBS_ip arrangement has an improvement in power usage and has less number of planned transistors and most insignificant power, it is sensible for tip top and low power circumstances.

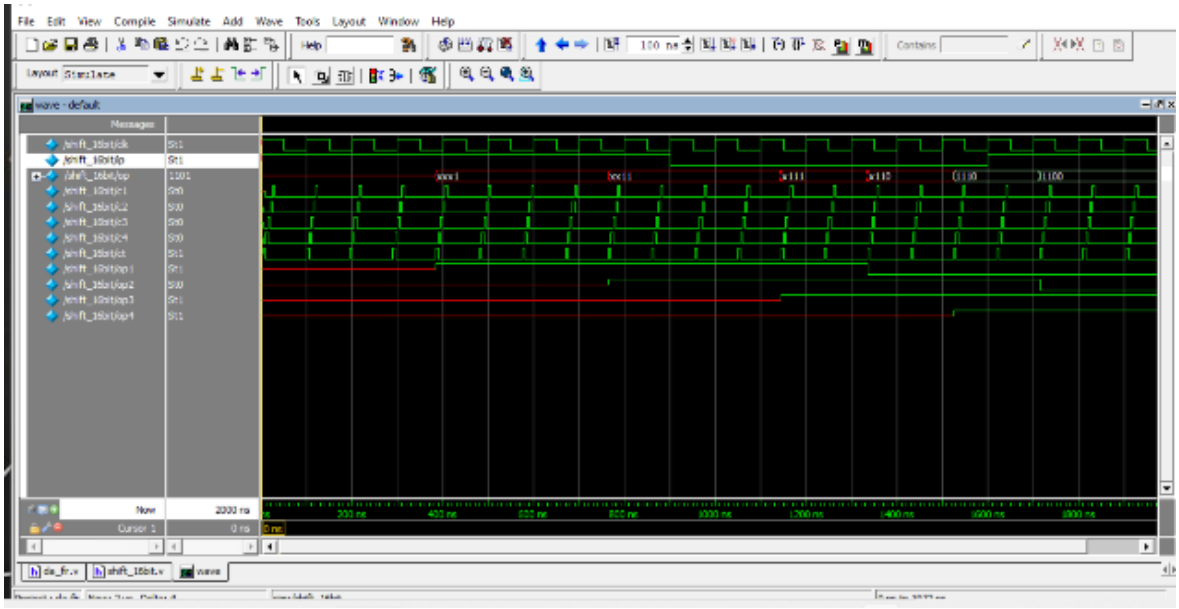

Fig 10. Projected shift register with latch and late circuits

The move register diminishes zone and power usage by superseding flip-flops with beat snares. The arranging issue between beat locks is settled using different non-spread delayed beat clock hails as opposed to a lone beat clock signal. Barely any the

Table 1. Shift register with different flip flop and latches

Parameters	shift register with flip flop	shift register with latches	Proposed shift register with pulsed latches
Average power consumption	19.02 μw	7.53 μw	0.502 μw
Static power	5.784mw	0.404mw	0.0269 mw
PDP	7.6nws	18.6nws	1.24 nws
Operating frequency	100MHz	100MHz	100MHz
Area of transistor	0.075 μw^2	0.031 μw^2	0.031 μw^2
Static currernt	3.261 μA	1.21 μA	0.080 μA

beat clock signals is used by sub shifter enlists and using extra temporary accumulating locks. In this paper, the zone capable move registers using flipflop and pulsed latches bases are organized and their ability is surveyed. In light of these structures the planning issue of the move registers is unravelled. Reproduction brings about 0.18-μm CMOS innovation affirmed that the region of the proposed move register is diminished around half and the force utilization is additionally decreased.

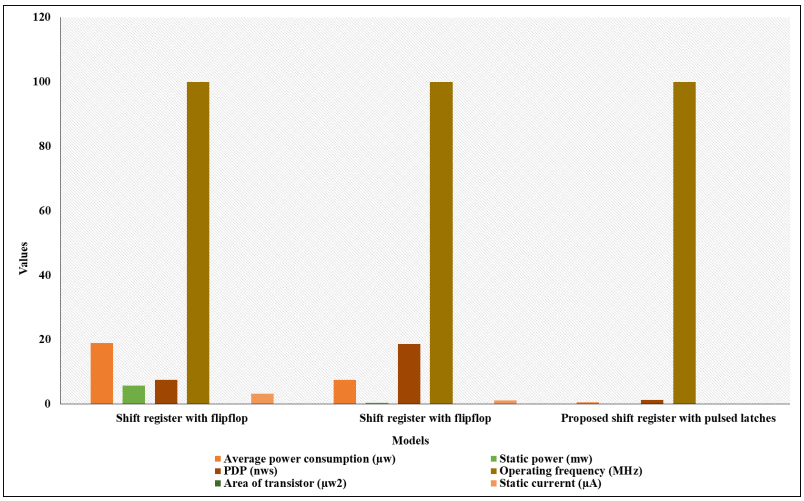

Fig 11. Comparison of simulation results of proposed shift register

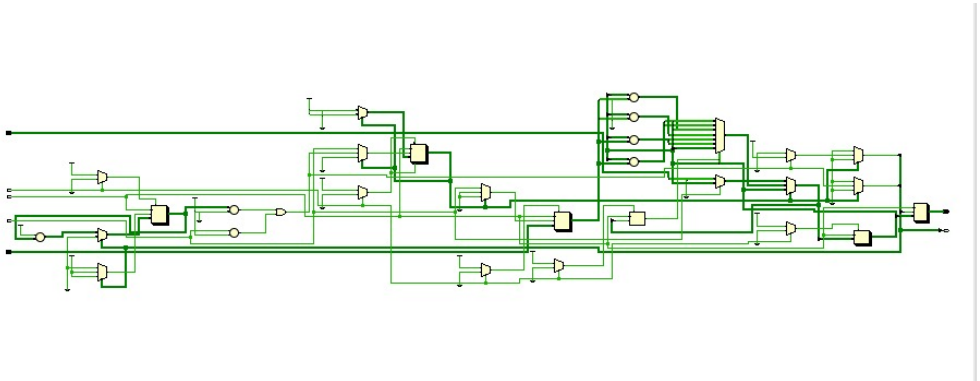

Fig 12. Proposed Model

In binary, the multiplier is 0b10001, or 17 in decimal from Figures 12 and 13. Because of the 'a' placeholder, the multiplicand is not fully specified. In order to obtain the product [35:0], Xilinx tool is used to simulate it if 'a' is also a binary digit (0 or 1). In digital logic design, the "reset" and "clock" signals are control signals that are typically used to clock or reset the system; however, in this context, they have no direct impact on the product calculation. If 'a' is a binary digit, could manually multiply

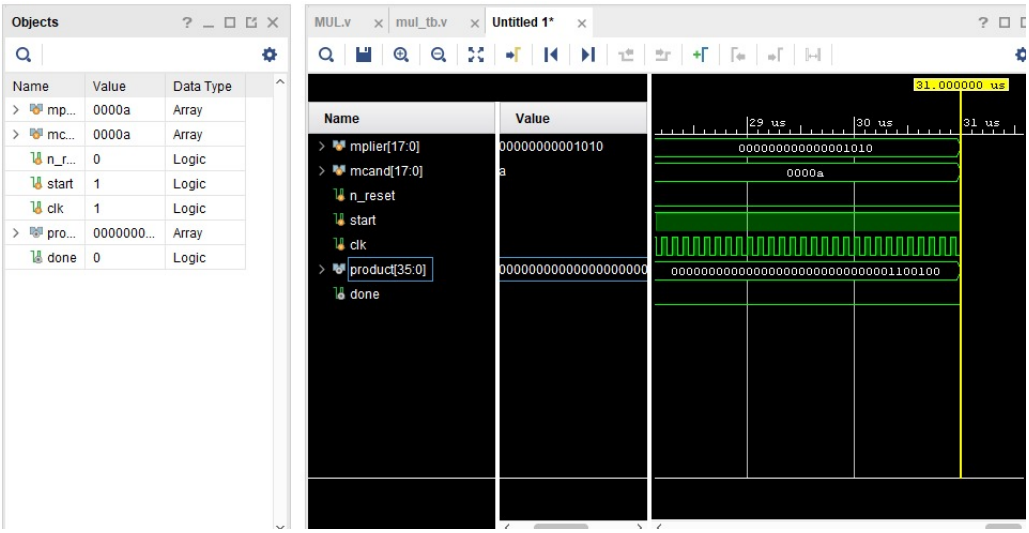

Fig 13. Proposed low power shift register

the number by following the steps of an algorithm for binary multipliers to get the result. With the multiplier and multiplicand values provided, can compute the product using simulation.

3.1 Existing models comparison results

Certainly, here's a table comparing the results of the Low-Power Shift Register Based on Pulsed Latch (LPSR-PL) with existing papers:

Table 2. Existing models comparison results

Parameters	(14)	(15)	(16)	Proposed model
Frequency (MHz)	250	250	-	100
PDP (fJ)	144.43	690.22	-	124
Power consumption (μw)	794	504	149	0.502

From Table 2 and Figure 14, frequency attained in reference[14] was 250MHz, Frequency attained in reference[15] was 250MHz and the proposed model had frequency of 100Hz. The measuring factor PDP in reference[14] was 144.43 fJ and in reference[15] PDP value is 690.22 fJ. The proposed model attains PDP value of 124. The power consumption in reference[14] is 794 μW, in reference[15] is 504 μW, in reference[16] is 149 μW and the proposed model consume 0.502 μW.

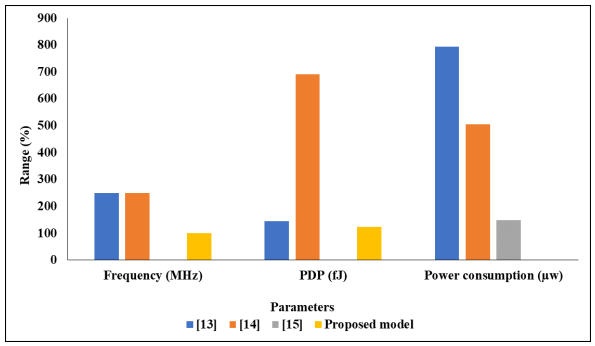

Fig 14. Comparison with existing models

4 Conclusion

Finally, designing energy-efficient digital circuitry remains a significant challenge in contemporary electronic design. This work introduces the Low-Power Shift Register Based on Pulsed Latch (LPSR-PL), a revolutionary solution to the hard issues of timing restrictions and power consumption related to shift registers. Traditional shift registers typically rely on a single pulsed clock signal for the organisation of data transmission, which commonly leads to timing mistakes and increased power usage. The LPSR-PL presented in this paper revolutionises this paradigm by utilising the concept of multiple non-overlapping signals. By dividing latches into including more temporary storage latches, this approach successfully addresses timing difficulties while consuming less power overall. Additionally, our design represents a significant leap in the simplification of the intricate clock-pulse circuitry by incorporating a Decoder-Enabled architecture. This streamlines the control logic and dramatically increases power efficiency. In order to lower the power overhead caused by switching transitions, this study presents the revolutionary Gated Clock Circuit. When subsequent data values are the same, this circuitry automatically ceases producing pointless pulses, dramatically lowering power consumption during idle or static data periods. Particularly for applications where energy conservation is of the utmost significance, such as portable devices and Internet of Things sensors, the envisioned LPSR-PL stands out as a particularly promising method to achieve low-power operation in shift registers. By combining non-overlapping clock signals, the decoder-enabled architecture, and the usage of gated clock circuits, this work demonstrates significant advancement in the ongoing search for low-power, high-performance shift register systems. In a time when energy-efficient and sustainable technology is crucial, the proposed LPSR-PL is at the forefront of innovation. It provides a viable way to advance digital circuitry and enable the smooth operation of many different devices while lessening their environmental impact. This study is a significant step towards the day when energy conservation and efficiency ideas are seamlessly incorporated into electronic design. With a much reduced power usage of 0.502μW, the suggested model outperforms other existing models. Future research will concentrate on tailoring the LPSR-PL for particular applications, evaluating cutting-edge materials and technologies for additional power savings, and researching adaptive clocking mechanisms for dynamic situations.

References

1) Wei Y, Wang D, Jiang S, Ma H, Yu J. A High-Voltage Serial-In-Parallel-Out Shift Register With Amorphous Silicon TFTs. *IEEE Journal of the Electron Devices Society*. 2023;11:416–420. Available from: https://doi.org/10.1109/JEDS.2023.3293232.
2) El-Razouk H. Novel Trace-Based Construction of the Parallel-In-Serial-Out Multiplication for Elliptic Curve Digital Signature Algorithm Like Binary Extension Fields. In: 2019 IEEE 9th Annual Computing and Communication Workshop and Conference (CCWC). IEEE. 2019;p. 955–0961. Available from: https://doi.org/10.1109/CCWC.2019.8666604.
3) Jeon S, Lee H, Kim HS, Kim Y. Universal Shift Register: QCA based Novel Technique for Memory Storage Modules. *Journal of VLSI circuits and systems*. 2023;5(02):15–21. Available from: https://www.vlsijournal.com/index.php/vlsi/article/view/67/83.
4) Cotrina G, Peinado A, Ortiz A. Gaussian pseudorandom number generator based on cyclic rotations of linear feedback shift registers. *Sensors*. 2020;20(7):1–18. Available from: https://doi.org/10.3390/s20072103.
5) Fujiwara H, Fujiwara K, Hosokawa T. Universal Testing for Linear Feed-Forward/Feedback Shift Registers. *IEICE Transactions on Information and Systems*. 2020;E103.D(5):1023–1030. Available from: https://doi.org/10.1587/transinf.2019EDP7205.
6) Thoutam LR, Alekya D, Triveni CC, Shruthi S, Varun K, Ajayan J. Design and Analysis of Low-Power High Performance 4-Bit Parallel Shift Register using Retentive True Single Phase Clocked D-Flip Flop. In: 2022 IEEE International Conference on Nanoelectronics, Nanophotonics, Nanomaterials, Nanobioscience & Nanotechnology (5NANO). IEEE. 2022;p. 1–5. Available from: https://doi.org/10.1109/5NANO53044.2022.9828902.
7) Tien N, Vozna M. High Speed And Reliable Double Edge Triggered D-Flip-Flop For Memory Applications. *Journal of VLSI Circuits and Systems*. 2019;1(1):13–17. Available from: https://doi.org/10.31838/jvcs/01.01.04.
8) Shin G, Lee E, Lee J, Lee Y, Lee Y. A Differential Flip-Flop With Static Contention-Free Characteristics in 28 nm for Low-Voltage, Low-Power Applications. *IEEE Journal of Solid-State Circuits*. 2023;58(5):1496–1504. Available from: https://doi.org/10.1109/JSSC.2022.3219091.
9) Soumya S, Ramesh KB. Pulsed Latch Technique Shift Registers for High Performance and Low Power Shift Registers. *Journal of Power Electronics and Devices*. 2022;8(1):24–34. Available from: https://matjournals.co.in/index.php/JOPED/article/view/243.
10) Authimuthu SB, Umadevi S, Andrushia AD. Low–power and High-speed Multi-operational Shift Register on Silicon Using Bi-enabled Pulsed Latch. *Silicon*. 2022;14(5):2373–2387. Available from: https://doi.org/10.1007/s12633-021-01517-2.
11) Kuo PY, Sheu MH, Tsai CM, Tsai MY, Lin JF. A Novel Cross-Latch Shift Register Scheme for Low Power Applications. *Applied Sciences*. 2021;11(1):1–11. Available from: https://doi.org/10.3390/app11010129.
12) Bhalghare S, Ramesh KB. Comparative study of shift register using flip flop and latches. *International Journal of Scientific Research in Engineering and Management*. 2022;06(02):1–4. Available from: https://ijsrem.com/download/comparative-study-of-shift-register-using-flip-flop-and-latches/.
13) Nidagundi JC, and V. Applications of Pulsed Latches and Bidirectional Pulsed Latches. *Advances and Applications in Mathematical Sciences*. 2022;21(12):7135–7143. Available from: https://www.mililink.com/upload/article/1567304475aams_vol_2112_october_2022_a41_p7135-7143_jayashree_c_nidagundi_and_vanishri_yandigeri.pdf.
14) Sharma N, Maurya VK. Analysis of High Performance & Low Power Shift Registers using Pulsed Latch Technique. *IJSRD - International Journal for Scientific Research & Development*. 2017;5(7):319–323. Available from: https://www.ijsrd.com/articles/IJSRDV5I70182.pdf.
15) Deenu K, Vaishnavi R, Sowntharya N, Keerthana M. Area Efficient and Low Power Shift Register Using Delay Circuits and Latch. *International Journal of Engineering Research & Technology*. 2023;12(04):399–403. Available from: https://www.ijert.org/research/area-efficient-and-low-power-shift-register-using-delay-circuits-and-latch-IJERTV12IS040219.pdf.

16) Kuo PY, Sheu MH, Tsai CM, Tsai MY, Lin JF. A Novel Cross-Latch Shift Register Scheme for Low Power Applications. *Applied Sciences*. 2021;11(1):1–11. Available from: https://doi.org/10.3390/app11010129.