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RESEARCH ARTICLE

# Transformer-less DC-DC Converter with Low Duty Ratio Using a Single Switch and Quasi Impedance Based Network

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## Abstract

**Objective:** Transformer-less DC-DC converter suitable for low-power applications, with a high voltage gain. With fewer elements, this suggested converter may generate a higher gain voltage at a lower duty ratio. **Method:** A transformer-less quasi-Z-source DC-DC converter with gain is introduced and examined. To boost the load voltage, the topology makes use of both the switched capacitor and active switched-inductor structure based on the quasi-Z-impedance network. The theoretical outcomes and the converter's functionality are verified by the simulation, which is run using the PLECS software program. **Findings:** The benefits of the conventional Z-source boost converter, including fewer voltage stress, constant input current, and common ground, are still present in the suggested converter. Additionally, at a relative duty ratio of 0.3, the gain is greatly increased by around 10 times. Each power switch's voltage stress is also significantly decreased. A detailed discussion is held on the steady-state operation. **Novelty:** A novel architecture with higher voltage gain at a decreased duty ratio is presented in this work. The network of inductors and capacitors typically used to raise the dc-dc converter's output voltage. The suggested topology raises the output voltage by using just one switch and switched capacitor and switched inductor network.

**Keywords:** Transformerless converter; duty cycle; voltage gain; common ground; single switch

## 1 Introduction

High-gain converters are becoming popular and necessary for electronics applications in green energy. It has high efficiency, and reliability requiring systems like standalone solar panels and fuel cells to have their low output voltages increased to 200–400 V [(1)]. High voltage gain has been produced with the help of some boost dc-dc topologies, which fall into two groups: transformer based and transformer-less based circuits. By raising the turn ratio of the transformer, a frequency transformer is utilized to enhance the output voltage gain for the isolated [(2)]. High voltage stress across components, conduction loss at high duty cycle, and low output voltage characterize non-isolated Traditional Boost converters (TBC). A reverse recovery issue arises when the voltage

gain is significant. It is inexpensive, compact, and simple to operate. These converters are characterized by a high power density, better transient responsiveness, less switch stress, higher voltage gain, and enhanced efficiency[3]. Moreover, a Z source converter is utilized to increase the voltage gain at a fixed duty ratio of 0.5. This layout reduces voltage stress between components, which increases efficiency. A converter based on quasi-Z-source (qZS) has been designed[4]. With a duty ratio of D, the voltage gain may be increased to 1/(1-2D) in comparison to the traditional boost converter (TBC). The lower duty cycle for better voltage gain, which minimizes the inductor's current ripple, allows for lower power ratings for inductors, diodes, and capacitors.

The qZS-based converters are better suited for PV applications because of these qualities. This voltage gain is still not optimal when greater output voltages are needed, though. As a result, many topologies, such as switched inductors have been developed that combine the qZS network[5]. Numerous components are used in the converter that was developed using the Z-source and quasi-Z-source concepts. This allows it to achieve the necessary voltage gain with a lower initial inrush current. Nevertheless, the power losses are greater than with other converters because of the many components[6]. A switched inductor cell that has been changed can assist in attaining high gain while reducing the voltage stress on each switch. Two operating modes exist for the converter: CCM and DCM. Dual switches are present in the converter. Furthermore, the converter may be employed in a variety of devices due to its constant input current. At both switches, the same control is used. The converter contains a large number of components, which is its only drawback[7]. With less voltage between the components, voltage multiplier cells allow for four times the voltage gain of a TBC. It is made with relatively few components and is simplistic in design. Continuous input current is required for applications involving renewable energy. Additionally, $V_o/2$ represents the percentage of voltage stress on the switches[8]. There is a discussion about a buck-boost dc-dc converter with continuous input current. With only one switch and less voltage stress on semiconductor components, it offers a larger voltage gain than a conventional converter. It is simple to direct a single switch. Because the input current is constant, filtering is not necessary. This converter achieves a high voltage gain[9]. With common ground, the more effective quasi-Z-source series dc-dc converter is created to boost the voltage level[10]. With a voltage-at-duty ratio of 0.3 six times, the architecture that is being shown results in lower voltage stress and better efficiency. With three inductors that complicate the circuit, it runs in DCM mode. It has more components as a result[11–15]. This article describes in detail an innovative single-switch common ground quasi-Z source DC-DC converter that may work in continuous conduction mode. Compared with the traditional converter, the suggested converter has a larger voltage gain of 1/1-3D. There is just one power switch utilized, and it is simple to operate. As such, it can find applications in several other fields in addition to renewable energy applications.

## 2 Proposed Converter

### 2.1 Topology Detail

The presented topology is depicted in Figure 1 with a single power switch(S), three inductors specified as ($L_1$, $L_2$, and $L_3$), three diodes named ($D_1$, $D_2$, and $D_3$) and five capacitors including $C_o$ acts as output filter with the resistive load R. By using inductors and capacitors, voltage step-up cells are made to enhance the voltage gain of the circuit with high switching frequency $f_s$. To improve performance, it is thought that assumptions should be followed.

1. Lossless components.
2. Sufficient capacitance and inductance for analysis.
3. Constant voltage across all of the capacitors.

### 2.2 Mode 1 ($t_o$-$t_1$): (When S=1)

Switch(S) is turned ON. Diodes.$D_1$, $D_2$, and $D_3$ are in reverse bias. In this period, the inductor current rises linearly and stores the energy in magnetic form, and capacitors discharge through the inductors ($L_1$, $L_2$, and $L_3$) and load separately. Applying KVL in Figure 2.

$$\begin{cases} V_{L1} = V_{in} + V_{C2} \\ V_{L2} = V_{in} + V_{C1} + V_{C3} \\ V_{L3} = V_{in} + V_{C4} \end{cases} \quad (1)$$

$$V_{Co} = V_o \quad (2)$$

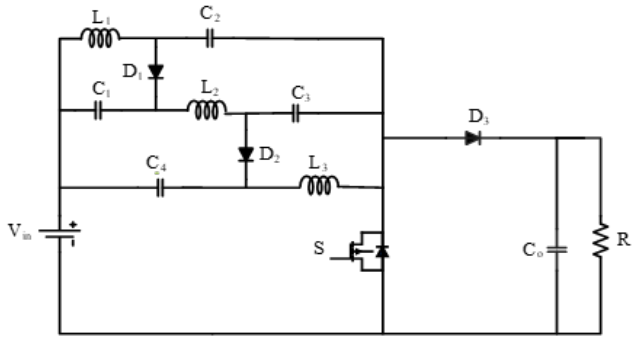


**Fig 1. Proposed Converter**

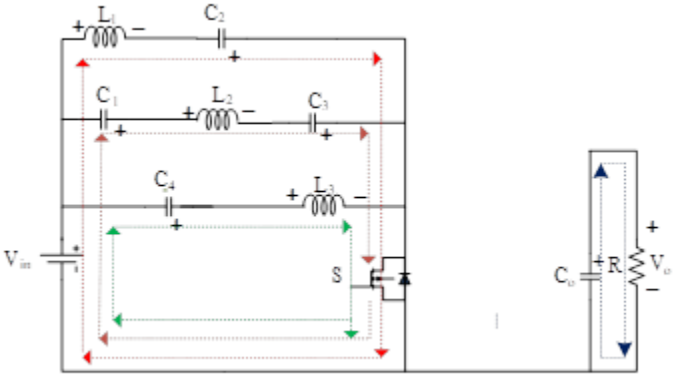


**Fig 2. Mode 1(When S=1)**

## 2.3 Mode 2($t_1$-t2): (When S=0)

When Switch is turned OFF, Diodes $D_1$, $D_2$, and $D_3$ are in forward bias. Capacitors are charged by the demagnetization of the inductors. Applying KVL in Figure 2,

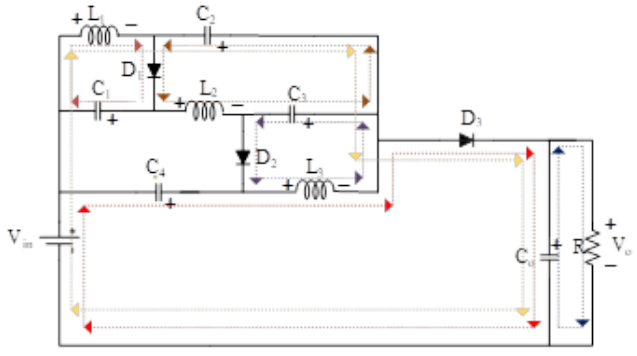


**Fig 3. Mode 2 (When S=0)**

$$\begin{cases} V_{L1} = -V_{C1} \\ V_{L2} = V_{C3} - V_{C2} \\ V_{L3} = -V_{C3} \end{cases} \tag{3}$$

$$\begin{cases} V_{in} + V_{C4} + V_{C3} = V_o \\ V_{in} + V_{C1} + V_{C2} = V_o \end{cases} \tag{4}$$

In steady state, volt-sec balance on the inductors $L_1$, $L_2$ and $L_3$

$$\begin{cases} \int_0^T V_{L1}(t).dt = 0 \\ (V_{in} + V_{C2}) \times DT + (-V_{C1}) \times (1-D)T = 0 \\ V_{C1} = \dfrac{D(V_{in} + V_{C2})}{(1-D)} \end{cases} \tag{5}$$

$$\begin{cases} \int_0^T V_{L2}(t).dt = 0 \\ (V_{in} + V_{C1} + V_{C3}) \times DT + (V_{C3} - V_{C2}) \times (1-D)T = 0 \\ D(V_{in} + V_{C1}) - (1-D)\, V_{C2} + V_{C3} = 0 \end{cases} \tag{6}$$

$$\begin{cases} \int_0^T V_{L3}(t).dt = 0 \\ (V_{in} + V_{C4}) \times DT + (-V_{C3}) \times (1-D)T = 0 \\ D(V_{in} + V_{C4}) + DV_{C3} = V_{C3} \end{cases} \tag{7}$$

From Equations (4) and (7)

$$V_{C1} = V_{C3} = DV_o \tag{8}$$

From Equations (4) and (5)

$$V_{C4} = V_{C2} = V_o(1-D) - V_{in} \tag{9}$$

From Equations (6), (7), (8) and (9)

$V_{C1} = V_{C3}$ and $V_{C4} = V_{C2}$

By Using Equations (6), (7) and (9). To find the voltage gain

$$\begin{cases} D(V_{in} + DV_o) - (1-D)^2\, V_o + (1-D)V_{in} + DV_o = 0 \\ V_{in} + D^2\, V_o + DV_o - (1-D)^2\, V_o = 0 \\ V_{in}\, [D^2 + D - (1-D)^2] V_o\, V_{in}\, 0 \end{cases}$$

$$M_{CCM} = \frac{V_o}{V_{in}} = \frac{1}{1-3D}$$

## 2.4 Stresses of power devices

The voltage that appears on the switch and other components while those specific components are off is indicated by the stress on the switch and other components. The voltage stress across switch $S_1$ and all of the diodes $D_1$, $D_2$, and $D_3$.

$$\begin{cases} V_s = \dfrac{V_{in}}{1-3D} \\ V_{D3} = V_{D2} = V_{D1} = \dfrac{V_{in}}{1-3D} \end{cases} \tag{10}$$

Inductor current can be calculated using the following formula based on the charge balancing concept of capacitor Co: Equation (3) and Figure 3 are used to investigate the idea that,

$$I_{D3} = I_o$$

$$\begin{cases} I_s = \dfrac{3D}{1-3D} I_o \\ I_{D2} = I_{D1} = I_{L3} = I_{L2} = I_{L1} = \dfrac{I_o}{(1-3D)} \end{cases} \tag{11}$$

## 2.5 Power Loss and Efficiency Analysis

Conduction losses are computed without accounting for switching losses, based on the assumption that the inductor's currents are ripple-free. Resistance $r_{L1,}$ $r_{L2}$ and $r_{L3}$ of inductors $L_1$, $L_2$ and $L_3$. Additionally, $r_{S1}$ represents the MOSFET on-resistance. Power loss equations given,

$$i_{L1_{rms}} = i_{L2_{rms}} = i_{L3_{rms}} = \sqrt{\frac{\int_0^T i_L(t)^2}{T}\, dt} \approx \frac{I_O}{1-3D}$$

$$P_{L_1} = i^2{}_{L1_{rms}} r_{L1} \tag{12}$$

$$i_{S_{rms}} = \sqrt{\frac{\int_0^T i_s(t)^2}{T}\, dt} \approx \frac{1}{(1-3D)\sqrt{D}} I_O$$

$$P_{S_{conduction\ loss}} = i^2{}_{S_{rms}} r_s \tag{13}$$

Efficiency of the topology can be expressed as,

$$\eta = \frac{P_O}{P_O + P_{L_{total,\ loss}} + P_{C_{loss,\ total}} + P_{S_{loss,total}} + P_{D_{loss.total}}} \tag{14}$$

## 2.6 Comparison Table

A summary of the proposed converter's total components compared to those of various existing converters is given in Table 1. Table 1 expresses that all of the converters' voltage gains are lower than the suggested converter's. However, the merits of the suggested converter are its relative duty ratio (0.3) and constant input current. Compared to TBC and Z-source converters, the suggested converter has more components.

The number of components in converters[7] and[9] is greater than that of other converters. Since every converter has continuous input current and common ground, it is possible to use it for applications using renewable energy. Due to the four inductors and dual switch, Topology[7] is a complex circuit. Comparing the voltage gain of the proposed converter to converters TBC and Z-source, it is higher[7], [8], [9], and[10].

Figure 4 shows a graph that compares the voltage gain and duty ratio of the suggested topology to those of existing converters, such as TBC and Z-source[7], [8], [9], and[10]. It is evident that the presented topology outperforms all existing topologies in terms of voltage gain at extremely low duty ratios.

**Table 1. Comparison with recent topologies and proposed topology**

| Converters | TBC | Z-Source | (7) | (8) | (9) | (10) | Proposed |
|---|---|---|---|---|---|---|---|
| **Switch Count (Sc)** | 1 | 1 | 2 | 1 | 1 | 1 | 1 |
| **Inductor Count (Lc)** | 1 | 2 | 4 | 2 | 4 | 3 | 3 |
| **Capacitor Count (Cc)** | 1 | 3 | 3 | 4 | 6 | 7 | 4 |
| **Diode Count (Dc)** | 1 | 2 | 7 | 5 | 3 | 5 | 3 |
| **Total Components** | 4 | 8 | 16 | 12 | 14 | 16 | 11 |
| **Gain($V_o/V_{in}$)** | $\frac{1}{1-D}$ | $\frac{1}{1-2D}$ | $\frac{3+D}{1-D}$ | $\frac{4}{1-D}$ | $\frac{3D}{1-D}$ | $\frac{2+D}{1-2D}$ | $\frac{1}{1-3D}$ |
| **Gain (G) at 0.3** | 1.4 | 2.5 | 4.7 | 6 | 1.3 | 6 | 10 |
| **Voltage Stress (Vs/Vin)** | $\frac{1}{1-D}$ | $\frac{1}{1-2D}$ | $S_1=\frac{2}{3+D}$ $S_2=\frac{1+D}{3+D}$ | $\frac{2}{1-D}$ | $\frac{1}{D}$ | $\frac{1}{1-2D}$ | $\frac{1}{1-3D}$ |
| **Duty Cycle Limit** | 1 | 0.5 | 1 | 1 | 1 | 0.5 | 0.33 |
| **Input Current** | Continuous | Continuous | Continuous | Continuous | Continuous | Continuous | Continuous |
| **Common Ground** | Yes | Yes | Yes | Yes | Yes | Yes | Yes |

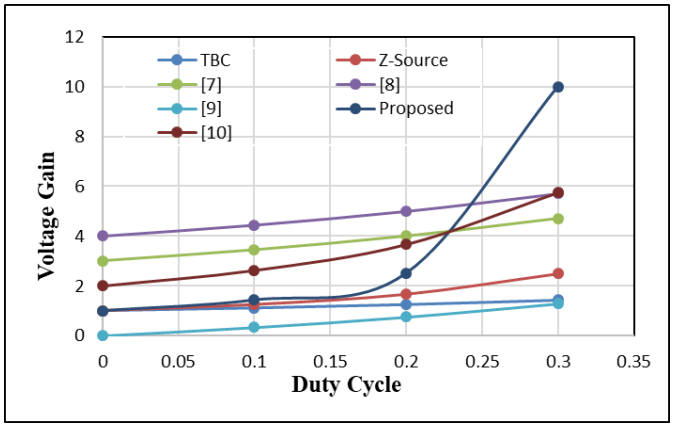


**Fig 4. Voltage gain v/s Duty cycle**

# 3 Results and Discussion

## 3.1 Simulation Results

The PLECS software simulation results are displayed in the below figures. The simulation's output was obtained at a duty ratio of 30%, feeding a resistive load of 400 ohm at a switching frequency of 50 kHz with a source voltage of $V_{in}$ = 12V. Using the above formulas, 150 mF of capacitance was chosen for the capacitors and 1mH of inductance for the inductors. The inductor currents with gate pulses are displayed in Figure 5. Inductor currents $I_{L1}$, $I_{L2}$, and $I_{L3}$ have average values of 6A, 6A, and 6.2A, respectively. The voltage of the capacitor is displayed in Figure 6. The capacitor voltages Vc2 and Vc3 are the same, measuring 36 volts, and the capacitor voltages Vc1 and Vc4 are identical, or about 72 volts. The gate pulse and diode voltages are shown in Figure 7. For every diode, there is an identical voltage of 118 volts across them.

The simulated $V_o$, $V_{in}$, and $V_{gs}$ waveforms at a 30% duty ratio are shown in Figure 8. It is observed that for an input voltage of $V_{in}$ = 12V, the suggested converter delivers an output voltage of $V_o$ about 119V. Voltage gain is around ten times the duty ratio of 0.3. Because of the voltage drop between switches, diodes, capacitors, and inductors, the voltage gain will actually be decreased. Input and output currents of the converter are presented in Figure 9. The output current is 0.3 A, whereas the input

current is roughly 10 A. when the resistive load fluctuates or the input voltage change. Under load and input voltage variations, the suggested converter's performance can vary.

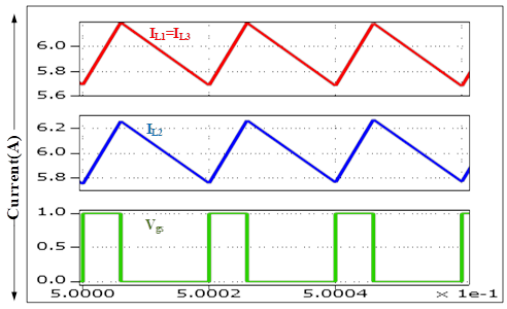


**Fig 5. Simulated waveform of Inductor currents witha gate signal**

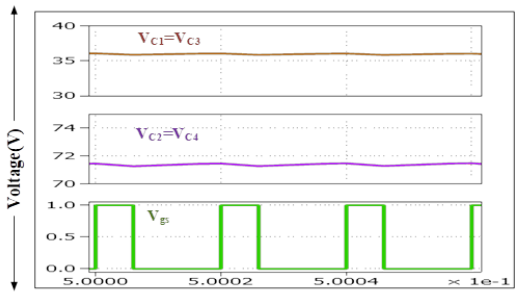


**Fig 6. Simulated waveform of capacitor Voltages with gate signal**

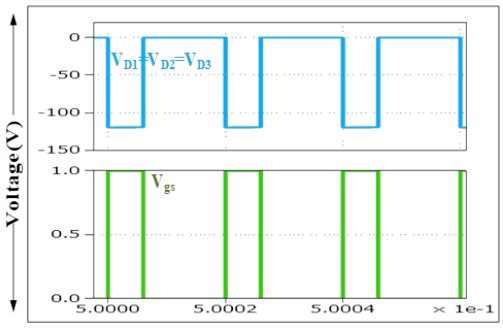


**Fig 7. Simulated waveform of diode voltages with gate signal**

## 3.2 Hardware Results

The simulation parameters addressed in the section above are similar to the same hardware parameters. The suggested hardware prototype's CCM mode operation requires a DC input source of 12 V. For the power MOSFET, the experimental gate pulse is 30%. Within the experimental waveforms, Figure 10 depicts the input voltages ($V_{in}$) and input currents ($I_{in}$). The gate drive signal, shown by Vgs in Figure 11, gives an output voltage ($V_o$) of 115 volts and an output current ($I_o$) of 0.3. Because of component losses, hardware results differ from simulation findings exactly.

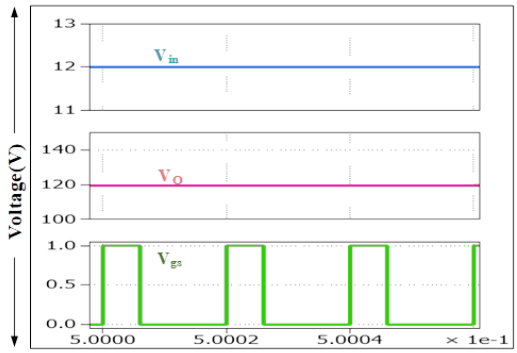


**Fig 8. Simulated waveform of source voltage and Generated voltage witha gate signal**

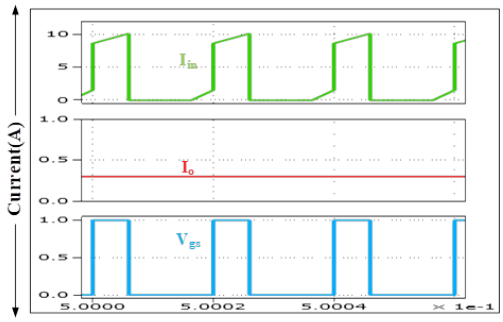


**Fig 9. Simulated waveform of source current and load current with a gate signal**

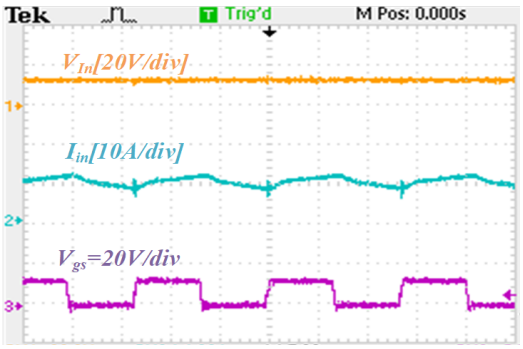


**Fig 10. Experimental waveforms ofInput voltage ($V_{in}$) and input current ($I_{in}$) with gate pulse (Vgs)**

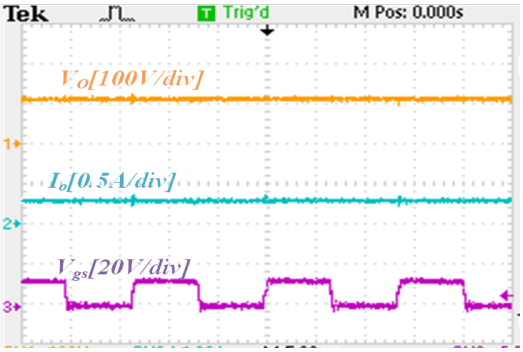


**Fig 11. Experimental waveforms of Output voltage ($V_o$) and Output current ($I_o$) with gate pulse (Vgs)**

## 4 Conclusion

A transformer-less DC-DC converter using a single switch and a quasi-impedance network has been suggested. It is possible to produce high voltage with a relatively low duty cycle of 0.3. The steady-state discussion of CCM has been done. Simulation and experimental results have also been discussed. It is appropriate for renewable energy applications because of the continuous input current. Comparisons between the proposed converter and existing converters have been made regarding its voltage gain, voltage stress of the primary switch, total components, and other criteria. In this research, the findings that were also simulated on PLECS are also presented. The high voltage stress on the switch and diodes, among other components, is the disadvantage of this design. The output voltage and the voltage stress across the switch are the same. The value of the input current ripple of the proposed converter is 10.17A.

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