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Design and Development of FPGA Based Image Acquisition System

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Abstract

Background/Objective: This article presents an image acquisition system which consists of two important elements, namely a CMOS sensor and an FPGA. **Method:** In this article, the domain under observation is incessantly supervised by capturing the video of the area. This is successfully completed with the help of the CMOS sensor, through which the image frames are captured. Pixel data interface and CMOS senor are connected to the FPGA through the I2C bus. VGA Controller module in the FPGA will read the pixel data from one of the ports of DDR SDRAM and it can display the video on LCD monitor. FPGA used in the present work is Cyclone II, which is manufactured by ALTERA. Quartus II 13.0 suite is used for software development. FPGA will be programmed with the help of Verilog HDL. **Findings:** The mode register of the CMOS sensor is programmed with I2C protocol, so that CMOS settings like resolution, exposure are configured with this protocol. ALTERA DE2 board consists of SDRAM, which can store the captured image frames. This system consists of the black and white converter module so that the black and white images only stored in the data. VGA Controller module in the FPGA always reads the pixel data from one of the ports of DDR SDRAM and it generates the required signals to display the video on the monitor.

Keywords: CMOS Sensor, FPGA, SDRAM, VGA Controller

1. Introduction

Now a day's advances in FPGA technology have impressively increased the use of FPGAs for computer vision applications[1]. With the help of advanced versions of FPGAs, one can get both software programmable processor and hardware computing resources on the same IC[2]. The hardware is enforced on the sufficient logic blocks of the chip. To implement the application software, these ICs are also having an additional integrated processor with the system software[3]. In the case of signal processing and image processing area, FPGA-based embedded systems importance is increasing a lot[4]. In that, smart cameras for image processing using intelligent embedded systems have faith on FPGA-based architectures[5,6]. On the end, the most crucial rewards of the FPGA is the facility to effort the in-house parallel existence of many sight algorithms[7,8]. The persona of FPGA in embedded systems is acquiring importance referable to its increasing potentialities and handiness of mighty EDA tools[9,10]. A number of available sources in today's FPGAs is rather high and can practically deal numerous suing operations. FPGA could instantly operate the data coming from the sensor or any acquisition device[11].

Presently, for the execution of software algorithms, FPGA technology becomes an alternative. The radically

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distinctive architecture of the FPGA has permitted the technology to be used in number of applications like close observation of a person or group (usually by the police) by capturing video and medical imaging etc. FPGA belongs to a VLSI circuit which can be re-programmed in a number of times[12,13]. The word "field programmable" concerns the ability to change the performance of the device. The word gate array pertains to the basic internal structure which allows re-programming[14]. In general, image processing algorithms are enforced with the help of DSPs and ASICs[15]. The diligent use of FPGAs in the field of image processing and video processing has a great regard. This is because of the collimated and superior computational compactness of FPGA as likened to a general-purpose microprocessor[16]. Images and videos are captured by CMOS sensor and it can commute them into digital format, procedures and produces gumption of the information that it accepts in a period of time[17]. The block diagram of the FPGA-based image acquisition system is shown in Figure1.

2. Software Specifications

2.1 Quartus II

Quartus II software allows productivity enhancements resulting in faster simulation, faster board bring-up, and faster timing closure. The Quartus II Design Suite is developed by the ALTERA Company. This software is being used with different ALTERA family FPGAs/CPLDs like MAX, Stratix, Apex II, and Flex 10K, Cyclone etc. In the present work Quartus II software (Version 13.0) is used to program the EP2C35F672C6 which is basically a Cyclone II FPGA.

2.2 I2C protocol

Inter Integrated Circuit bus can be written in a short form as I2C. This can also be represented as IIC and I²C, which is a consecutive and co-occurrent bus protocol. How the data is processed through the I2C bus is clearly characterized by the fabricator of the I2C chips. Generally I2C system can have one master and few slaves, but the master can produce the clock pulse. The master also specifies at what time communication likely to take place. For bus timing, it is significant that the obtuse slave should, however, be capable of following the master's clock. Alternatively, one can say that, the bus is as quick as the lazy slave.

3. Hardware Specifications

3.1 CMOS Image Sensor

The CMOS image sensor used in the present work is MT9M011, which is one third inch active-pixel digital image sensor with a resolution of 1280Hx1024V. Advanced camera operations are integrated on CMOS chip, which includes snapshot mode, windowing, column and row skip mode. It will consume very low power and with the help of mere two-wire serial interface it can be programmed[18]. The quality of captured pictures by CMOS is almost achieved CCD picture quality; although asserting the built-in size, cost and consolidation advantages of CMOS[19]. The user can program the sensor for advanced

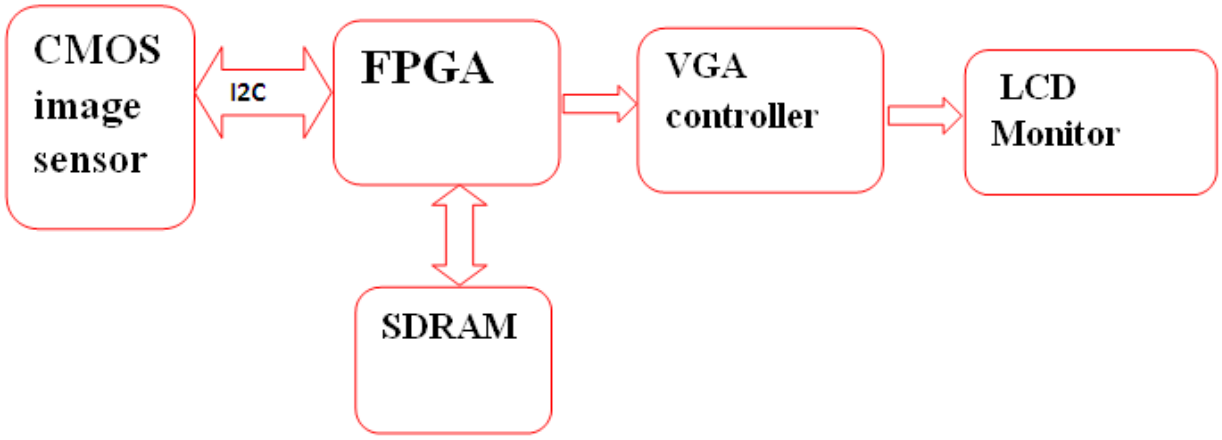

Figure 1. Block diagram of FPGA based image acquisition system.

setting, exposure and frame size for different parameters. 13.9 FPS (Frames Per Second) is the default mode outputs of an SXGA image. The operating temperature range of CMOS sensor is from -30^{0}C to +70^{0}C. It requires low supply voltage: 2.8V ±0.3V. Its power consumption will be very low and is ideal for battery operated devices. This CMOS sensor will produce direct digital output because its associated circuit is incorporated with ADC. The photograph of the CMOS sensor with internal ADC circuit is shown in Figure 2. The construction of CMOS camera is shown in Figure 3. The block diagram of CMOS camera with ADC circuit is shown in Figure 4.

Figure 2. CMOS sensor with ADC.

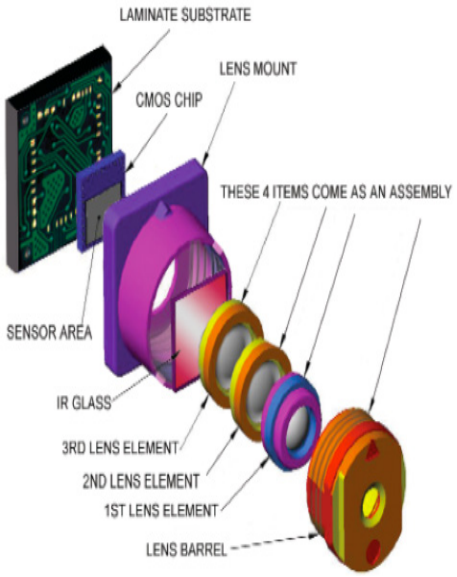

Figure 3. Construction of CMOS camera.

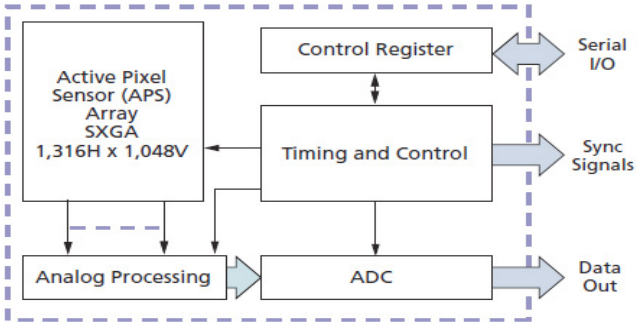

Figure 4. Block diagram of CMOS camera with ADC circuit.

3.2 SDRAM (Synchronous Dynamic RAM) IS42S16400

SDRAM is nothing but a DRAM that has a concurrent interface. Conventionally, for every change in control inputs DRAM can react as speedily as possible, so that it has an asynchronous interface. Before reacting to control inputs, SDRAM can wait for a clock signal and therefore it is contemporized with the PC's system bus so that it has a synchronous interface. In order to pipeline the incoming instructions, the clock should drive an internal finite state machine. This permits the chip to have a more complex pattern of performance than an asynchronous DRAM[20].

3.3 FPGA (Field Programmable Gate Array)

The immensely successful low-cost FPGA Cyclone II broadens the density range to 68,416 LEs and it has 622 usable input/output pins. It is also having 1.1 megabits of inbuilt memory[21]. Cyclone II FPGAs are fabricated on 300-mm wafers to assure rapid accessibility and affordability. As Cyclone II devices are using less silicon area, at a cost of ASICs itself they can endorse composite digital systems on a single chip[22]. The affordable price and optimized characteristic set of Cyclone II FPGAs nominate them perfect choice for an extensive range of video processing, automotive supplies, communications, test & measurement, goods & services, and other commercial applications. The FPGA used in the present work is Cyclone II EP2C35F672C6.

3.4 Altera DE2 Board

ALTERA DE2 package includes the following important features. It consists of an FPGA namely Cyclone II 2C35F672C6 device with 35,000 LEs, 16MB Serial Configuration device for AS mode. For programming and user API control it is having in-built USB blaster. It also

has TV decoder for NTSC/PAL/Multi-format systems, 24-bit CD-quality audio CODEC. It will support two programming modes namely JTAG and AS. DE2 board also consists VGA DAC with VGA-out connector which can support up to 1600x1200 at 100 Hz rate, Ethernet 100/10Mbps, SRAM, 8MB SDRAM, 4MB Flash memory, SD card connector, RS232, 16x2 LCD panel, 4 pushbutton switches, 18 toggle switches etc. The DE2 board also has software endorse for standard input/output ports and a control panel feature for accessing several elements. In order to supply utmost tractability for the user, all the connections are established through the Cyclone II FPGA[23]. The photograph of the Alter DE2 board with CMOS camera is shown in Figure 5.

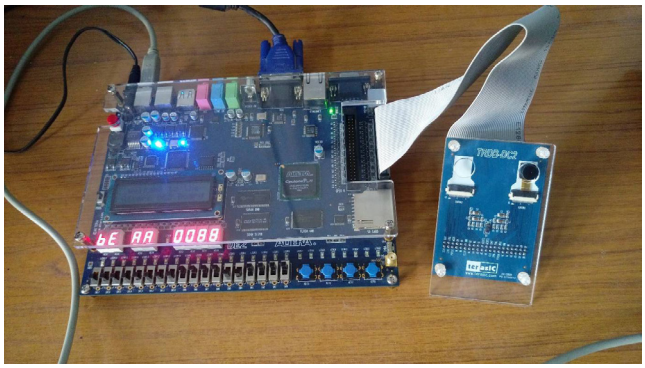

Figure 5. Altera DE2 board with CMOS camera.

3.5 VGA (Video Graphics Array)

VGA is denoted as an "array" rather than "adapter" since it was enforced from the start as a single chip, substituting the Motorola 6845 and lots of distinct logic ICs that occupied the full-length ISA boards of the MDA, CGA, and EGA. Its single-chip execution also permitted the VGA to be located instantly on a computer's CPU board with a minimum of difficulty (it need only three things, they are timing crystals, video memory, and an external RAMDAC).

4. Results and Discussions

In this article, the domain under observation is incessantly supervised by capturing the video of the area. With the help of the CMOS sensor, the capturing of video under observation is successfully completed. This CMOS sensor will produce direct digital output because its associated circuit is incorporated with ADC. The mode register of the CMOS sensor is programmed with I2C protocol, so that CMOS settings like resolution, exposure are configured with this protocol. The serial data is assigned to the CMOS sensor which is obtained from the available parallel data. The data is ceaselessly captured by the programmed sensor. CMOS sensor's I2C interface and Pixel Data interface are connected to the FPGA through GPIO interface of the DE2 Board. FPGA will have I2C Slave controller module that will write the CMOS sensor configurable register values. In order to restrain the stream of data coming from the sensor which is programmed to the memory, the IDFC (Image Data Flow Controller) is used. This IDFC influences the stream of data to the memory. Whenever the START signal is triggered then only the data is stored in the memory. It happens continuously until STOP signal is found. This system consists of the black and white converter module so that the data is laid-in in the pattern of black and white images only. ALTERA DE2 board consists of SDRAM, which can store the captured image frames. Two frames can lay in the memory at a time. Therefore, it is split into two and the data is read from or written into the memory. SDRAM controller is used to supervising these performances. The read & write signals are rendered by SDRAM controller and it can also track which frame is being read or written. The video can be monitored on a visual display unit such as an LCD monitor. For this purpose, the VGA controller is used.VGA Controller module in the FPGA always reads the pixel data from one of the ports of DDR SDRAM and it generates the required signals to display the video on the screen.Figure 6 shows real-time video capturing and displaying on the monitor through CMOS camera connected with ALTERA DE2 board.

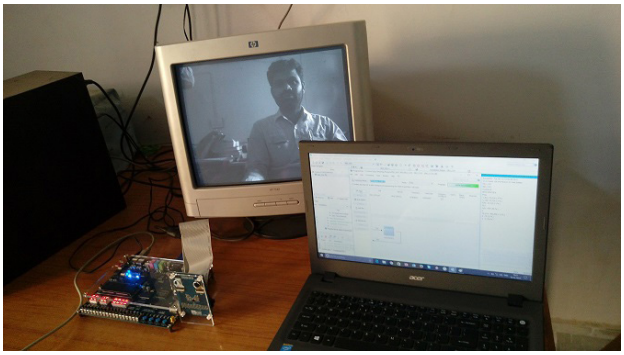

Figure 6. Photograph of the image acquisition system.

5. Conclusion

The CMOS camera interface unit is developed for ALTERA Cyclone II EP2C35F672C6 FPGA device which is presented in the ALTERA DE2 board. This interface unit is having ability to capture update information at the same rate they receive. The design is being operated with a clock of frequency 27MHz. This design uses only 664 out of 33,216 logic elements (2%), 1,128 out of 33,216 combinational functions (3%), 939 out of 33,216 dedicated logic registers (3%), 247 out of 475 total IO pins (52%), 43,545 out of 483,840 memory bits (9%), 0 out of 70 embedded multipliers 9-bit elements (0%), 1 out of 4 PLLs (25%). This synthesis results show that the CMOS camera interface unit uses only few resources available on ALTERA Cyclone II EP2C35F672C6 FPGA. Efforts are in progress to develop FPGA based intruder detection system by utilizing remaining resources available on Cyclone II EP2C35F672C6 FPGA.

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