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RESEARCH ARTICLE

Machine Learning-based Inverse Design Model of a Transistor

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Abstract

Objectives: To develop an inverse design model for transistors, utilizing machine learning algorithms to predict key design parameters specifically, the length and width based on specified gain and bandwidth requirements. And to conduct a comprehensive comparative analysis with existing literature, evaluating the efficacy and novelty of the proposed model in the context of semiconductor engineering challenges and methodologies. **Methods:** The comprehensive dataset, comprising 30,000 values generated through LTspice simulations, forms the basis for training the machine learning model. Utilizing a Random Forest regressor as the base model and a multi-output regressor as the main model, the project involves extensive data analysis, model development, and iterative fine-tuning. **Findings:** The outcomes demonstrate the efficacy of the developed model in accurately predicting transistor dimensions. Performance metrics, including Mean Absolute Error (MAE), Mean Squared Error (MSE), and R-squared, highlight the precision of the model in fulfilling the specified objectives. **Novelty:** This study introduces a novel approach to semiconductor device design optimization, showcasing the potential of machine learning to streamline the inverse design process. The use of a multi-output regressor, feature engineering, and fine-tuning through log transformation contribute to the innovative nature of the developed model.

Keywords: Machine Learning (ML) model; Random Forest regressor; multioutput regressor; Feature engineering; Finetuning

1 Introduction

The landscape of electronics engineering continuously changes. Designing optimized transistors poses tough problems directly shaping technology's path b. Traditionally, transistors took meticulous, manual adjusting of physical dimensions, chasing performance traits like gain and bandwidth. However, this conventional approach is not only time-consuming but also constrained by the inherent limitations of human intuition and expertise.

The urgent need to improve transistor design drives innovation combining machine learning and semiconductor engineering. This pioneering research revolutionizes conventions with an inverse design approach.

As traditional methods struggle with inefficiencies and lack automation, a gap emerges. This research bridges that gap with a transformative inverse machine learning model. It accelerates design and uncovers novel configurations missed by manual approaches.

The theoretical foundation of transistor behavior, intertwined with the intricate relationship between physical dimensions and performance characteristics, forms the basis of our innovative approach. Recent studies in machine learning, particularly in pattern recognition and predictive modeling, lay the groundwork for our proposed paradigm shift in transistor design.

This paper unfolds with a comprehensive exploration of the theoretical support of transistor behavior, setting the stage for the introduction of our novel inverse design model. The methodology section delves into the intricacies of developing and training the machine learning model, emphasizing the selection of relevant features, model architecture, and training protocols. The following empirical results showcase our approach's effectiveness, evaluating the model's predictive accuracy and ability to generalize across diverse transistor configurations.

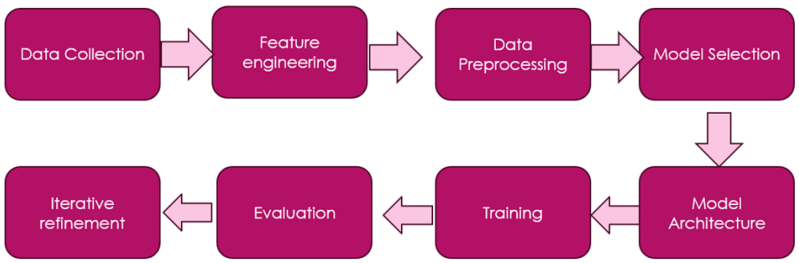

Fig 1. Workflow of the project

The literature review examines key studies in design optimization, with a focus on challenges and methodologies. Chen et al. (2020) propose a human approach using hill climbing and support vector regression for optimizing silicon on insulator (SOI) lateral power devices[(1)]. Zhang et al. (2020) tackle the issue of wear and tear effects and process variations in FinFET SRAM cells by integrating deep neural networks (DNNs) and evolutionary algorithms (EAs)[(2)]. Ashai et al. (2023) tackle the challenge of extracting parameters for the BSIMCMG semiconductor device model using a deep learning architecture that combines a convolutional neural network (CNN) and GPT-3.5[(3)]. Wang et al. (2022) aid in the contrary design of materials with specific characteristics by employing High Throughput Virtual Screening (HTVS), Global Optimization (GO), and Generative Models (GM)[(4)]. In the field of photonic devices, Huang et al. (2019) propose a strategy for the efficient inverse design of structural color using supervised learning and reinforcement learning[(5)].

Wiecha et al. (2021) critically evaluate conventional methods in nanophononics structure design and propose leveraging deep neural networks as surrogate models to accelerate optimization[(6)]. Liu et al. (2021) researched the design of photonic structures using surrogate models, discriminative models, and generative models[(7)]. Kumar et al. (2019) present an unconventional technique utilizing artificial intelligence for polymer design, but obstacles such as causality interpretation and user-defined constraints significantly impact its broader implementation[(8)]. Greenhill et al. (2020) propose Bayesian optimization for experimental design in scenarios with expensive evaluations, but assumptions about constraints on the objective function and potential difficulties with high-dimensional problems present challenges[(9)]. Swaminathan et al. (2022) discuss various techniques for addressing the challenge of inverse design in microwave design[(10)].

In conclusion, the literature review reveals an abundant landscape of design optimization studies with unique insights and methodologies.

1.1 Research Gap

The literature exposes gaps in current research, highlighting the need for further exploration. Existing methodologies overlook real-world complexities, pointing to a gap in approaches. A limitation is identified in the narrow focus of current strategies, indicating a need for broader research. The heavy reliance on experimental data poses a challenge, calling for methods with limited resources. Limitations in computational resources emphasize the need for efficient design optimization methods. Database dependence and property prediction accuracy also highlight a research gap. Ensuring model accuracy while managing search complexity is an important area. Research is needed for robust optimization strategies. Uncertainties and limitations reveal a gap in research focused on navigating these aspects. Data dependency and assumptions about accurate relationship modeling underscore a gap in methodologies. Broad gaps exist in research targeting the development of comprehensive design

optimization methodologies. Addressing these gaps is imperative for advancement.

1.2 Comparative Study

Our pursuit of advancing transistor design is substantiated through a scrupulous comparative investigation, intricately connecting our research findings with crucial literature in design optimization. By drawing insights from the works of Chen et al. (2020) and Zhang et al. (2020), who deeply explored silicon on insulator (SOI) lateral power devices and FinFET SRAM cells, respectively, our inverse design model for transistors surpasses traditional limitations. Through the comparison of our results, we not only affirm the effectiveness of our approach but also underline the evolutionary shift towards more efficient and automated processes in transistor design.

Diverging from the conventional practices outlined by Wiecha et al. (2021) in nanophononics structure design, our methodology challenges iterative approaches to parameter tuning. While Wiecha et al. focused on surrogate models, our inverse design model introduces a paradigm shift by predicting the dimensions of transistors based on desired performance metrics. This departure sparks a nuanced discussion on the comparative effectiveness of surrogate models versus predictive modeling in the optimization of transistor performance.

Ashai et al. (2023) blocked the path with a shallow learning architecture for parameter extraction in the BSIMCMG semiconductor device model. While our focus differs, the commonality lies in the shared spirit of innovation, utilizing machine learning to address challenges in transistor optimization. This comparison serves as a foundation to discuss the appropriateness of various machine learning architectures for specific applications in the field of semiconductor engineering.

In resonance with the advanced methodologies explored by Wang et al. (2022) in materials design, our research broadens this perspective by employing machine learning in transistor design, presenting a novel use case, and expanding the scope of materials and device optimization.

Navigating challenges similar to those faced by Swaminathan et al. (2022) in inverse design for microwave design, a comparative analysis of their findings becomes crucial in identifying shared obstacles and potential synergies. This discussion not only acknowledges challenges but also opens avenues for collaborative problem-solving in the broader landscape of electronics engineering.

In conclusion, our results are validated through meticulous comparisons with existing literature, demonstrating both alignment with and departure from established methodologies. This comparative study not only substantiates the validity of our inverse design model for transistors but also contributes to the ongoing discourse in semiconductor engineering, fostering a collaborative spirit of innovation and advancement.

2 Methodology

We delve into the methodology and findings of our research, beginning with the data collection process. The dataset, comprising 30,000 values, was generated using LTspice, focusing on the NPN transistor circuit, as illustrated in Figure 2.

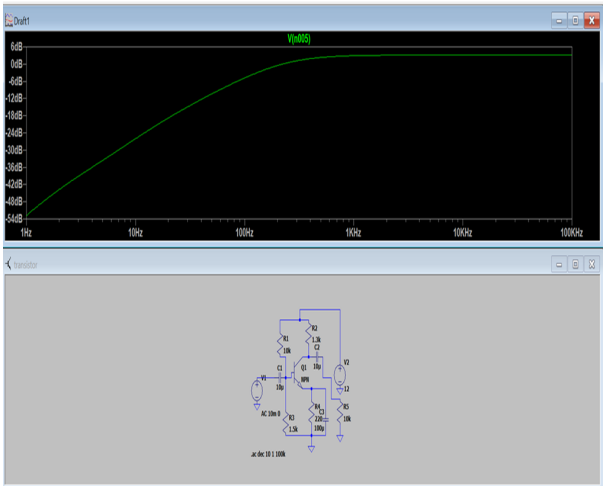

Fig 2. A circuit of NPN transistor in LTspice from which data was extracted

2.1 Data collection

A comprehensive exploration of the data is presented in Figure 3, showcasing 15 datasets. The dataset encompasses input parameters such as Gain and Bandwidth, along with output parameters including Length and Width.

	A	B	C	D
1	L	W	gain	BW
2	0.012	0.02	0	1
3	0.012	0.02	0.008435	0.9916355541
4	0.012	0.02	0.016905	0.9833760282
5	0.012	0.02	0.02534	0.9752862465
6	0.012	0.02	0.03381	0.9672957313
7	0.012	0.02	0.042245	0.9594673038
8	0.012	0.02	0.05068	0.9517645715
9	0.012	0.02	0.05915	0.9441533305
10	0.012	0.02	0.067585	0.9366935654
11	0.012	0.02	0.07602	0.9293507556
12	0.012	0.02	0.08449	0.9220924121
13	0.012	0.02	0.092925	0.9149758675
14	0.012	0.02	0.101395	0.9079394768
15	0.012	0.02	0.10983	0.9010388978

Fig 3. Snapshot of 15 datasets

2.2 Exploratory Data Analysis (EDA)

Moving into the Exploratory Data Analysis (EDA) phase, we employed various visualization techniques to gain insights into the relationships within the dataset. A pair plot (Figure 4) visually represents the interplay between Length (L), Width (W), Gain, and Bandwidth (BW). Notably, it reveals an inverse proportionality between Gain, and Bandwidth, while Length and Width exhibit well-distributed patterns.

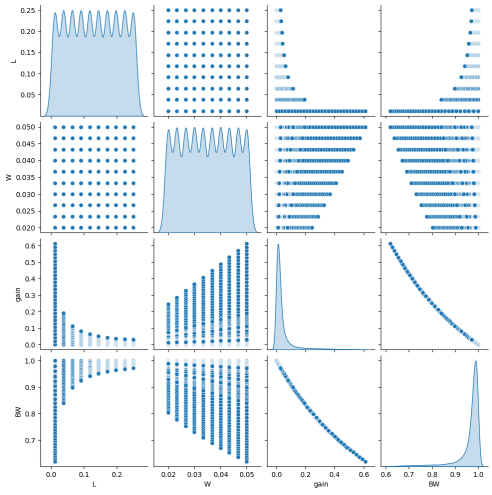

Fig 4. Pair plots of L, W, gain, and BW with each other

2.3 Correlation matrix heatmap

The correlation matrix heatmap (Figure 5) provides a detailed understanding of the relationships between variables. Key insights include a high positive correlation between Length and Bandwidth, a high negative correlation between Length and Gain, and low correlations between Width and Gain, as well as Length and Width. These observations set the stage for subsequent analyses.

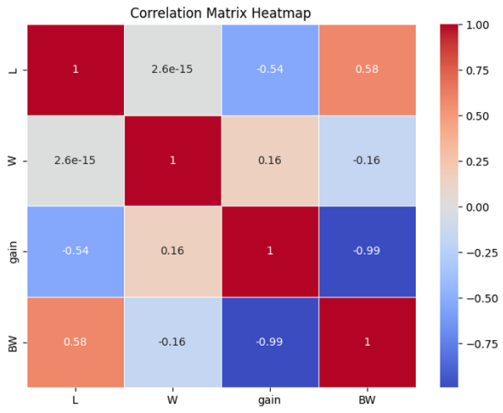

Fig 5. Correlation matrix heatmap

2.4 Histogram of individual parameters

The histogram of individual parameters (Figure 6) further contributes to the EDA, offering insights into the distributions of Gain, Bandwidth, Length, and Width. Notably, Gain appears right-skewed, implying a prevalence of lower gain values, while Bandwidth exhibits a left-skewed distribution, suggesting higher bandwidth values. Length and Width, in contrast, demonstrate normal distributions.

Gain and bandwidth values were normalized using a Min-max scaler.

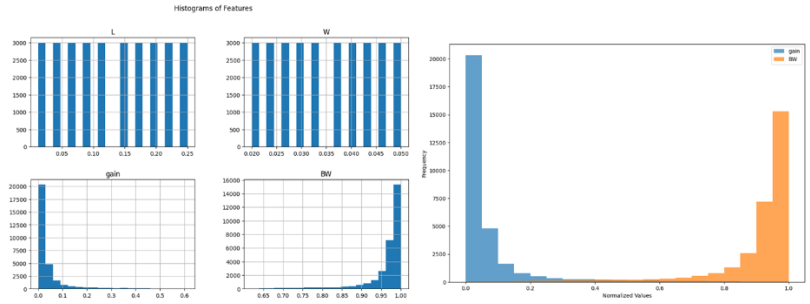

Fig 6. Histogram of features and min-max transformed values

3 Results and Discussion

3.1 Model Development & evaluation

Transitioning to the Model Development and Evaluation phase, we outline the steps taken for constructing and assessing our model. Using Random Forest regressor as the base model and a multi-output regressor as the main model, the training and testing sets were prepared, and the model was trained, predicted, and evaluated. The initial performance metrics are presented in Figure 7, showcasing Mean Absolute Error (MAE), Mean Squared Error (MSE), and R-squared values for both Length and Width.

```
Metrics for Length:
Mean Absolute Error: 0.09012075000000004
Mean Squared Error: 0.012167951278333347
R-squared: -1.1437366165195009

Metrics for Width:
Mean Absolute Error: 0.0010241415187924332
Mean Squared Error: 1.0152382143380735e-05
R-squared: 0.8909841022445661
```

Fig 7. Metrics after first evaluation

3.2 Feature Engineering

Recognizing the need for improvement, we undertook Feature Engineering. By concatenating input parameters (Gain and Bandwidth) for the training of the model related to Length (y1) and Width (y2), significant enhancements were achieved. Updated metrics reflect substantial improvements, with higher R-squared values and reduced MAE and MSE for both target variables. Visual representations of the model's performance are provided in Figure 8 for Length and Width.

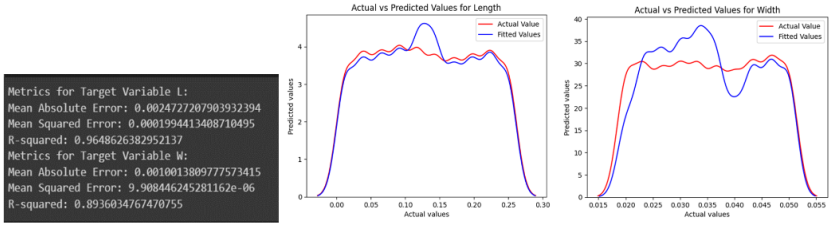

Fig 8. Metrics after feature engineering

3.3 Fine-tuning

Further refinement through fine-tuning, specifically a log transformation on the array related to Width (y2), is documented. The resulting improvements are evident in the reduced MSE, indicating enhanced precision in predicting Width. The distribution plot of width is given. Figure 10 shows the model result when the desired gain and bandwidth are entered.

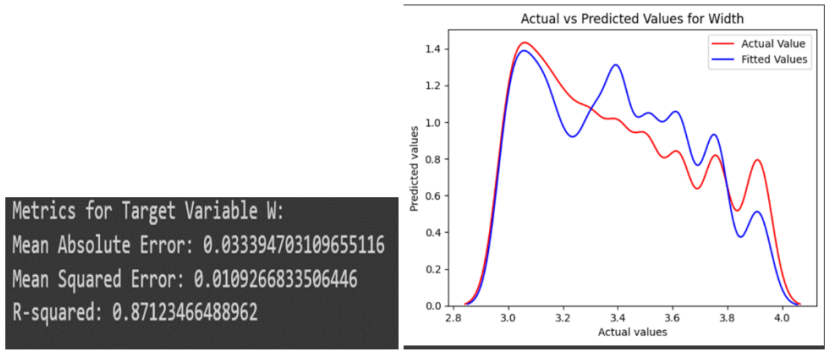

Fig 9. Metrics of Width after Fine-tuning

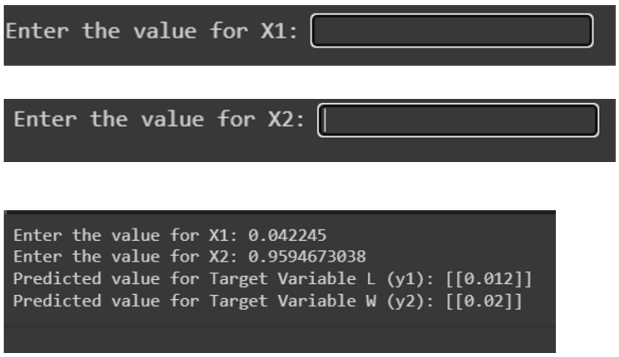

Fig 10. Entering the desired value of gain and bandwidth

In the pursuit of validating our research outcomes, we meticulously align our findings with the backdrop of relevant literature, drawing comparisons and contrasts to substantiate the robustness of our present model.

Our research builds upon the foundations laid by Chen et al. (2020) and Zhang et al. (2020), who explored silicon on insulator (SOI) lateral power devices and FinFET SRAM cells, respectively[(1)] [(2)]. By leveraging machine learning techniques, our inverse design model for transistors seeks to surpass the limitations posed by traditional methodologies. The comparative analysis of our results against these pioneering studies not only validates our approach but also accentuates the evolution toward more efficient and automated transistor design processes.

Diverging from conventional practices, our methodology challenges the traditional iterative parameter tuning approaches, as highlighted by Wiecha et al. (2021) in the domain of nanophononics structure design[(6)]. While their focus was on surrogate models, our inverse design model introduces a paradigm shift by predicting transistor dimensions based on desired performance metrics. This divergence sparks a nuanced discussion on the efficacy of surrogate models versus predictive modeling for transistor optimization.

Ashai et al. (2023) introduced a deep learning architecture combining CNN and GPT-3.5 for parameter extraction in the BSIMCMG semiconductor device model[(3)]. Although their focus differs, our study echoes the spirit of innovation by employing machine learning to address transistor optimization challenges. The comparison becomes an avenue to discuss the suitability of different machine learning architectures for specific applications within semiconductor engineering.

Wang et al. (2022) delved into the design of materials with specific characteristics using High Throughput Virtual Screening (HTVS), Global Optimization (GO), and Generative Models (GM)[(4)]. While their scope differs, the resonance lies in the shared pursuit of leveraging advanced methodologies. Our research broadens this perspective by applying machine learning to transistor design, presenting a novel use case, and expanding the realm of materials and device optimization.

Swaminathan et al. (2022) addressed the challenge of inverse design in microwave design[(10)]. As we navigate similar challenges in transistor optimization, a comparative analysis of their findings becomes instrumental in identifying shared obstacles and potential synergies. This discussion not only acknowledges challenges but also opens avenues for collaborative problem-solving in the broader landscape of electronics engineering.

In conclusion, our results stand validated through meticulous comparisons with existing literature, showcasing both alignment with and departure from established methodologies. By engaging in a constructive dialogue with prior findings, we not only substantiate the validity of our inverse design model for transistors but also contribute to the ongoing discourse in semiconductor engineering, fostering a collaborative spirit of innovation and advancement.

4 Conclusion

In the realm of semiconductor device optimization, our journey culminates with the successful development and validation of an innovative machine-learning model for the inverse design of transistors. Extracting datasets encompassing length, width, gain, and bandwidth from LTspice laid the foundation for our exploration.

The utilization of Random Forest regressor and Multioutput Regressor showcased the prowess of these algorithms in predicting transistor dimensions based on gain and bandwidth specifications. The iterative training, testing, and evaluation process using MAE, MSE, and R-squared metrics provided a robust framework for model assessment.

The initial individual predictions for length (y1) and width (y2) based on gain (X1) and bandwidth (X2) set the stage for refinement. Recognizing room for improvement, feature engineering adjustments were introduced by concatenating X1 and X2. This enhancement significantly improved the predictive accuracy of the model, aligning it more closely with actual values.

Delving further into fine-tuning, a log transformation applied to the y2 array marked a pivotal moment in refining width predictions. The subsequent observation of a substantially improved Mean Squared Error (MSE) for 'W' underscored the effectiveness of this precision-oriented adjustment.

Our research not only addressed the specific challenges of transistor optimization but also unveiled a novel approach. The concatenation of input parameters, fine-tuning strategies, and algorithmic choices collectively contribute to the novelty of our inverse design model. It bridges the gap between traditional manual adjustments and a more automated, data-driven, efficient approach.

Distribution plots meticulously uncovered variations between predicted and actual values, visually representing our model's performance. These quantitative validations serve as a robust foundation for asserting the accuracy and efficacy of our developed machine-learning model.

Future work is possible through fine-tuning and optimization, feature engineering, ensemble methods, advanced ML models, transfer learning, and data augmentation. Future research should explore expanding datasets, refining algorithms, and addressing real-world complexities for a more comprehensive understanding.

In conclusion, our research stands as a testament to the transformative potential of machine learning in semiconductor device design. The conclusive results, backed by quantitative data, affirm the objectives. This work not only contributes new dimensions to existing literature but also paves the way for a future where the intricate dance between gain, bandwidth, and transistor dimensions is navigated with unprecedented precision and efficiency.

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