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Ge/Si Hetero-Junction Hetero-Gate PNPN TFET with Hetero-Dielectric BOX to Improve I_{ON}/I_{OFF}

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Abstract

Objective: PNPN TFET is a semiconductor device in which the gate controls the source to channel tunneling current through modulation of band-to-band tunneling. Silicon film thickness is also optimized to remove the kink effect. **Methods/ Statistical Analysis:** As the Silicon device technology as downsized to nanometers, it experiences certain issues like short channel effects, low I_{ON}/I_{OFF} and low Sub-threshold Slope. The hetero-gate dielectric structure is designed with the addition of a hetero-dielectric Buried Oxide (BOX) on the doped substrate for reduction of ambipolar current and improvement of tunneling current at drain and source side respectively. The hetero-dielectric BOX has SiO_2 dielectric below source/channel regions and HfO_2 below the drain region. **Findings:** The proposed device type is of Ge/Si Hetero-junction hetero-gate dielectric with hetero-dielectric BOX PNPN Tunnel FET with low bandgap material at source region increases the tunneling probability and hence improves I_{ON}. Various combinations of the simulation where executed with reference to channel, source, drain and N pocket doping for getting the optimized results for Id-Vg characteristics. The entire simulations were done in licensed Cogenda TCAD version 1.7.4 software. The hetero-gate dielectric improves the I_{ON} and suppresses the ambipolar current. Also DIBN effect gets reduced because drain current is not varied with changes in Vds(V) values with respect to Vgs(V) values. With the proposed device we obtained the performance parameters as I_{ON}=1.24mA/μm, SS=44.66mv/dec and $I_{ON}/I_{OFF}=3.47\times10^{12}$. **Applications/Improvements:** Modeled PNPN TFET had resulted in improved performance in-terms of I_{ON}/I_{OFF} ratio, using low band gap material and hence is best alternative over the conventional CMOS devices for the low power and moderate speed applications of FPGA.

Keywords: Ambipolar Behavior, Band-to-Band Tunneling, Hetero-Dielectric BOX, Hetero-Gate, Power Delay Product (PDP), Sub-Threshold Slope, Tunnel FET

1. Introduction

As Metal-Oxide Semiconductor field effect transistor (MOSFET) scaled down, it showed the limiting factors based on short channel effects, Sub-threshold slope >60mV/decade. Now a day's lot of work has been done on band to band tunneling principle based Tunnel Field Effect Tansistor (TFET) devices[1-3]. The Tunnel FET have p-i-n structure which works by means of gate modulated tunneling, in any case it has one of the significant disadvantage of not having sharp tunneling near the source bending, due to which its I_{ON} gets reduced and which is not compatible with the ITRS requirement. So the obtained SS is higher than 60mV/decade[4,5]. The p-i-n structure have large tunneling width, due to that voltage drop occurs the tunneling junction reduces the I_{ON}. Generally conventional TFET have

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10μA I_{ON} which is half of ITRS requirement[6]. Various TFET types has been proposed in last two decades, starting from the Surface Tunnel Transistor, p-i-n based TFET, Feedback TFET, Vertical TFET, Junction less TFET, DG-TFET, p-n-i-n TFET Raised Buried Oxide Tunnel FET, Hetero-junction TFET, and Doping less TFET[7]. The idea of PNPN TFET[4] has been proposed as an alternative for getting enhanced SS and I_{ON}/I_{OFF}. Hetero-gate dielectric PNPN TFET is presented in[8].

The homojunction tunnel FET has some shortcomings like[7,9-11] minimum I_{ON}, ambipolar behavior, high I_{OF}F and maximum SS. As we use small band gap materials, they improve I_{ON} but at the same time I_{OFF} also gets increased[12-14], this happens as the TFET shows ambipolar behavior. In ambipolar behavior as we apply the negative gate bias, conduction occur at the drain/channel junction. This ambipolar behavior of TFET can be suppressed by making asymmetric structure with the help of different doping for the drain and the source region including different gate oxide materials with high k dielectric material near source region. Besides utilizing materials with smaller band gaps, hetero-junction devices could also be adopted. Using of small band gap material, the on-state current could be improved[15]. Channel and drain regions are made with materials having larger band gap, so that drain side tunneling leakage could be suppressed.

In this paper we propose a Ge/Si Heterojunction hetero-dielectric PNPN Tunnel FET which adds a hetero-dielectric BOX on the highly doped ground plane. The device is designed and simulated using licensed Cogenda TCAD software version 1.7.4. The structure surpasses the Drain – Induced Barrier Narrowing (DIBN) effect, which had been predominant in the previous designed PNPN structure.

The paper is sorted as follows: A brief presentation concerning Tunnel FET device is given in section-I. Section II portrays the device structure and its simulation. In section III, the electrical characteristic of proposed device has been analyzed. Section IV displays the outcomes and discussion about the proposed Ge/Si heterostructure hetero-gate dielectric with hetero-dielectric BOX PNPN Tunnel FET. At last, section V specifies the conclusion.

2. Device Structure and Simulation

Rather than utilizing p+ source as a part of an ordinary TFET, a tunneling junction is framed between the p+ area and a completely depleted thin n layer under the gate which decreases the tunneling width and makes nearby band bowing and in this manner a steep subthreshold slope is gotten. This n pocket enhances the tunneling by accomplishing steep subthreshold conduct and in the meantime gives high I_{ON} when contrasted with ordinary PNPN TFET utilizing Gate oxide made of HfO_2 (k=25) and SiO_2 (k=3.9)[17]. An option way to deal with totally wipe out the ambipolar conduction in TFETs by utilizing a hetero-dielectric BOX over a vigorously doped (P+) substrate of a N-channel PNPN TFET. The proposed device design encourages the depletion of the drain area at the channel-drain interface expanding the tunneling obstruction width on the drain side bringing about the suppression of the ambipolar conduction[16].

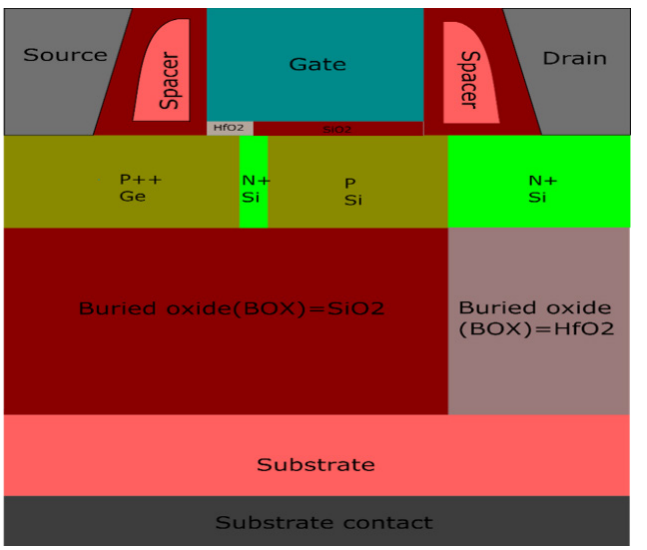

Figure 1. Structure of PNPN TFET.

The Ge/Si Heterojunction hetero-gate dielectric with hetero-dielectric BOX PNPN TFET structure is shown in Figure 1 Technology Computer Aided Design (TCAD) is an intense tool for 2D/3D simulation of devices. A device design can be optimized for decreasing the design costs, enhancing the device design efficiency and getting the better device and the technology designs. The simulation is helpful in predicting the electrical characteristics of devices. We have used a Kane Band-to-Band Tunneling model in which value of two parameters of Kane's model are A.BTBT = $3.9e+22eV^{(-1/2)}cm^{-1}s^{-1}V^{-2}$ and B.BTBT = $2.25e+07\ Vcm^{-1}eV^{(-2/3)}$. Also a mobility model like Lombardi mobility model is used.

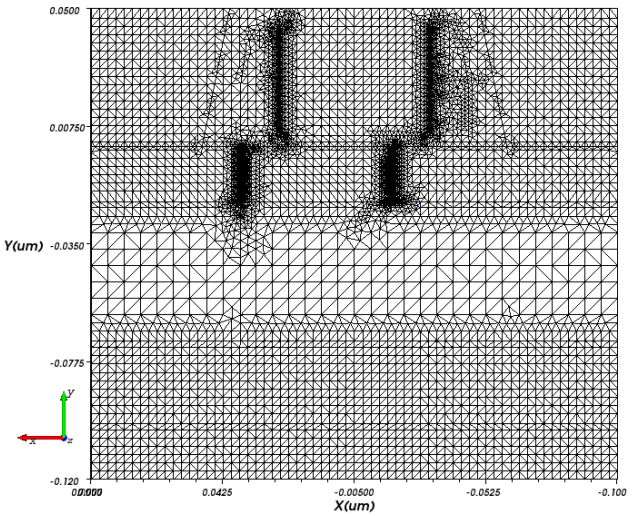

Figure 2. Mesh structure of the PNPN

A meshing is applied to the whole device to create the calculation points where the semiconductor equations are applied. Figure 2 shows a mesh structure of the simulated PNPN Tunnel FET. We can visualize that meshing is dense near the gate oxide/source/channel tunnel junction, where actual tunneling in TFET occurs so that accurate values of current and voltages can be predicted. When meshing is applied, the TCAD simulation software automatically predicts the junction points and finer mesh is applied to the region. Before we finalize our device parameters, we simulated the device and varied various parameters to analyze which device gives the best performance. Simulations are done at Vds = 1.2V and Vgs is varied from 0 to 2.5V.

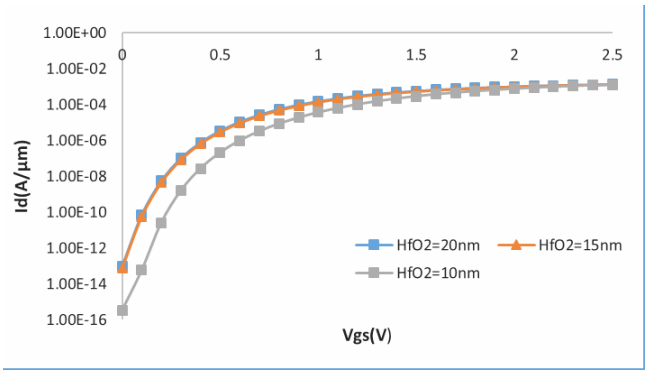

Figure 3. Id-Vg characteristics of HfO_2 length variations.

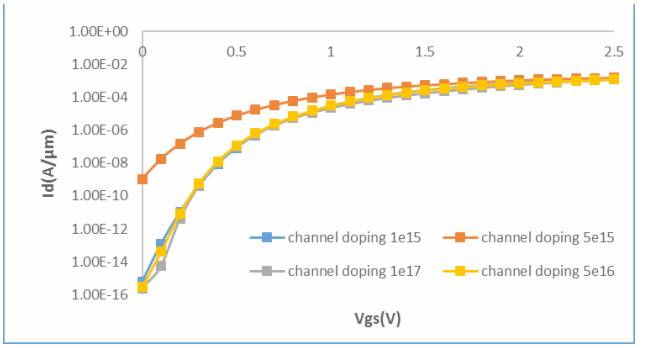

Figure 4. Channel doping variations.

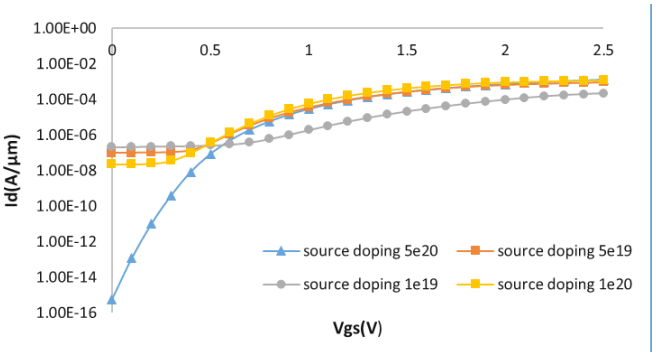

Figure 5. Source doping variations.

In the proposed device we have used two dielectrics for gate oxide namely: High-k HfO_2 and Low-k SiO_2 hetero-dielectric. The Plot of Id-Vg characteristics for various HfO_2 lengths are shown in Figure 3. Among them at 10nm we get higher I_{ON}. To ponder the impact of channel doping on device performance, we have varied the channel doping, keeping source and drain doping to 5e+20 atoms/cm-3 and 5e+18 atoms/cm-3 respectively. The proposed device is N- type Tunnel FET, in which channel region is n type doped. We varied the Nd concentration from 1e+15, 5e+15, 1e+16, 5e+16 and 1e+17 atoms/cm-3. Drain current values for channel doping with 5e+15atoms/cm-3 are better among them. There is not much difference in the Id-Vg characteristics for these values as indicated in Figure 4. At 5e+20atoms/cm-3 have better drain current for source doping as shown in Figure 5. Also n packet doping's varying with 1e+19, 5e+18, 5e+19 and 1e+20 atoms/cm-3. Among them 1e+19 shows better I_{ON} as shown in Figure 6. The alternative variations in work function for 4.17, 4.33,

4.7 and 4.5eV where analyzed; 4.5eV shows steeper performance as indicated in Figure 7. When we change the position of the N packet which is extra layer in PNPN, it changes its Id-Vg characteristics and it shows superior performance under half of HfO_2 and half of SiO_2 as drawn in Figure 8. The simulated device parameters are listed in Table 1 which indicates region materials, contact materials, region thickness/length and doping concentrations of the regions. Gate material is of NpolySi.

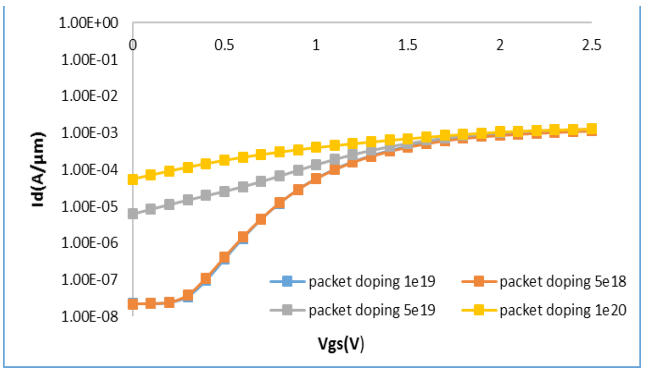

Figure 6. N packet doping variations.

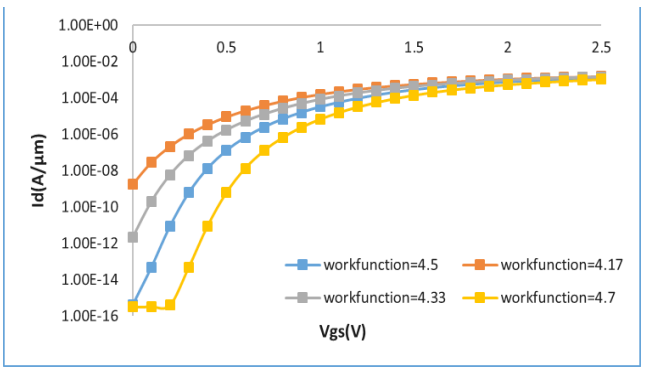

Figure 7. Work function variations.

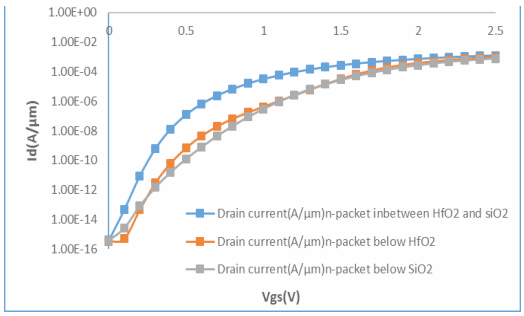

Figure 8. N packet position variations.

In the proposed device we have used two dielectrics for gate oxide namely: High-k HfO_2 and Low-k SiO_2 hetero-dielectric. The Plot of Id-Vg characteristic for various HfO2 lengths is shown in Figure 3. Among them at 10nm we get higher I_{ON}. To ponder the impact of channel doping on device performance, we have varied the channel doping, keeping source and drain doping to 5e+20 atoms/cm-3 and 5e+18 atoms/cm-3 respectively. The proposed device is N-type Tunnel FET, in which channel region is n type doped. We varied the Nd concentration from 1e+15, 5e+15, 1e+16, 5e+16 and 1e+17 atoms/cm-3. Drain current values for channel doping with 5e+15atoms/cm-3 are better among them. There is not much difference in the Id-Vg characteristics for these values as indicated in Figure 4. At 5e+20atoms/cm-3 have better drain current for source doping as shown in Figure 5. Also n packet doping's vary with 1e+19, 5e+18, 5e+19 and 1e+20 atoms/cm-3. Among them 1e+19 shows better I_{ON} as shown in Figure 6. The alternative variations in work function for 4.17, 4.33, 4.7 and 4.5eV where analyzed; 4.5eV shows steeper performance as indicated in Figure 7. When we change the position of the N packet which is extra layer in PNPN, it changes its Id-Vg characteristics and it shows superior performance under half of HfO_2 and half of SiO_2 as drawn in Figure 8. The simulated device parameters are listed in Table 1 which indicates region materials, contact

Table 1. Design parameters of the device

Region	Contact material	Material	Thickness/ Length	Doping (Atoms/cm^3)
Source	Aluminium (Al)	Ge	50nm	N_A (P++ type) 5×10^{20}
Drain	Aluminium (Al)	Si	50nm	N_D (N+ type) 5×10^{18}
Channel	–	Si	50nm	N_D (N type) 5×10^{15}
N pocket	–	Si(4nm)	20nm	N_D (P type) 1×10^{19}
Substrate	Aluminium (Al)	Si	30nm	N_A (P type) 1×10^{17}
Buried Oxide	–	SiO_2(136nm) +HfO_2(54nm)	50nm	–
Gate Oxide	–	HfO_2(10nm) + SiO_2(40nm)	4nm	–
Spacer	–	Nitride	20nm	–

materials, region thickness/length and doping concentrations of the regions. Gate material is of NpolySi.

3. Electrical Characteristics of Proposed Device

The choice of source/channel materials with the reduced (effective) band gap is important for increasing tunneling current with suppressing OFF current. By utilizing materials with smaller band gaps, the on-state current of a tunneling FET could be greatly improved. The flow of electric current is from source region to channel region and then from channel region to drain region where as the flow of hole current is from drain region to channel region and from channel region to source region which is seen in Figure 9 and Figure 10 respectively. Figure 11 shows that by varying Vds from 0V to 2.4V; the plot of Id vs Vgs are analyzed. These values predict that, for different values of Vds, Id value varies in a small fraction. It means that the proposed device doesn't show any drain induced barrier narrowing (DIBN) effect[17].

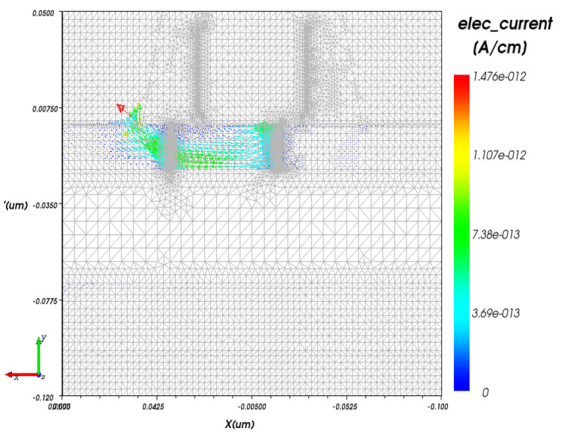

Figure 9. Electric current.

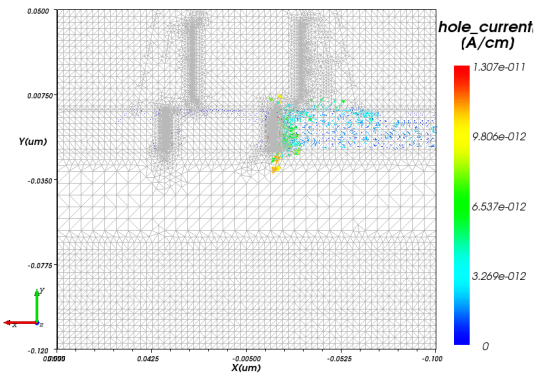

Figure 10. Hole current.

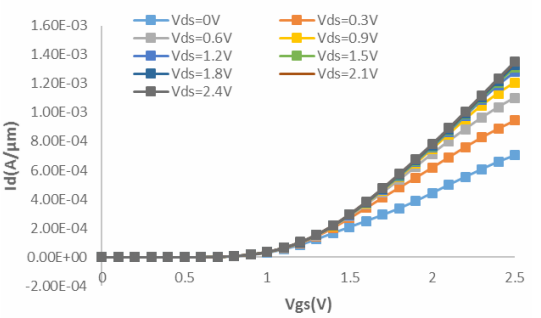

Figure 11. Id-Vg characteristics.

When PNPN TFET is in OFF-state i.e. Vgs = 0V; TFET is reverse biased which ends up in larger tunneling barrier width. A High-k HfO_2 dielectric oxide is used near source/channel junction due to which valance band of channel near source end will be increased. This reduces the tunneling probability and thus we get lowest OFF-state current as appeared in Figure 12. Once TFET is in ON state i.e. Vgs = 2.5V, electrons begin tunneling from valance band of P++ source to the conduction band of the N channel then towards the conduction band of the N+ drain region[18] as shown in Figure 13. In Figure 14 potential distribution is shown at Vdd=0.6V; when Vgs=0V then potential distribution is in linear manner and when Vgs=2.5V it increases in appropriate proportion.

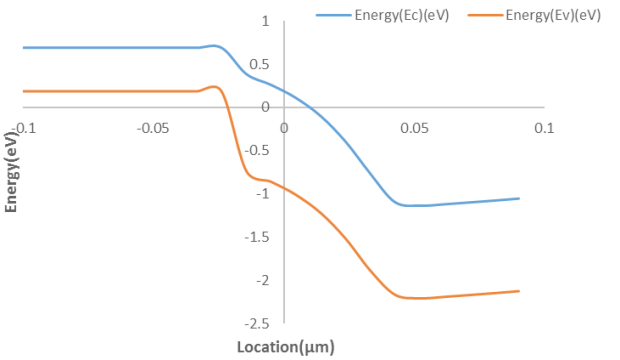

Figure 12. Energy band diagram at Vgs=0V.

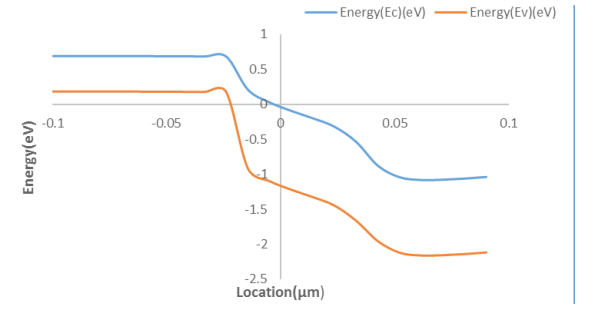

Figure 13. Energy band diagram at Vgs=2.5V.

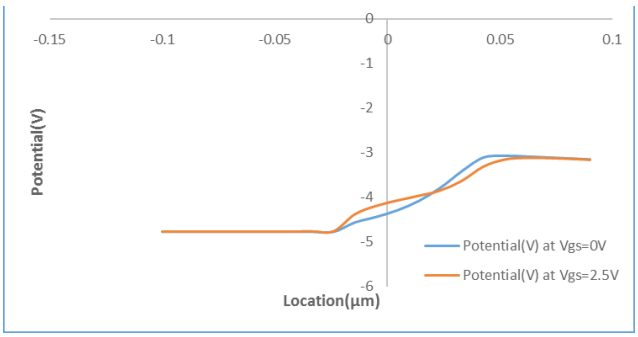

Figure 14. Potentials distribution at Vdd=0.6V.

4. Results and Findings

From the electrical characteristics, we studied and analyzed the performance of the device. We extracted I_{ON}, I_{OFF}, Sub-threshold slope, switching delay, power dissipation and PDP from simulated data at Vdd=0.6V, I_{ON}=9.62×10^{-7}A/μm and $C_{g,avg}$=1×10^{-15}F.

4.1 Subthreshold Slope/Swing (SS)

The sub-threshold swing (SS) is vital property of TFET: smaller the SS, the better is the dynamic performance. Subthreshold Swing/Slope can be described as Gate Voltage required to change drain to Source current by one decade. It can be determined as the inverse of slope of the log Ids vs Vgs curve, in the subthreshold exponential region[19].

$$SS = \frac{\partial V_{gs}}{\partial(\log I_d)} \quad (1)$$

The switching speed of a device is determined by SS[20].

4.2 Transconductance

It is defined as the adjustment in the drain current divided by the little change in the gate-to-source voltage with a consistent drain-to-source voltage and it is measured in Siemens.

$$g_m = \frac{\partial I_d}{\partial V_g} \quad (2)$$

4.3 Switching Delay

Switching delay is given by[21].

$$\tau = \frac{C_{g,avg} V_{dd}}{I_{ON}} \quad (3)$$

$C_{g,avg}$ is average capacitance across the gate bias range.

4.4 Dynamic Power Dissipation

$$P_{dynamic} = C_{g,avg} V_{dd}^2 f \quad (4)$$

4.5 Power Delay Product

Represents Power-Performance trade-off at provided operation frequency and is given by[21].

$$PDP = C_{g,avg} V_{dd}^2 f \times t_{delay} \quad (5)$$

The electrical parameters that we have considered in this paper are the following: the ON-current and the sub-threshold swing. The ON-current is defined as the drain current at a gate voltage of 0.6V. The threshold voltage is defined as the gate voltage when the drain current reaches 1 × 10^{-7} A/μm. For Vds=0.6V; I_{OFF}= 3.17× 10^{-16}A/μm at Vgs=0V and I_{ON}=1.24mA/μm at Vgs=2.5V.

Results are listed in Table 2.

Table 2. Simulated results

Parameters	Proposed TFET Device
ION(mA/μm)	1.24
IOFF(fA/μm)	0.317
ION/IOFF (× 1012)	3.47
Subthreshold Slope(mv/dec)	44.66
Transconductance(× 10-6 S)	7.84
Switching delay (psec)	623.7
Power dissipation (pWatt)	0.36
PDP (× 10-22 J) at Vds = 0.6V	2.24

5. Conclusion

The Ge/Si Heterojunction hetero-gate dielectric with hetero-dielectric BOX PNPN Tunnel FET with low band-gap material at source region increases the tunneling probability and hence improves I_{ON}. With the different variations of channel, source, drain and N pocket doping, we selected best value from Id-Vg characteristics. Also we had varied the work function for exploring the possibilities of improvement of I_{ON} and reduction of I_{OFF}. Hetero gate dielectric improves the I_{ON} and suppress the ambipolar current. Also DIBN effect gets reduced because drain current is not varied with changes in Vds(V) values with respect to Vgs(V) values. Heterodielectric Buried Oxide (BOX) layer reduces the parasitic capacitance and reduces

the leakage currents and also suppress the ambipolar behavior. We obtained $I_{ON}/I_{OFF}=3.47\times10^{12}$, SS=44.66mV/dec which is greater than [17]. From this study, we conclude that PNPN TFET with low bandgap materials and with the combinations of hetero-dielectric is the promising key alternative for high speed low power FPGA applications. In future, with the help of low band gap materials like SiGe/Si with varied concentration PNPN TFET can be designed.

6. References

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