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A New Improved Trans Z Source Inverter based Three Phase UPS

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Abstract

Objective: In applications like Wind Energy Conversion System, electric cell power conversion and Grid-connected PV generation, a small DC source voltage should be boosted to induce fascinating AC output voltage. **Methods/Statistical Analysis:** Z Structured Impedance Source Inverter (ZSI) is well-liked for its buck to boost operations. The high voltage gain will be obtained from the normal Z Structured Impedance Source Inverter at low modulation index state. On the other side, a little modulation index state produces high voltage stress at the inverter side switches. To defeat this problem, a Trans Z Structured Impedance Source Inverter (TZSI) is developed. In TZSI, transformer winding turns demand is high and the windings get burnt because of high instant current throughout shoot through length. **Findings:** A new topology of Trans Z Structured Impedance Source Inverter is introduced in this paper to boost the voltage gain fair enough. In this new topology the winding turn's usage is smaller amount and consequently inverter gain is lift up by lower the modulation index. To validate the ideas planned in theories, experimental results were taken and bestowed in this paper. **Application:** This inverter is utilized for three faze Uninterruptable Power Supply. The proposed inverter is designed and simulated in MATLAB/Simulink podium for 3 KVA load capacity and it will sustain the specified output voltage with the substantial drop in voltage at battery bank side.

Keywords: PWM Inverter, Shoot Through Period, Trans Z Source Inverter (TZSI), Uninterruptable Power Supply (UPS), Z Source Inverter (ZSI)

1. Introduction

Uninterruptible Supply scheme is used to offer uninterrupted, consistent and prime quality power to critical loads. It offers protection against irregular power-line voltage or power outage to critical loads. Three different UPS are there traditionally in three wire system. The primary type stepped up transformer needs enhanced inverter side output voltage[1], as in Figure 1(a). At this time the current in inverter is much higher than the current at load side. Owing to this, current stress raise happens on the switches in inverter and conjointly increases transformer weight, size and volume. The second kind requires DC/DC boost converter, inverter as in Figure 1(b). During this type, the extra boost converter results in high prize, difficult boost management and low efficient output. The inverter with dead time requires protection for short circuit of inverter in the same leg. Also dead time distorts the output voltage wave shape. The third sort UPS, the necessity of booster circuit is eliminated and it provides single stage power translation during ZSI[2–6] as like Figure 1(c). The voltage plane of ZSI isn't ample with low modulation index (M) condition from[7–10]. In addition ZSI leads high voltage stress in switching mechanism[11–13].

To overcome listed troubles in the TZSI is introduced. In TZSI transformer winding turns demand is high.

This study presents a unique topology of Trans Z Structured Impedance Source Inverter so as to produce

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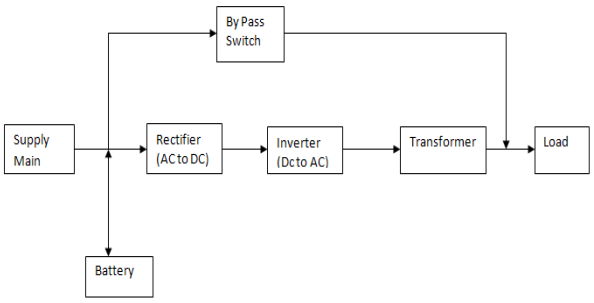
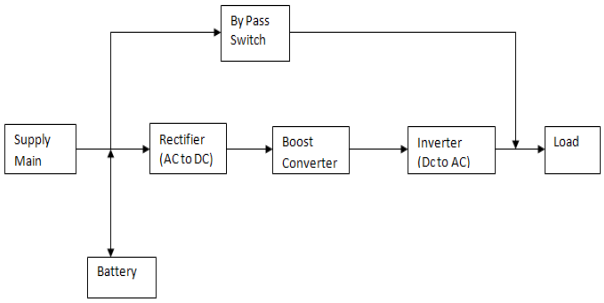
improved performance in TZSI. This improved TZSI is implemented in UPS system, as shown in Figure 1 (d). This new suggested UPS offers the subsequent deserves than the traditional UPSs:

- One step power conversion by mingling DC/DC converter with the inverter operation.
- Elimination of dead time interval within the PWM signal results reduction of AC output-voltage wave shape distortion.
- The output voltage level inverter is high enough throughout low modulation index condition by means of voltage stress reduction across the switching elements.
- The transformer winding turns demand is smaller amount and it needs less shoot through duration
- Quick transient response and sensible steady state performance is achieved by adopting twin-loop control.



(a)



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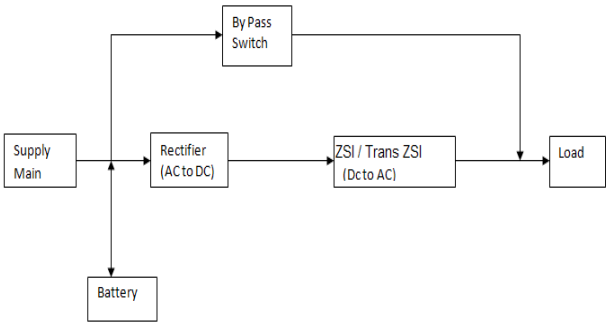
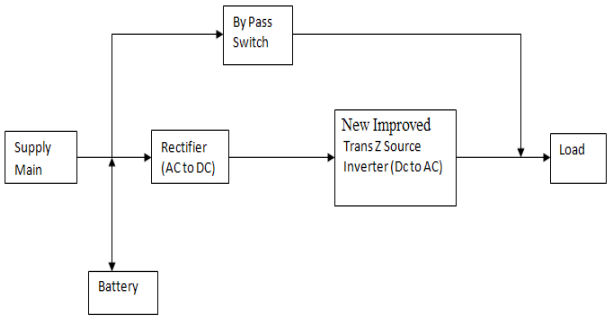


(c)



(d)

Figure 1. Topologies of UPS.
(a) Inverter + Transformer. (b) DC/DC Booster + inverter. (c) Z/Trans ZSI. (d) A New Improved Trans ZSI.

2. System Arrangement and Description

Figure 1(d) shows a brand new topology of the UPS through a proposed inverter. During regular operation, the battery bank and inverters are powered by the rectifier unit. In case of power failure, the battery bank energises the inverter as like Figure 2.

It consists of a DC supply (Rectifier, battery V DC, Capacitor C4 and diode D), Novel impedance network (W1, W2, C1, C2 and C3), PWM inverter switch (S1-S6), Inductive Filter Ls and Capacitive filter Cs. The gate pulses to the inverter are given as Z Structured Impedance Source Inverter triggering. The Novel impedance network makes the projected UPS to produce the desired AC output voltage, in spite of the battery powered DC voltage. While improved TZSI in T1 time interval (non shoot-through state), on condition of diode D, starts to charging of capacitors C1 and C2 in one direction while C3 in conflicting direction.

The improved TZSI equivalent circuit on non shoot-through interval (T0) is viewed in Figure 3.

The consequent voltage expression is written as:

$$Vc1 + Vc2 = Vin \quad (1)$$

$$Vw1 + Vc1 = Vdc \quad (2)$$

The C2 capacitor voltage is remains same as of winding W2 voltage. Once Improved TZSI is Functioning on shoot-through state (T0 time Interval), D the diode is in reverse bias condition. C1 and C2 Capacitors discharge their stored energy to the transformer. Improved TZSI on shoot-through time interval is bestowed in Figure 4.
The respective voltage expressions are written as:

$$Vw2 = Vc2 = -Vc1 \quad (3)$$

$$Vw2 = Vw1 + Vc3$$

VC1 Average value = 0

$$(Vdc - Vw1)T1 - Vw2To = 0$$

$$Vw2 = \frac{VdcT1}{nT1 + T0} \quad (4)$$

VC2 Average value = 0

$$(Vc1 - Vin)T1 + Vc1T0 = 0$$

$$Vc1 = \frac{VinT1}{T} \quad (5)$$

$$Vin = \frac{VdcT1}{(nT1 + T0)d} \quad (6)$$

$$Vin = BVdc$$

$$B = \frac{T1}{(nT1 + T0)d} \geq 1 \quad (7)$$

Vin Peak DC link voltage, B boost factor is acquired at shoot through interval. Vac The peak phase voltage is expressed as

$$Vac = MB\frac{Vdc}{2} \quad (8)$$

$$Vac = M\frac{T1Vdc}{(nT1 + T0)2d} \quad (9)$$

Where M is modulation index?

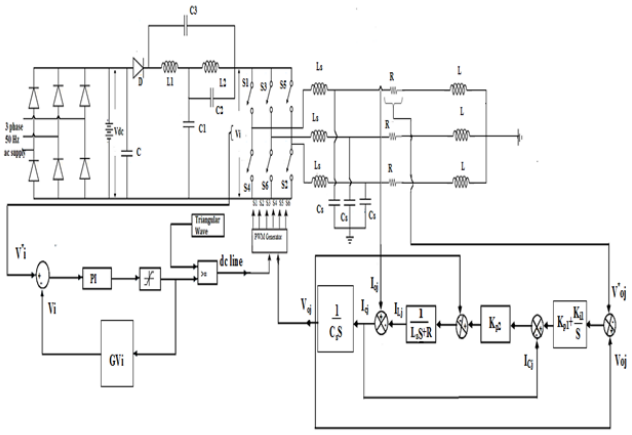


Figure 2. Proposed UPS with new improved TZSI.

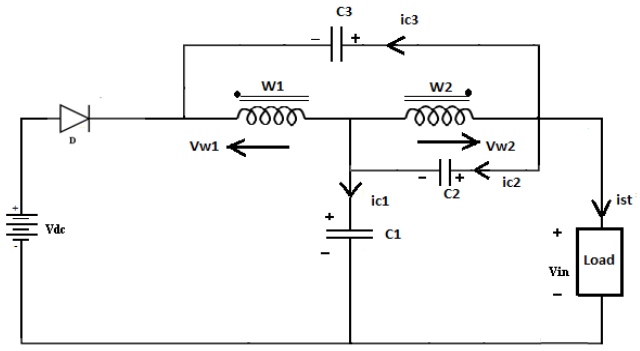


Figure 3. New improved ZSI in non shoot-through interval.

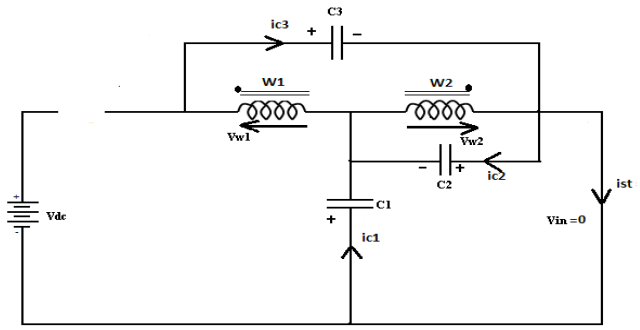


Figure 4. New improved ZSI in shoot-through interval.

3. Proposed UPS with Improved RZSI Control

Figure 2 presents proposed UPS twin loop control with improved TZSI. The appropriate choice of d and M produces the necessary output voltage despite of battery voltage. The range of T0 period is decided by duty ratio. This involves control of DC link voltage level and it is revealed in Figure 5. Reference voltage V^*_i compared with DC link voltage V_i.

The error signal sent to the PI Controller to optimize the output voltage and it is limited to 0.99. Therefore the saturation limiter connected to the controller circuit and it limits the error signal to maximum of 0.99. Thus the simple boost controller DC line obtains the constant value from this limiter. The DC constant value is match up with the triangular wave to estimate shoot though interval. The evaluation of shoot through interval (T0) is shown in Figure 6.

$$\begin{bmatrix} \dot{I}_{L1} \\ \dot{I}_{L2} \\ \dot{V}_{C1} \\ \dot{V}_{C2} \\ \dot{V}_{C3} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{CL} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{CL} & 0 \\ \frac{1}{CL} & -\frac{1}{CL} & 0 & 0 & 0 \\ \frac{1}{CL} & \frac{1}{CL} & 0 & 0 & 0 \\ \frac{1}{CL} & 0 & 0 & 0 & 0 \end{bmatrix} * \begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{C1} \\ V_{C2} \\ V_{C3} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ -1 & -R & 0 \\ -1 & 0 & 0 \end{bmatrix} * \begin{bmatrix} I_{dc} \\ I_0 \\ V_{dc} \end{bmatrix}$$

In this Figure 6 the triangular carrier wave height is represented as HT and DC line voltage height is represented as HP. W and T0 are the Width of triangular carrier wave and shoot through rate is represented as W and T0.

The calculation of shoot through interval can be articulated as:

$$T0 = \frac{HT - HP}{HT} * W \tag{10}$$

The Control methodology of simple boost is revealed in Figure 7. The evaluation of shoot through interval and non shoot through interval is feasible with this flow diagram. The firing pulse for devices is often programmed victimization the Figure 7. The modulation index control utilizes twin loop control as expressed in Figure 8. The inner load current (i_{0j}) is match up to reference current (I_{Lj}). The result is match up with capacitor current (I_{Cj}) and it's given to the proportional gain controller (K_p). Reference output voltage V_{oj} estimation involves the (I_{Lj}) and (I_{Cj}) prediction. The reference output voltage (V_{oj}) given to feedback loop and conjointly given to the gate circuit wherever the proportional modulating sine wave voltage calculable.

By referring Figure 4 the Laplace Transform equations for T0 interval is expressed below:

$$-L_1 sI_{L1}(s) = \frac{2}{C_1 s} I_{C1}(s) \tag{11}$$

$$L_2 sI_{L2}(s) = \frac{1}{C_2 s} I_{C2}(s) = -\frac{1}{C_1 s} I_{C1}(s) \tag{12}$$

$$\frac{1}{L_1 s} I_{L1}(s) + \frac{1}{L_2 s} I2(s) = C_2 sI_{C2}(s) \tag{13}$$

$$C_3 sI_{C3}(s) = \frac{1}{L_1 s} I_{L1}(s) \tag{14}$$

By referring Figure 3 the Laplace Transform equations for T1 is written below:

$$L_1 sI_{L1}(s) + \frac{1}{C_1 s} I_{C1}(s) = V_{dc} \tag{15}$$

$$L_2 sI_{L2}(s) = \frac{1}{C_2 s} I_{C2}(s) \tag{16}$$

$$C_1 sI_{C1}(s) = \frac{1}{L_1 s} I_{L1}(s) - \frac{1}{L_2 s} I_{L2}(s) \tag{17}$$

$$C_2 sI_{C2}(s) = \frac{1}{L_2 s} I_{L2}(s) + \frac{1}{L_1 s} I_{L1}(s) - I_{dc} - I_0 \tag{18}$$

$$C_3 sI_{C3}(s) = \frac{1}{L_1 s} I_{L1}(s) - I_{dc} \tag{19}$$

To simplify the analysis assume C1 = C2 = C3 = C and L1 = L2 = L. The dynamic Equation for the T1 interval is written as:

$$\begin{bmatrix} \dot{I}_{L1} \\ \dot{I}_{L2} \\ \dot{V}_{C1} \\ \dot{V}_{C2} \\ \dot{V}_{C3} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{2}{CL} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{CL} & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \frac{1}{CL} & \frac{1}{CL} & 0 & 0 & 0 \\ \frac{1}{CL} & 0 & 0 & 0 & 0 \end{bmatrix} * \begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{C1} \\ V_{C2} \\ V_{C3} \end{bmatrix}$$

$$\dot{X} = A_{st} X + B_{st} U \tag{20}$$

The dynamic Equation for T0 interval is written as:

$$\dot{X} = A_{Non} X + B_{Non} U \tag{21}$$

The small signal perturbations $\hat{V}_{dc}(t)$ and $\hat{d}(t)$ are given as input level voltage and duty ratio to the state variable in order to derive the small signal model. The State Space Average Method formulated as[14]:

$$sC_1 \hat{V}_{C1}(s) = dR\, I_0(\dot{s}) + RI_0 d(s) \tag{22}$$

$$\begin{aligned} \ddot{X} = {} & (dA_{st} + (1-d)A_{Non})\dot{X} + (d.B_{st} + (1-d)B_{Non})\dot{U} \\ & + ((A_{st} - A_{Non})X + (B_{st} - B_{Non})U))\hat{d}(t) \end{aligned} \tag{23}$$

Subsequent application of Laplace transform for the above Equation becomes:

$$sL_1\hat{I}_{L1}(s)=(-\frac{(1-d}{CL})\dot{V}_{C1}(s)+(1-d)\dot{I}_{dc}(s) -\frac{1}{CL}V_{C1}(s)-V_{dc}d(s) \quad (24)$$

$$sL_2\hat{I}_{L2}(s)=\frac{1}{CL}\dot{V}_{C2}(s) \quad (25)$$

$$sC_2\hat{V}_{C2}(s)=\frac{2}{LC}(1-d)\dot{V}_{C2}(s) -(\frac{R}{L})d\dot{I}_0(s)+(i_{dc}+i_0)d(s) \quad (26)$$

$$sC_3\hat{V}_{C3}(s)=\frac{1}{LC}\dot{V}_{C3}(s)-(1-d)\dot{I}_{dc}(s)+I_{dc}\,d(s) \quad (27)$$

The response of each state variable expressed as a linear combination of perturbation variables by solving the above Equations the DC side voltage gain GV_i as follows:

$$GV_i=\frac{Ls^2I_{L1}+((1-d)(V_{C1}+V_{C2})-(1-d)i_{dc})s-V_{dc}R}{LCs^3-(1-d)s^2-\frac{1}{LC}s+(1-\frac{R}{C})} \quad (28)$$

For the AC-side control management, the voltage regulation explored in traditional control method for the individual system. In order to get a good control system, AC side dynamics should be designed more quickly than the DC side to prevent oscillation. The control parameter change in DC side control will limit the AC side, as the shoot through interval is limited within the zero state. The controller generally will achieve good performance with higher end of input voltage.

The AC side controller consists of inner and outer control loops. Stabilized output and quicker response for a current disturbance is achieved via proportional controller that is employed in the midst of inner loop current. PI compensator, the glorious control loop that produces the stabilized variations and quick reference tracking. The Mason's gain rule applied to estimate the system transfer function as follows:

$$G^{Icj}_{I^*cj}(s)=\frac{Icj(s)}{I^*cj}=\frac{K_{p2}C_ss}{L_sC_ss^2+(R+K_{p2})C_ss+1} \quad (29)$$

$$G^{Icj}_{Ioj}(s)=\frac{Icj(s)}{Ioj(s)}=\frac{L_sC_ss^2+Rs}{L_sC_ss^2+(R+K_{p2})C_ss+1} \quad (30)$$

$$G^{Voj}_{V^*oj}(s)=\frac{Voj(s)}{V^*oj(s)} =\frac{(K_{p1}+K_{i1})K_{p2}}{L_sC_ss^3+(R+K_{p2})C_ss^2+(1+K_{p2}K_{p1})s+K_{i1}K_{p2}} \quad (31)$$

$$G^{Voj}_{Ioj}(s)=\frac{Voj(s)}{Ioj(s)} =\frac{L_ss^2+Rs}{L_sC_ss^3+(R+K_{p2})C_ss^2+(1+K_{p2}K_{p1})s+K_{i1}K_{p2}} \quad (32)$$

Where $G^{Icj}_{I^*cj}(s)$ and $G^{Icj}_{Ioj}(s)$ are control input-to-output and disturbance signal-to-output side inner loop transfer function. $G^{Voj}_{V^*oj}(s)$ and $G^{Voj}_{Ioj}(s)$ are control input-to-output, disturbance signal-to-output of outer voltage loop transfer function, respectively: K_{p2}, K_{p1}, K_{i1} are proportional gain 2,1 and integral gain parameters respectively. Further it is given to the simple boost control strategy reference voltage control circuit to fix the modulation index value.

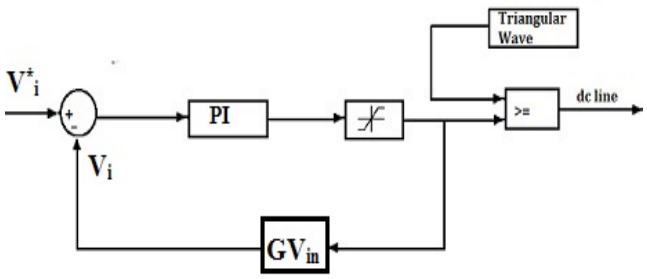


Figure 5. Block diagram of DC link control.

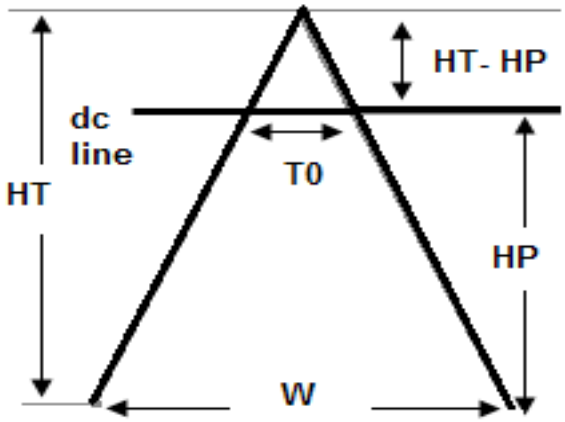


Figure 6. Evaluation of shoot through interval

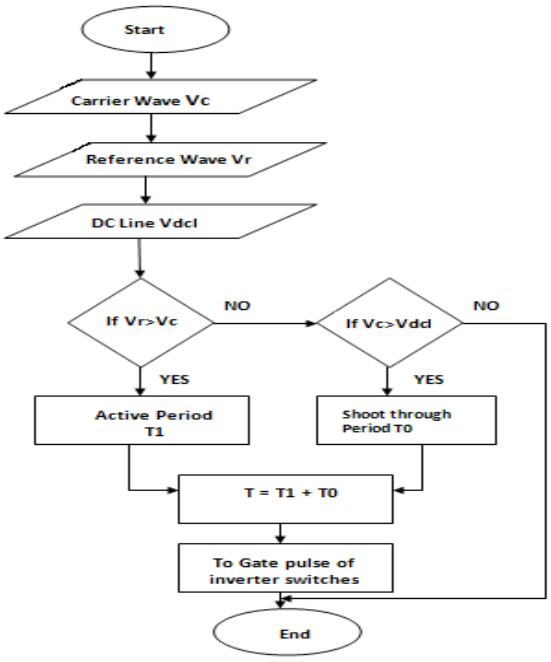


Figure 7. Flow chart for SBC method.

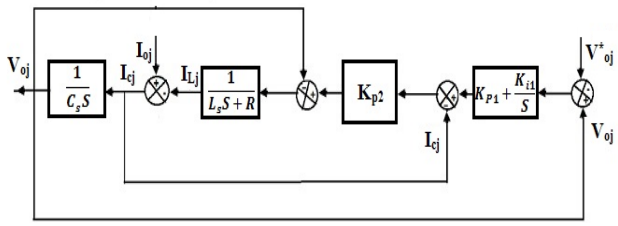


Figure 8. Block diagram of AC side control.

4. Simulation Results and Discussions

The suggested UPS is compared with traditional Z Structured Impedance Source Inverter based UPS and with Trans Z Structured Impedance Source Inverter (TZSI) based UPS. MATLAB/Simulink plat form kind is effectively utilized to replicate the system. The circuit parameter for simulation is exposed in Table 1.

The simulation is done at the switching frequency rate of 10 KHz, switching period of time Ts is 5×10^{-5} sec and T1 interval is 0.08×10^{-4} sec. M, T0/T1 is set to 0.84 and 0.16. The system intention is to generate a three phase AC output voltage of 415 V from DC voltage supply of 154.5 V. From the above analysis the subsequent theoretical calculations are done.

$$Vin = \frac{154.5*4.2*10^{-5}}{(1.5*4.2*10^{-5}+0.8*10^{-5})0.16} = 571V \quad (33)$$

$$Vac = 0.84*\frac{4.2*10^{-5}*154.5}{(1.5*4.2*10^{-5}+0.8*10^{-5})2*0.16} = 415V \quad (34)$$

With the Equations (33) and (34) we are able to perceive that any modification in supply voltage will built variant in DC link side voltage and alteration with boost factor able to maintain AC output side voltage constant. DC link set to 571 V and AC line voltage set to 415 V. The assessment between reference and actual value produces the error signal. These error signals initiate the closed loop system operation and it's given to PI controller.

PI controller transfer function is:

$$G(S) = K_p + \frac{K_i}{s}$$

The Proportional and Integral gain (K_p and K_i) ranges are evaluated by using Zieglers-Nichols scheme. This technique is incorporated in step response system. This system nature is normalized by two different parameters, time constant (Tp) and delay time (Lp). These parameters are calculated by sketching a tangent at the point of intersection in the step response and intersections with time axis. Thus the steady state value noted is shown in Figure 9. In the same way the error signal generated in output side voltage is processed through PI controller.

Step function to the system applied to predict the output response and L_p and T_p has been calculated. The calculated $L_p = 1$ and $T_p = 0.004$, for this the K_p and K_i are 0.3 and 0.1 respectively. Bode plot has been drawn to examine stable condition and it is revealed in Figure 10. Here gain margin posses positive value and the phase margin shows infinite value. Thus the system is a stable system. In conventional UPS 20% of variation in battery voltage makes wave shape distortion in inverter output voltage. The suggested UPS showing glorious voltage regulation even with 50% voltage droop in battery bank voltage. At 100% battery bank voltage (i.e. 154.5 V) the UPS produces inverter side output AC voltage of 415 V and it is exposed in Figure 11. In 50% of battery voltage (78 V), the AC side output voltage wave shape is not distorted because of Improved TZSI action and it's shown in Figure 12. Total Harmonic Distortion of UPS voltage is revealed in Figure 13. The UPS voltage THD is restricted to 0.60%. Figure 12 showing some second order harmon-

ics, this will be eliminated by selecting higher rating of capacitive filter.

The proposed UPS competency level with the conventional UPS has been calculated for different KVA ratings. It is plotted in Figure 14. It is noted that the suggested UPS has exhibited 10% greater efficiency than that of conventional UPS.

Table 1. Simulation circuit parameters for proposed UPS

System Parameters	Values
V_{LAC} -Three phase AC line voltage	114.4 V
fs - Switching frequency	10 KHz
T -Total Switching period	5×10^{-5}
T1-Active Period	4.2×10^{-5}
T0-Shoot Through Period	0.8×10^{-5}
C1, C2 and C3- Capacitors	33 µF
N1- Inductor1 Winding	108 turns
N2- Inductor2 Winding	72 turns
K- coupling coefficient	0.998
K_p, K_{p1} and K_{p2} - Proportional gain	0.05, 0.03 and 0.03
Integral gain	0.1
Star connected R load	3 KW
M- Modulation index	0.84
d (Boost mode) - duty ratio	0.16
n- Turns Ratio	1.5
f- Fundamental AC frequency	50 Hz

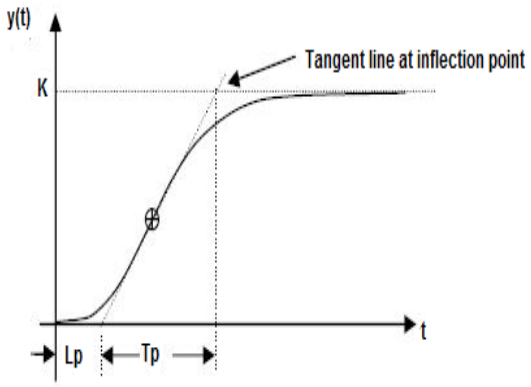


Figure 9. Zieglers-Nichols method.

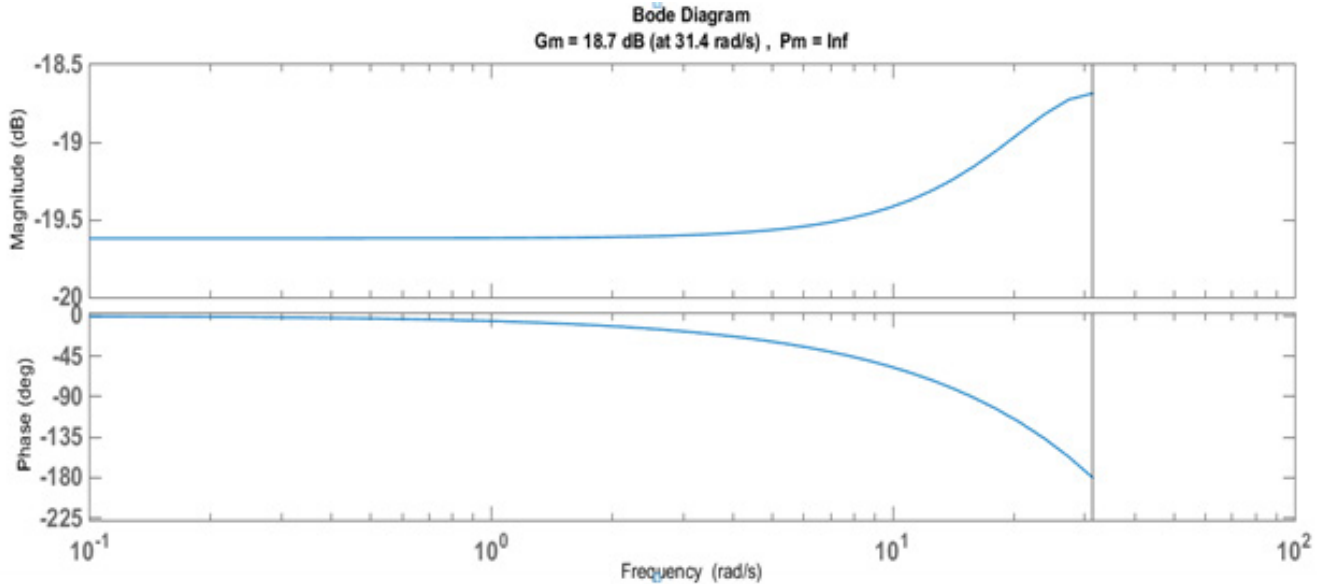


Figure 10. Bode plot for stability analysis.

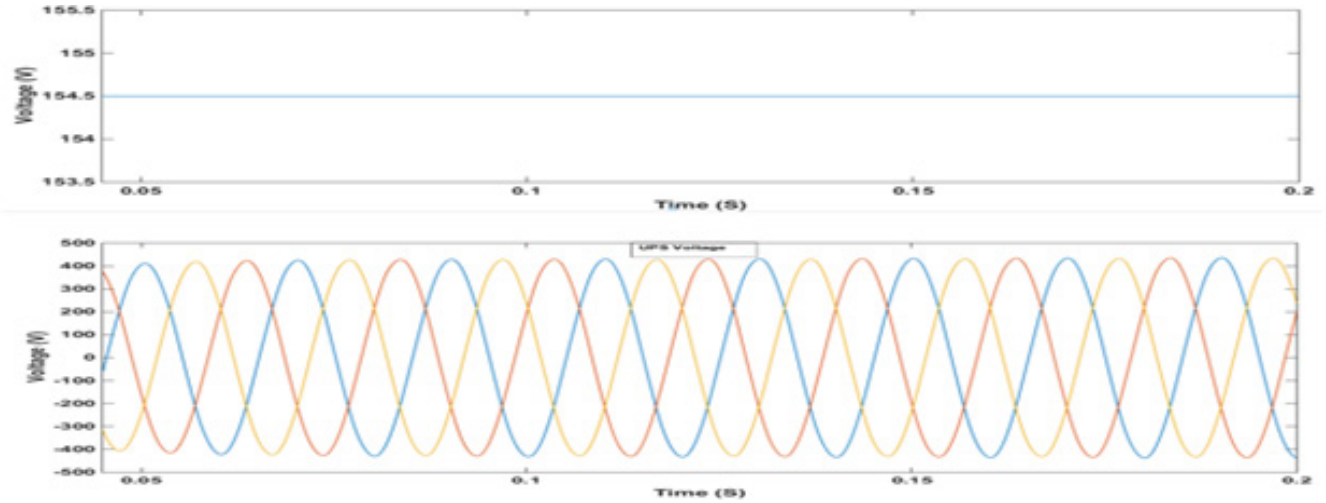


Figure 11. 100% battery voltage vs. AC response.

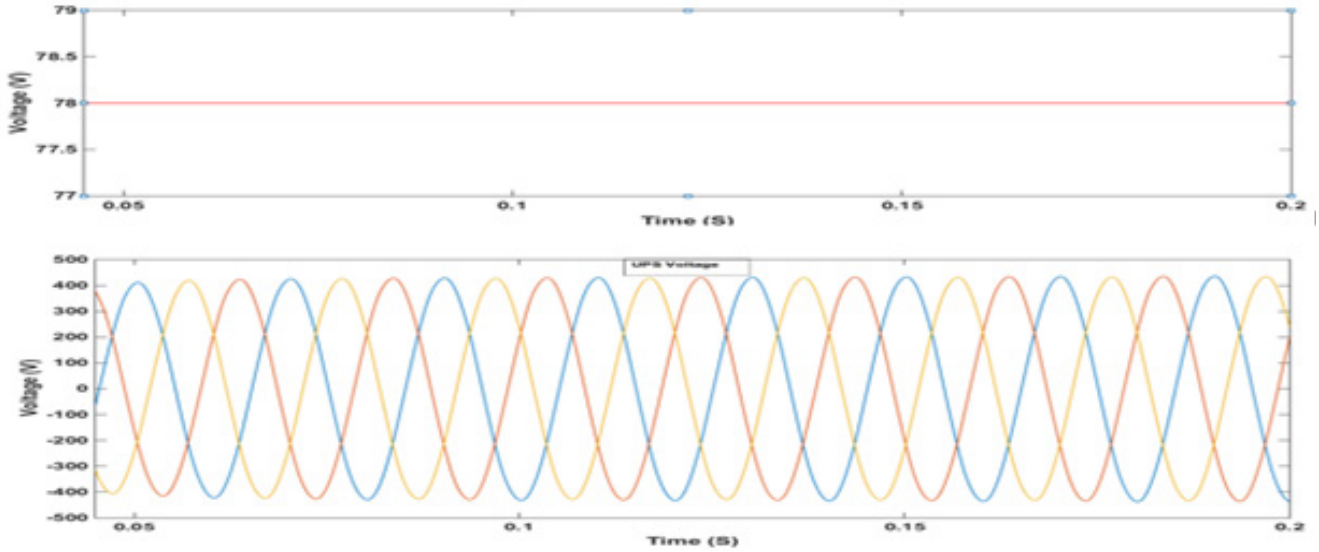


Figure 12. 50% battery voltage drop vs. AC response.

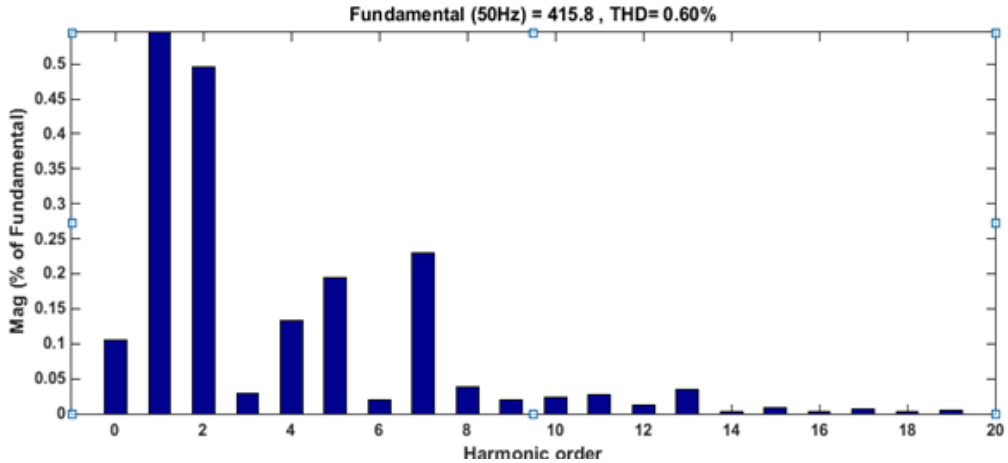


Figure 13. UPS output voltage FFT analysis.

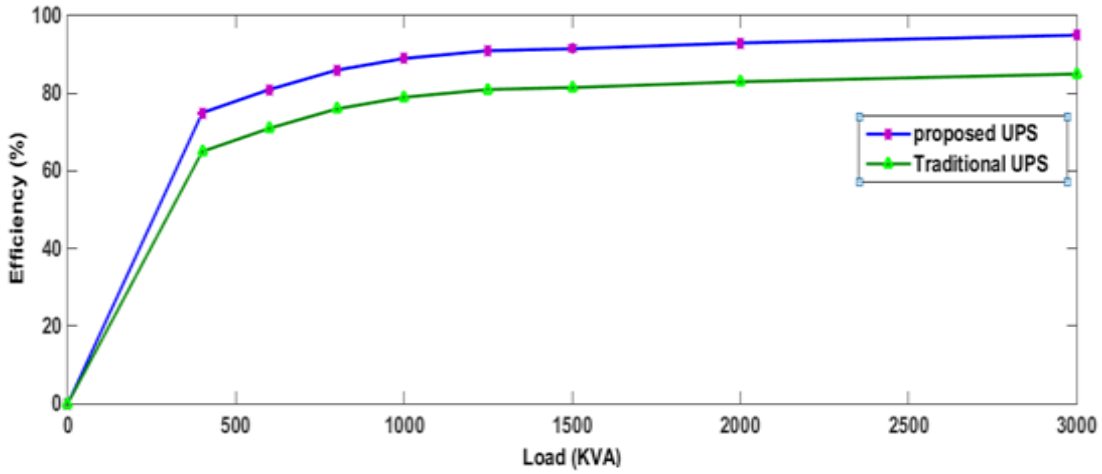


Figure 14. Proposed and traditional UPS efficiency.

5. Hardware Implementation

To validate the simulation result, experimental setup for NTZSI has been deliberated for 3 KVA load capacity. This setup consists of NTZSI impedance network, power circuit and feedback circuit shown in Figure 15(a). The PWM pulses for IGBT (FGA25N120AN) have been generated using ARDUINO software. The coding is embedded into the ATmega328 chip. 1 KHZ switching frequency has been chosen. The chosen shoot though period T0 and T1 are 0.8 x 10^{-4} and 4.2 x 10^{-4}. The simulated value of d and M are considered.

The inverter is designed for 3.7 boost factor and output AC voltage value of 415 V using Equation (35) and (37). The Equation (38) shows the expected AC line voltage value of inverter.

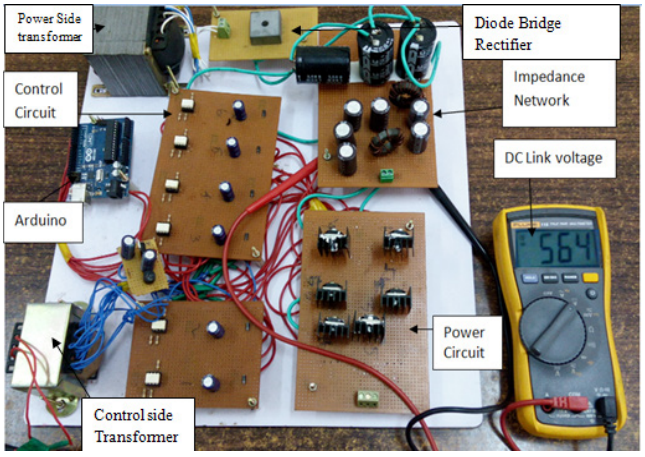
$$B = \frac{T1}{(nT1+T0)d} == \frac{4.2}{(1.5*4.2+0.8)0.16} = 3.7 \quad (35)$$

$$Vi = B*Vdc = 3.7*154.5 = 571V \quad (36)$$

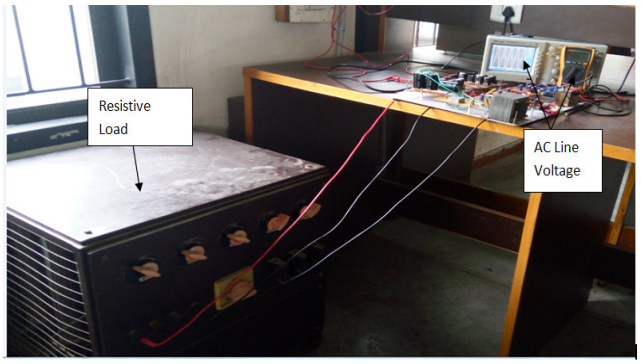
$$Vac = M*B*Vdc/2 = 0.84*3.7*154.5/2 = 240.09V \quad (37)$$

$$Vacl = \sqrt{3} \times 240.09 = 415V \quad (38)$$

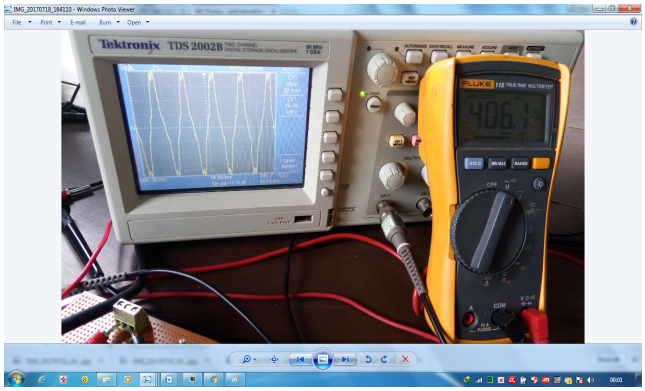
The Hardware implementation outcomes are shown in Figure 13 (b) and (c). During this obtained DC link voltage is 564 V and AC line voltage is 406 V. Table 2 shows the comparative results between theoretical estimation and experimental results of NTZSI. It is observed that Experimental results are closely are closely intact with the theoretical estimation.



(a)



(b)



(c)

Figure 15. Hardware implementation of NTZSI showing (a) Hardware setup, (b) DC link voltage, (c) AC line voltage.

Table 2. Comparative results between theoretical estimation and experimental results

	DC link Voltage	AC line Voltage
Simulation Results	571 V	412 V
Experimental Results	564 V	406 V

6. Conclusion

A brand new improved TZSI has been introduced in this paper. This inverter finds its appliance in three phase UPS for the load capacity of 3 KW. Once the load of traditional UPS raises the drop across the battery bank voltage directs to deficient AC voltage generation at the inverter. The ZSI based UPS resolves this trouble by regulating the shoot through time interval at the inverter side. However this inverter cannot produce enough voltage under high modulation index conditions and it desires long shoot through time interval. This raises stress across the device. In contrast to traditional ZSI UPS, the planned UPS can sustain at high modulation index condition with terribly less shoot through time interval amount and also the transformer winding turns demand is very less with this inverter. This reduces the prize and weight of the system. Here quick transient response and superior steady state performance is achieved by twin-loop control management. Simulation has been executed in MATLAB/ Simulink platform.

7. References

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