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Energy Efficient ARABIC Unicode Reader Design on FPGA

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Abstract

Objectives: This paper proposes an Energy Efficient ARABIC Unicode Reader design on FPGA. **Methods/Statistical Analysis:** Two types of energy efficient techniques such as Frequency Scaling and FPGA technology scaling have been used to make the device energy and power efficient. In the frequency scaling technique the frequency of device has been varied from 1MHz to 1THz; whereas, in FPGA scaling technique the power consumption of the device at two FPGA technologies(Artix-7 and Virtex-6) has been compared in order to identify the most energy efficient technology at least power consumed frequency. **Findings:** In this Unicode reader, results have been analyzed using X Power Analyzer. Different types of tables have been created for different range of frequencies showing different power dissipation values. It has been observed that 99.67% of total power can be saved in case of Artix-7 while operating the device at a frequency of 1MHz instead of 1 THz and in case of Virtex-6 98.5% of total power can be saved while operating the device at a frequency of 1MHz instead of 1 THz. So it has been concluded that more amount of power has been dissipated in case of Virtex-6 FPGA technology in which the length of channel is 45nm in comparison to Artix-7 in which length of channel is 28nm. Also it is advisable to operate the device at a low range of frequencies in order to have less power consumption. **Application/Improvements:** Conclusions drawn from the analysis will be helpful in making the device more power efficient as compared to the existing ones. It comes out to be a step towards Go-Green Mission in order to serve the humanity.

Keywords: Energy, FPGA, Frequency, Green Computing, Power, Unicode Reader, Xilinx

1. Introduction

Unicodes are a type of standards used for representing and encoding for writing and reading systems. The recent version of Unicode includes a range of more than 128,000 characters. Unicode provides universal code for every character. Initially Unicode was designed for 16 bit encoding space, consists of 256 rows of 256 characters each 1.2. Unique number of codes is provided for every character irrespective of the code and platform is provided 3.4. Unicode is an easy way to represent any character. The effect of Islamic religion made alphabets of ARABIC as one of the very most prevalent written structure of countries, and are bringing into different

parts of African and Western and Central Asian regions. ARABIC language is used frequently in ethnic communities in East Asia, Europe and Americas. Arabic alphabet is also used for writing different languages like Persian Urdu and many more. Arabic is a middle Semitic communication to be firstly spoken in Iron age. It is named after the Arabs. Arab is a word originally used to depict people living from Mesopotamia in the east to the Anti-Lebanon Mountains in the west.

The Arabic Unicode Reader consists of 16-bit hexa decimal codes for Arabic digits, Arabic Symbols, Extended Arabic Letters, Koranic Annotation. Range allocation of few words of Arabic Unicode scripts is shown in Table 1. Frequency scaling energy efficient technique and FPGA

technology scaling energy efficient technique has been used in order to make the Unicode reader an energy efficient device.

Table 1. Range Allocation of few words of Arabic Unicode Scripts

Hexadecimal code	Arabic letter
0600	Arabic Sign NUMBER
0601	Arabic SANAH SIGN
0602	Arabic FOOTNOTEMARKER
0603	Arabic SAFHA
0604	Arabic SAMVAT
060D	Arabic DATE SEPARATOR
06D4	Arabic FULLSTOP

Large amount of work has been done in this field of energy and power efficiency to contribute towards Green Computing. Work has already been done on different energy efficient techniques like thermal scaling technique⁵ by making significant change in temperature and capacitance scaling technique in which capacitance of the device has been varied from 1pF to 25pF. Researchers have also worked on voltage scaling technique^Z in which voltage has been scaled from 3V to 1V in order to make device energy and power efficient. Frequency scaling technique has also been employed on Malayalam Unicode reader⁸ by varying the frequency from 1MHz to 1THz using Virtex-6 and Spartan-6 FPGA technologies. Many researchers had also worked on different Unicode readers like Kannada Unicode reader² and Devnagri Unicode reader¹⁰ in which the results of 28nm FPGA technology has been compared with 40nm technology in order to discard the most energy hungry FPGA technology. Different clock gating techniques are also applied in order to make an energy efficient Gurmukhi Unicode reader¹¹. In order to save the power consumption in digital circuits, energy and power efficient techniques have also been applied on many digital circuits like FIR Filter¹², Solar Charge System¹³ and Counter Design¹⁴.

2. Experimental Setup

The design of Arabic Unicode reader is implemented on Xilinx ISE 14.6 Project Navigator. X Power Analyzer has been used for the survey of the power dissipation at different frequency levels. 5 D Flip-flops and 20 Slice LUT's are used by the software for the designing of an Arabic Unicode reader. The schematic of an Arabic reader is shown in Figure 1 it takes 16-bit hexadecimal code and a clock as an input. At the output port it can show any of the six outputs. If alphabets are not amongst the range of Arabic Unicode reader then the output shown is a Not Valid Sign otherwise it will show the corresponding output according to the Arabic input.

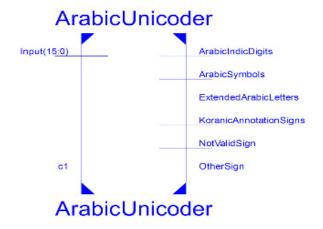


Figure 1. Schematic of Arabic Unicode Reader.

3. Result Analysis by X Power Analyzer

3.1 Analysis of Clock Power

Virtex 6 Analysis: It has been shown in Figure 2 that power dissipation is almost negligible if the frequency range is set to 1 MHz or 10 MHz or 100 MHz instead of 1THz and almost 99.99% power can be saved. But if we operate at a frequency of 1GHz in place of 1THz then 99.90% power is saved. On operating the device on 10GHz of frequency then almost 99% of power is saved and if frequency is set to 100GHz instead of 1THz then 90% of power is saved.

Artix 7 Analysis: It has been analyzed from Figure2 that power dissipation is almost negligible if the frequency range is set to 1MHz or 10 MHz or 100MHz instead of 1THz then almost 99.99% power is saved. But if we operate at a frequency of 1GHz in place of 1THz then 99.8% power is saved. On operating the device on 10GHz of frequency then almost 99% of power is saved and if frequency is set to 100GHz instead of 1THz then 90% of power is saved.

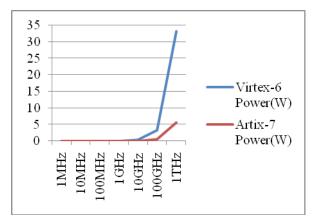


Figure 2. Clock Power Dissipation at VIRTEX-6 and ARTIX-7.

3.2 Analysis of Logic Power

Virtex 6 Analysis: It has been shown in Figure 3 that power dissipation is almost negligible if the frequency range is set to 1MHz or 1GHz or 100MHz instead of 1THz and almost 97.52% power is saved. But if we operate at a frequency of 1GHz in place of 1THz then 98.34% power is saved. On operating the device on 10GHz frequency range almost 98.3% of power is saved and if frequency is set to 100GHz instead of 1THz then 88.4% of power is saved.

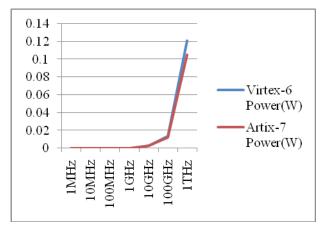


Figure 3. Logic Power Dissipation at VIRTEX-6 and ARTIX-7.

Artix 7 Analysis: It has been shown in Figure 3 that power dissipation is almost negligible if the frequency range is set to 1 MHz or 10 MHz or 100 MHz instead of 1THz and almost 96.1% power can be saved. But if we operate at a frequency of 1GHz in place of 1THz then 97.1% power is saved. On operating the device on 10GHz of frequency then almost 98.09% of power is saved and if

frequency is set to 100GHz instead of 1THz then 88.5% of power is saved.

3.3 Analysis of Signal Power

Virtex 6 Analysis: It has been shown in Figure 4 that power dissipation is almost negligible if the frequency range is set to 1 MHz or 10 MHz or 100 MHz instead of 1THz and almost 99.84% power can be saved. But if we operate at a frequency of 1GHz in place of 1THz then 99.89% power is saved. On operating the device on 10GHz of frequency then almost 98.9% of power is saved and if frequency is set to 100GHz instead of 1THz then 89.9% of power is saved.

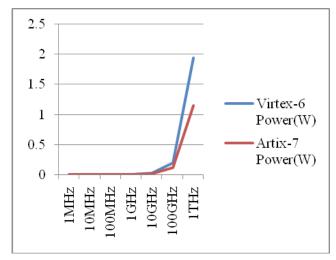


Figure 4. Signal Power Dissipation at VIRTEX-6 and ARTIX-7.

Artix 7 Analysis: It has been shown in Figure 4 that power dissipation is almost negligible if the frequency range is set to 1 MHz or 10 MHz or 100 MHz instead of 1THz and almost 99.73% power can be saved. But if we operate at a frequency of 1GHz in place of 1THz then 99.65% power is saved. On operating the device on 10GHz of frequency then almost 98.95% of power is saved and if frequency is set to 100GHz instead of 1THz then 89.94% of power is saved.

3.4 Analysis of IO Power

Virtex 6 Analysis: It has been shown in Figure 5 that power dissipation is almost negligible if the frequency range is set to 1 MHz or 10 MHz or 100 MHz instead of 1THz and almost 99.9% power can be saved. But if we operate at a frequency of 1GHz in place of 1THz then

99.8% power is saved. On operating the device on 10GHz of frequency then almost 98.99% of power is saved and if frequency is set to 100GHz instead of 1THz then 90% of power is saved.

Artix 7 Analysis: It has been shown in Figure 5 that power dissipation is almost negligible if the frequency range is set to 1 MHz or 10 MHz or 100 MHz instead of 1THz and almost 99.98% power can be saved. But if we operate at a frequency of 1GHz in place of 1THz then 99.89% power is saved. On operating the device on 10GHz of frequency then almost 98.99% of power is saved and if frequency is set to 100GHz instead of 1THz then 89.99% of power is saved.

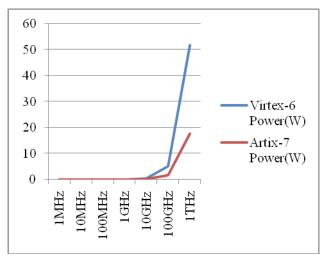


Figure 5. IO Power Dissipation at VIRTEX-6 and ARTIX-7.

3.5 Analysis of Leakage Power

Virtex 6 Analysis: It has been shown in Figure 6 that power dissipation is almost negligible if the frequency range is set to 1 MHz or 10 MHz or 100 MHz instead of 1THz and almost 20.8% power can be saved. But if we operate at a frequency of 1GHz in place of 1THz then 20.69% power is saved. On operating the device on 10GHz of frequency then almost 19.65% of power is saved and if frequency is set to 100GHz instead of 1THz then 6.85% of power is saved.

Artix 7 Analysis: It has been shown in Figure 6 that power dissipation is almost negligible if the frequency range is set to 1 MHz or 10 MHz or 100 MHz instead of 1THz and almost 89.91% power can be saved. But if we operate at a frequency of 1GHz in place of 1THz then 89.91% power is saved. On operating the device on 10GHz of frequency then almost 89.79% of power is saved and if frequency is set to 100GHz instead of 1THz then 88.56% of power is saved.

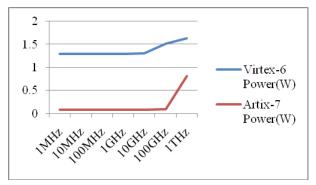


Figure 6. Leakage Power Dissipation at VIRTEX-6 and ARTIX-7.

3.6 Analysis of Total Power

Virtex 6 Analysis: It has been shown in Figure 7 that power dissipation is almost negligible if the frequency range is set to 1 MHz or 10 MHz or 100 MHz instead of 1THz and almost 98.5% power can be saved. But if we operate at a frequency of 1GHz in place of 1THz then 98.44% power is saved. On operating the device on 10GHz of frequency then almost 97.53% of power is saved and if frequency is set to 100GHz instead of 1THz then 88.46% of power is saved.

Artix 7 Analysis: It has been shown in Figure 7 that power dissipation is almost negligible if the frequency range is set to 1 MHz or 10 MHz or 100 MHz instead of 1THz and almost 99.67% power can be saved. But if we operate at a frequency of 1GHz in place of 1THz then 99.57% power is saved. On operating the device on 10GHz of frequency then almost 98.69% of power is saved and if frequency is set to 100GHz instead of 1THz then 89.94% of power is saved.

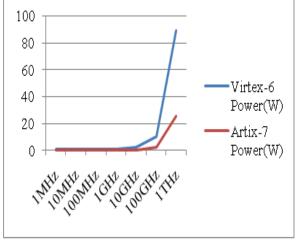


Figure 7. Total Power Dissipation at VIRTEX-6 and ARTIX-7

4. Conclusion

By changing FPGA technology and frequency, there is change in power dissipation. Different types of graphs are created for different range of frequencies showing different power values as already explained in detail above. Using different types of frequencies, it is concluded that more amount of power is saved in case of Artix-7 as compared to Virtex-6 while operating at a frequency of 1MHz instead of 1 THz. So it is advisable to operate the device on Artix-7 in which length of the channel is 28 nm FPGA technology instead of Virtex-6 in which length of the channel is 40 nm. Also it is always better to operate the device on the lowest range of frequencies so that minimum amount of power dissipation is there.

5. Future Scope

In this project Arabic Unicode reader is implemented on ISE Project Navigator and power of the device has been analyzed on X-power Analyzer. The power analysis can also be done for other language Unicode readers such as Tamil, Telugu, Gujrati, Devnagri etc. This design has been executed on Virtex-6 and Artix-7 FPGA. There is wide platform to re-execute this Unicode reader design on the latest ultra scale technology FPGA like ZYNQ. Also many other energy efficient techniques can be applied such as thermal scaling, capacitance scaling, and voltage scaling in order to make the device energy economical.

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