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BCD Adder Design using New Reversible Logic for Low Power Applications

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Abstract

Objectives: Proposed a novel GDI (Gate Diffusion Input) based low power BCD adder to improve the performance further compared with existing BCD adder design using BBCDC reversible gates. **Methods/Analysis:** Reversible logic is one of the potential techniques observed for low power designs having lot of research scope in the fields of nanotechnology, which involves with quantum computing. One major advantage of reversible logic is its low power capability. The power dissipation, speed, circuit density are the main concerns of research today. The proposed GDI cell based BBCDC reversible logic is implemented using Microwind 2, with 120nm technology. **Findings:** The proposed GDI based BBCDC reversible adder is proved that there is 91.5% of reduction in delay, 80.7% of reduction in power dissipation, 64.58% of reduction in logic overhead, and 93.88% of reduction in area when compared with the CMOS logic. The design goal is to minimize PDP, in order to get low power with high-speed advantage. **Novelty /Improvement:** The proposed GDI based BCD adder using reversible logic results in 98.38% of PDP advantage over existing designs, hence more reliable with extended performance.

Keywords: Area, BCD Adder, CMOS Logic, Figure of Merit, GDI Technology, Reversible Logic

1. Introduction

Reversible logic is an interesting area, which is highlighted due to its involvement in numerous technological design implementations. It is one of the potential techniques in the field of nano scale engineering where power dissipation reduction is a major criteria. The existing technologies are more prone to the heat dissipation, which is a major disquiet from the point of designer as well as end user. When the designer introduces a new design, as example mobiles, which include highly scalable technology may use impractical and in adequate range of parameters such as voltage or temperature. The major advantage of any design with reversible logic is complete reduction of power dissipation, which results in zero heat-generated products.

Investigations based on irreversible logic shows that the energy lost on every bit of information is kTln2 joules; where T is absolute temperature and k is Boltzmann constant.[1] Such energy lost would not occur if the process uses reversible method.[2] This is because the amount of energy that is dissipated has a direct connection with the number of bits that are erased during the computation. This result in a circuit with reversibility technique, in which any bit of information will not lose energy while employing the reversible computation, where as the reversible computation is performed using reversible gates.[3,4] Despite of their large area, reversible gate designs are proved their low power advantage compared to their counter designs using CMOS logic.

The important measuring parameters for logic design using reversible gates includes the number of gates used for the design with less number of unused outputs also called as garbage outputs. The optimized design also concerned about minimum number of inputs, which are left constant. The crucial design aspect for reversible logic lies in reduction of number of unused outputs because the accumulation of garbage by at least single digit causes an exhaustive and excessive execution of the circuit. Hence, a very important design aspect of reversible logic is to use less number of garbage bits.

One of the design aspects behind reduction of garbage outputs is to use large number of gates in the circuit design. Dynamic programming is the one that allows

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the user with lowest garbage count during the synthesis step. Circuit that uses Toffoli and Fredkin reversible gates results in minimal garbage. Switches that use "don't cares" also results in minimal garbage. Quantum technologies are the one that may use reversible logic. An example of complex antenna simulation design in which reversible logic is implemented in hidden but may not be seen as a separate logic. However, the importance of simulation reveals the reversible transformation in the process of propagating a wave.

Brief on implementation and design of BCD adder using conventional as well as reversible logic design is discussed in Section 2 Materials and Methods. Section 3 discuss about design implementation of BCD reversible adder using proposed GDI logic as well as conventional CMOS logic. Comparisons of obtained results are presented in Section 4, and finally, ended with conclusions in Section 5.

2. Materials and Methods

In this paper, BCD adder is implemented in two ways primarily using logic gates in traditional way and the same using reversible logic Gates, the corresponding flowchart shown in Figure 1 represents algorithm steps required.[5-8]

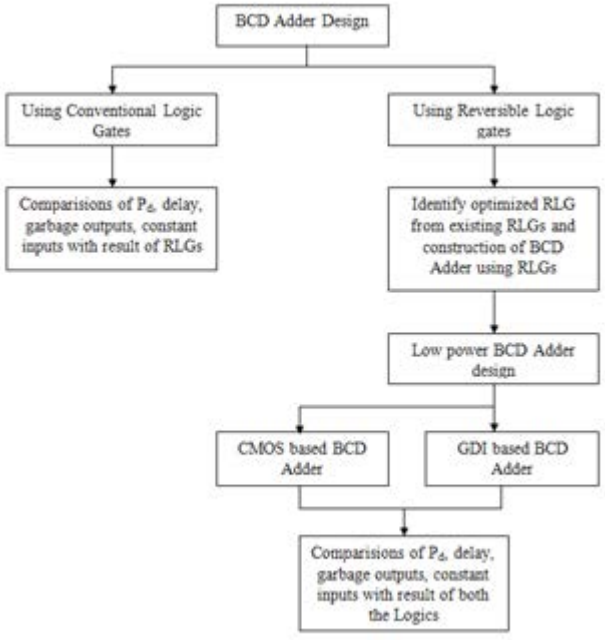

Figure 1. Flowchart.

2.1 Traditional BCD Adder

The traditional BCD adder is implemented by considering logic gates as shown in Figure 2. It uses two 4-bit adders and one correction circuitry in which OR and AND Gates were used.

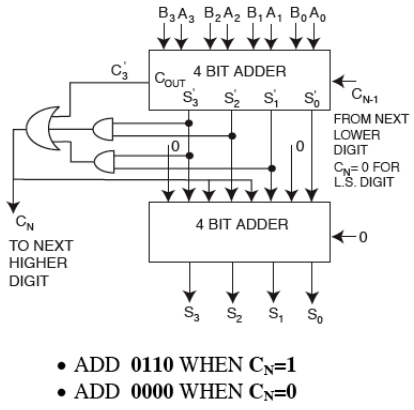

Figure 2. Conventional BCD Adder.

2.2 Design of BCD Adder using RLG

Reversible Logic Gates (RLG) is differentiated based on their complexity and input/output relation. Basic RLG's exists with sizes from minimum 2x2 to maximum 5x5 input/output combinations. The proposed work considered three types of RLG's namely HNG, TSG and BBCDC for the design of BCD adder.[5]

2.2.1. HNG Gate

A HNG (Hybrid New Gate) is a basic RLG gate, which uses four variables for input/output combinations as shown in Figure 3. The best implementation of this gate is ripple carry adder since using single gate itself it produces sum as well as carry output hence reduces the number of garbage and gate counts.

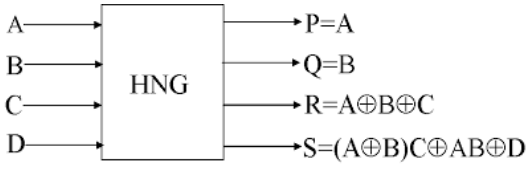

Figure 3. HNG 4x4 Gate.

2.2.1 TSG Gate

Figure 4 shows TSG gate implementation for full adder. If the input C is made zero then the circuit acts like a full

adder and the output R gives the sum and the output S gives the carry out.

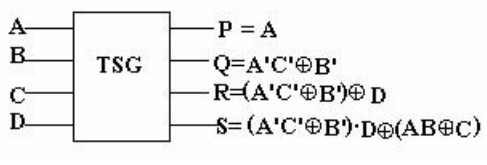

Figure 4. TSG 4x4 Gate.

2.2.3. BBCDC Gate

A BBCDC (Binary to BCD conversion) is a 5X5 reversible gate shown in Figure 5, is used in the implementation of BCD adder.[9] Table 1 shows the corresponding input/output vectors.

Design of BCD adder using reversible BBCDC gates is shown in Figure 6, which requires a minimum of nine inputs A_{0-3}, B_{0-3} and five outputs in which four bits are for sum bits S_0, S_1, S_2, S_3, and C_{out}.[5-17] Four bits are required to code the augends, which makes eight bits, and including circuit carry bit it makes the nine bits input.

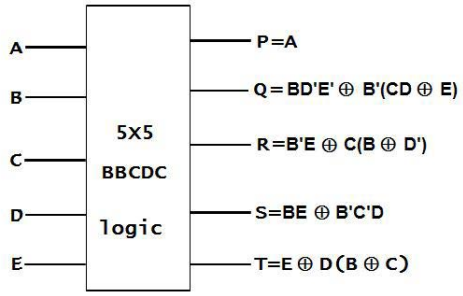

Figure 5. BBCDC 5x5 Gate.

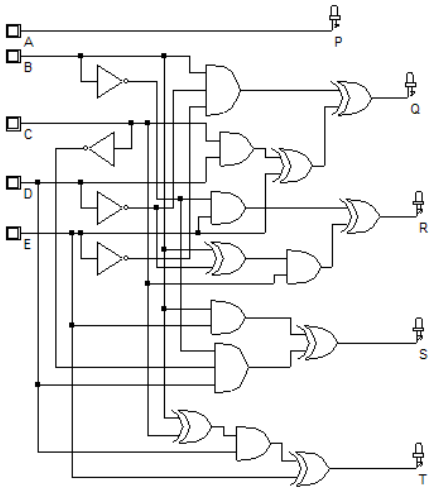

Figure 6. BBCDC 5x5 Gate.

Table 1. Truth table of BBCDC Gate

Inputs					Outputs				
E	D	C	B	A	T	S	R	Q	P
0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	0	0	1	0
0	0	0	1	1	0	0	0	1	1
0	0	1	0	0	0	0	1	0	0
0	0	1	0	1	0	0	1	0	1
0	0	1	1	0	0	0	1	1	0
0	0	1	1	1	0	0	1	1	1
0	1	0	0	0	0	1	0	0	0
0	1	0	0	1	0	1	0	0	1
0	1	0	1	0	1	0	0	0	0
0	1	0	1	1	1	0	0	0	1
0	1	1	0	0	1	0	0	1	0
0	1	1	0	1	1	0	0	1	1
0	1	1	1	0	1	0	1	0	0
0	1	1	1	1	1	0	1	0	1
1	0	0	0	0	1	0	1	1	0
1	0	0	0	1	1	0	1	1	1
1	0	0	1	0	1	1	0	0	0
1	0	0	1	1	1	1	0	0	1

Consider adding 9+9+1 in decimal, gives 19, in straight binary this should produce an output of 10011_2, but this is an invalid number in BCD. Because in BCD code the four bits binary which only represents decimal numbers 0-9. Table1 shows decimal numbers 0-19 with their binary and BCD codes.

3. Proposed BCD Adder using GDI Logic

The proposed GDI based BCD adder uses all reversible gates in terms of GDI cells and is shown in Figure 7. This technique replaces variety of intricate logics implementation with few transistors. Since the design needs less number of transistors, results in fast and low power circuits. The technique uses small cell library with top down design approach, which improves logic level along with static power at reduced number of transistors. The basic contradiction between the former and traditional CMOS logic are as follows:

- Gate G is a common input connected from both the controls of complemented P & N transistors,
- N diffusion input formed from source of n transistor
- P diffusion input formed from drain of p transistor

In this, diffusions of n & p transistors can be randomly biased unlike in CMOS inverter, in which P diffusion is always given supply voltage V_{DD}. However, in GDI technique, the input terminals N, P and G terminals could be given one of these values: a supply 'V_{DD}', or ground, or supplied with input signal depends on the requirement of circuit design. This lowers the transistors count in the implementation of the logic circuits such as AND, OR, XOR, MUX, etc. However, this achieves at the cost of low voltage swing and hence this GDI technique is suitable for low voltage as well as low power applications. Basic cell structure of GDI is shown in Figure 8. The following section briefs on few GDI based gate designs.[15]

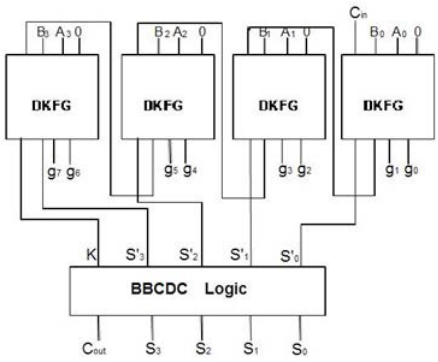

Figure 7. Proposed BCD Adder.

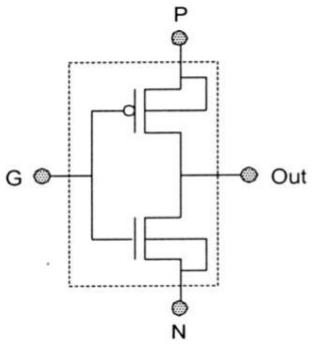

Figure 8. GDI basic cell.

3.1 AND Gate

GDI based AND gate needs only two transistors contrast to CMOS based AND which needs 6 transistors for its implementation, and is shown in Figure 9.

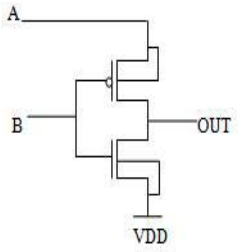

Figure 9. GDI based AND Gate.

3.2 OR Gate

GDI based OR gate needs only two transistors contrast to CMOS based OR which needs 6 transistors for its implementation, and is shown in Figure 10.

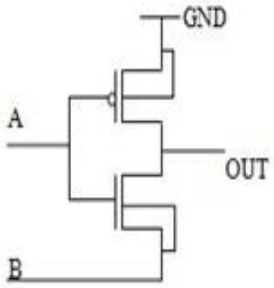

Figure 10. GDI based OR Gate.

3.3 XOR Gate

GDI based XOR Gate needs only 4 transistors contrast to CMOS based XOR which needs 12 transistors, and is shown in Figure 11. Further, these GDI based basic gates are used in the construction of proposed reversible logic gate design of BCD Adder.

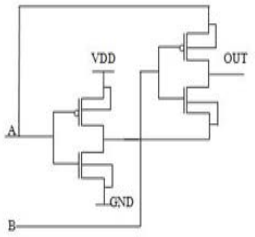

Figure 11. XOR Gate.

4. Results and Comparisons

Initially BCD Adder using reversible logic was implemented in gate level for the design proposed by resulted with more delay compared to in spite of less number of reversible gates.[9,16,17] Further, the performance of existing design is improved by implementing using GDI cells and compared with the traditional CMOS Logic.

Table 2 shows the values observed for conventional BCD adder using gate level structure. The same is implemented using CMOS and GDI techniques using transistor structures. As shown in Table 3, GDI logic is advantage in resulting low power, low delay and low area. Hence, this technique is used in implementing reversible BCD adders for further reduction of power and delay.

Table 2. Parameters observed for Conventional BCD Adder using logic gates

Parameters	Conventional BCD Adder(gate level)
Delay (ns)	2.180
Power dissipation (mw)	0.226
Number of Logic gates	24
Area (μm^2)	1572.5
PDP / figure of merit (pJ)	0.492

Table 3. Comparisons between CMOS and GDI based BCD adder design parameters

Parameters	BCD adder (using Transistor Level)	
	BCD Adder using CMOS logic	BCD Adder using GDI logic
Delay (ns)	6.350	0.998
Power dissipation (mw)	0.252	0.103
Number of transistors	320	108
Area (μm^2)	17063.7	2818.8
PDP / figure of Merit (pJ)	1.600	0.103

From the Table 4, out of comparison, design using observed with few unused outputs and stable valued inputs.[5] Further, observed that only few reversible logic gates were required and hence reduced the area. In spite of these, delay and hence figure of merit are increased. To overcome this, finally GDI logic at transistor level is used.

It is observed from Table 5, the proposed GDI cell based BBCDC reversible logic is proved that there is 91.5% improvement in speed, 80.7% of reduction in power dissipation, 64.58% of reduction in logic overhead, 93.88% of reduction in area, and 98.36% of improvement in figure of merit was observed when compared with the CMOS logic design. Figure 12 shows the proposed GDI based BCD adder. Figure 13 shows the delay comparison between existing and proposed BCD GDI based BCD adder. It is found that the design using CMOS logic reached a maximum delay of 10ns whereas using GDI it is just below 1ns. Figure 14 shows the variation in power dissipation among existing and the proposed design. The maximum power dissipation by CMOS logic reached up to 250uW, where as using GDI it is greatly reduced to 100uW. As a result, average energy per switching activity also reduced as shown in Figure 15. Hence, one can say design using reversible logic is more reliable with extended performance than the existing.

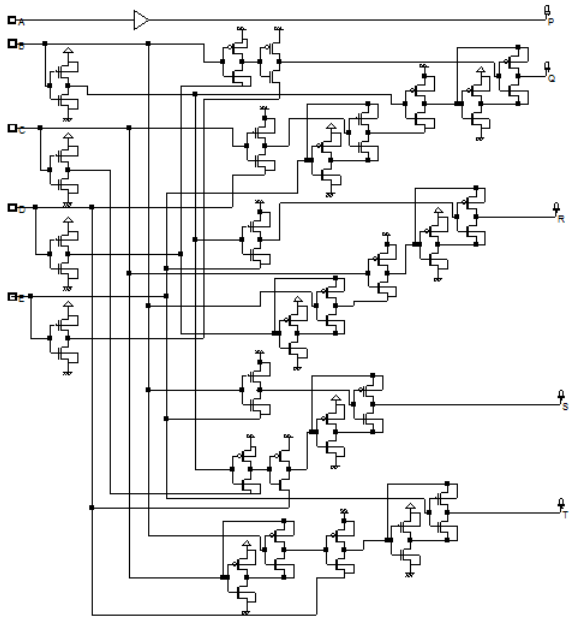

Figure 12. GDI based BCD adder using BBCDC reversible gates.

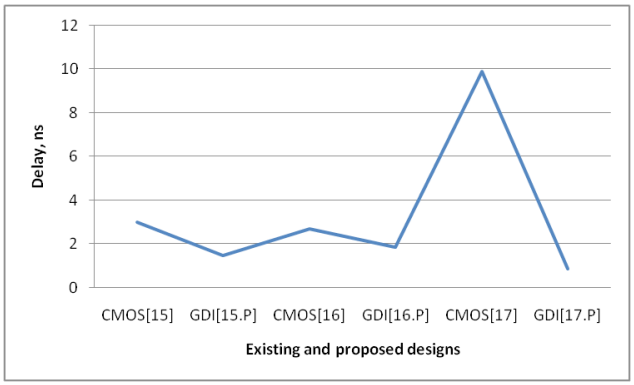

Figure 13. Delay comparison.

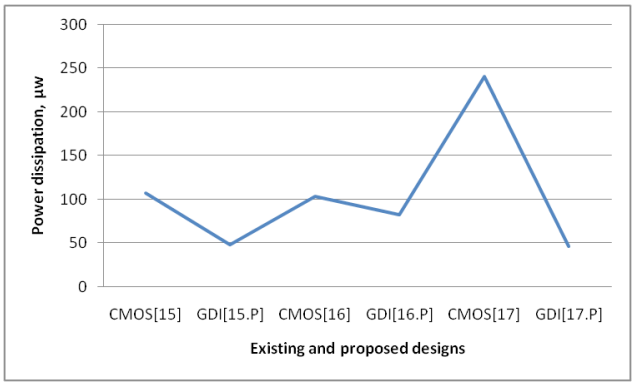

Figure 14. Power dissipation comparison.

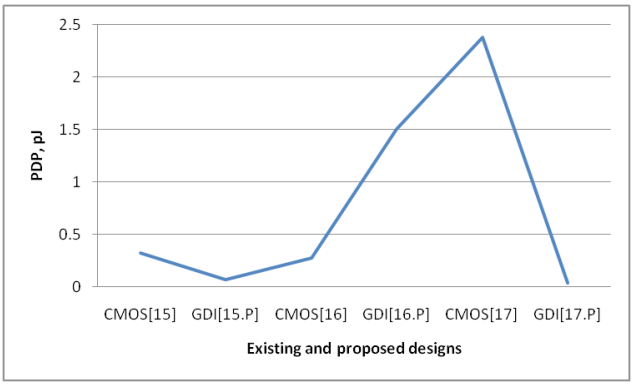

Figure 15. PDP comparison.

Table 4. Parameters observed for BCD Adder using reversible logic [15], [16], and [17]

Parameters	BCD adders using reversible Logic (Gate Level)		
	BCD Adder using reversible logic HNG gate [15]	BCD Adder using reversible logic TSG gate [16]	BCD Adder using reversible logic BBCDC gate [17]
Delay (ns)	0.545	0.960	2.530
Power dissipation, (mw)	0.126	0.104	0.237
Garbage outputs	10	11	8
Constant inputs	6	7	8
Reversible gates	8	9	5
Area (μm^2)	11869.6	2861.8	2201.6
PDP / figure of Merit (pJ)	0.068	0.099	0.599

Table 5. Proposed GDI technique for BCD Adders and comparisons with CMOS logic [15], [16], and [17]

Parameters	reversible Logic (using Transistor logic)								
	BCD adder using HNG[15]			BCD adder using TSG [16]			BCD adder using BBCDC [17]		
	CMOS	GDI	% improve	CMOS	GDI	% improve	CMOS	GDI	% improve
Delay (ns)	2.98	1.45	51.34	2.65	1.815	31.5	9.870	0.835	91.5
Pd, (µw)	108	48.19	55.37	104	82.8	20.38	241	46.52	80.7
#Transistors	366	122	66.66	498	198	60.2	384	136	64.58
Area (μm^2)	11378.3	4119.5	63.79	15167.1	6877.9	54.65	17063.7	1043.5	93.88
PDP / figure of Merit (pJ)	0.32	0.069	78.57	0.276	0.15	45.6	2.379	0.038	98.36

5. Conclusion

Low power BCD adder was implemented using BBCDC reversible logic. Different parameters such as number of unused outputs, constant inputs, delay, area, number gates used, power, and PDP are compared for different BCD adder logic designs. The proposed GDI based reversible BCD adder is more reliable and optimized with extended performance compared to existing designs.

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