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Dual Recycled Charge Power Gating For Retaining Data and Saving Leakage

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Abstract

Objectives: To innovate power gating technique which is used to recycle charge lost at moment from active to sleep mode by both PMOS header and NMOS footer. **Methods:** Three 32-bit Carry Look Ahead (CLA) adder circuits and ISCAS-85 benchmark circuits are compared in retention mode including the conventional power gating, single recycled charge power gating, dual recycled charge power gating in term of the power consumption using the 45 nm Predictive Technology Model. A fair timing comparison also is considered in this work. **Findings:** This proposed 32-bit CLA adder can reduce the standby leakage power consumption up to 60% and 53% in short and long sleep time, respectively, compared to the conventional power gating. Compared to the single recycled charge, the proposed saves up to 25% in short sleep time and 44% in long sleep time. The proposed 32-bit CLA adder is simpler in controlling the circuit in active mode and retention mode. The ISCAS-85 benchmark circuits are also applied to make conclusion in term of saving leakage power consumption. **Application:** This proposed leakage reduction technique is promising candidate for optimizing more leakage dissipation in digital circuits.

Keywords: Charge Recycling, CLA Adder, Leakage Current, Low Power, Power Gating

1. Introduction

Leakage current has become one of the most important factors for low power applications. Leakage current is the first concern when conducting these IC design applications.[1] Power Gating (PG) technology is used in many IC designs to reduce the leakage currentbelow.[1,2] Here, an NMOS switch which is high voltage threshold, is conventionally used to turn-off the low voltage threshold logic gate circuits.[1,2] Dual power gating using both PMOS header and NMOS footer to cut off power lines has been revisited3. The comparison results tell us that dual power gating is higher energy-efficiency compared to single switch power gating.[3]

Among various power gating techniques, charge recycling has been considered as an effective technique to reduce the leakage current.[4] By doing so, the switching power is recycled at the moment from active to sleep and sleep to active. Theoretically, the total power consumption can be saved to 50% during the switching time.[5] However, data output will be lost in long sleep time because the virtual V_{SS} node will be charged to nearly V_{DD} during sleep time. To maintain data without loss, the retention mode is configured during sleep time. A Diode-connected PMOS that is applied to clamp the virtual V_{SS} node voltage is often used to keep data output in power gating techniques.[6,7] The researchers give efforts to not only recycle power in reducing total power consumption but also maintain data output without loss.[8,9] A recycled charge technique which can recycle charge loss and retain data output is required for lower power consumption designs.

The CPU processor operations consist of addition, subtraction, multiplication, and comparison which use the adder unit as a basic component to generate results.

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Moreover, almost DSP processors and embedded systems use adders in the ALU structure to design data paths in IC chips. On average, 60% of operations take place in the tasks using the adder unit.[10, 11] Ripple Carry Adder (RCA) is the simplest candidate of an adder. However, the RCA is very slow. The performance of this implementation is the result of a long delay data path. The Carry Look Ahead (CLA) Adder is an alternative solution for this problem.

In this paper, we are applying the new concept of the dual recycled charge in power gating technique to 32-bit Carry Look Ahead (CLA) adder which is being used widely in various IP cores such as CPU, multiplier, DSP, etc. By using this dual charge recycling technique, we achieve low power consumption and still preserve data in sleep mode. We power off the 32-bit CLA adder to reduce the leakage dissipation but still remain the data output by this dual charge recycling PG technique. The ISCAS-85 benchmark circuits are also applied to make conclusion in term of leakage power consumption.

2. A Comparison in Three Data Retention Power Gating Schemes

Figures 1 (a) and (b) show two power gating schemes which are the conventional PG and single recycled charge PG. Firstly, the conventional PG shown in Figure 1 (a) has one logic block with MN0 and MP0. Here, MN0 switch plays a role as a power gating switch that can turn on and off the power supply. The PGN signal controls logic block to normal operation mode at PGN of high logic level and sleep operation mode at PGN of low logic level. The PMOS switch, MP0, is inserted between virtual VSS1 and VSS that is operated as a diode. This diode-connected PMOS is used to maintain the data before the logic circuit enters sleep mode and loses data. In active mode, the HLD/PGP is applied to low level to turn on this PMOS. In sleep mode, the VVSS1 node is charged and its node voltage will be clamped to high threshold voltage level of this PMOS.

Figure 1 (b) illustrates the single recycled charge PG scheme. The SLP signal controls MN1 to enable whether VVSS2 node is connected to NSW node or not. In active mode, SLP signal is low level which turns on MP1 then leads to turn on MN2. As a result, the VVSS2 node is connected to VSS. Then, source gate of MN2 is connected to VSS as well. Thus, the 32-bit CLA is in normal operation. The NSW node is kept at high level during active mode. Before the circuit moves to sleep mode, NSW node voltage still is high. In sleep mode, SLP signal is high, and then MN2 switch is turned off. At the moment when the circuit is going to the sleep mode, a charge sharing phenomenon happens between NSW node and VVSS2 node instantaneously. The high voltage of NSW node is shared with low voltage of VVSS2 node. By doing so, the VVSS2 node will be charged to voltage level where amount of the charge is balanced at both the NSW node and VVSS2 according to principle of charge sharing and charge balance. Amount of the recycled charge makes VVSS2 node charge up quickly. The VVSS2 node gets saturated to threshold voltage level of MN1. In sleep mode, NSW node and VVSS2 are connected through MN1. Figure 1 (c) shows dual recycled charge schemes are applied to dual power gating switches. Amount of loss charge due to turning on/off switches can be recycled at both MP3 PMOS and MN3 NMOS.

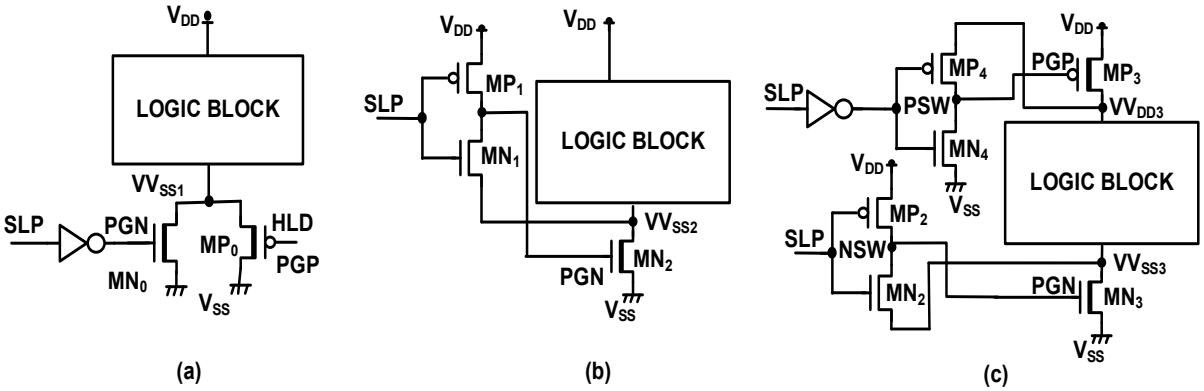


Figure. 1. **(a).** The conventional power gating; **(b).** The single recycled charge power gating; **(c).** The dual recycled charge power gating.

Figure 2 (a) shows waveforms of critical path delay in active time. The critical delay path is illustrated to calculate the longest delay time of 32-bit CLA adder. Here, an input vector set of A<0:31>="1s" and B <0:31>="0s" is applied to the 32-bit CLA adder. The Carry-out bit is generated by Carry-in bit and the above input vector set as shown in the Figure 2 (a). As a result, a delta (Δ) delay determines the longest path delay time of the 32-bit CLA adder.

Figure 2 (b) shows timing waveforms of the conventional PG from active to sleep time and sleep to active time. Here, the SLP signal is inverted to connect to the gate terminal of MN0 through an inverter. In active mode, the HLD signal is high. In otherwise, the HLD signal is low in sleep mode. When MN0 switch is turned-off to disconnect ground line, the VVSS1 node is charged up steadily by leakage current from VVSS1 to VSS. However, the increase at VVSS1 voltage node will be clamped by the diode-connected MP0 switch. Thus, the output state is retained to threshold voltage level during sleep mode.

Figure 2 (c) shows the timing waveforms of the single recycled charge PG technique. In active mode, the SLP is low, MP0 is turned on, then NSW node is pulled up to high voltage and its charge is stored at VDD. On the contrary, the SLP is high, MN1 is turned-on in sleep mode. Instantaneously, the stored charge is shared from NSW node to VVSS2 node through the MN1 that makes VVSS2 go up rapidly at active to sleep moment. The amount of stored charge at NSW node is shared to raise VVSS2 node up. At moment of charge balance in this sharing phenomenon, the VVSS2 node is kept at a certain voltage level and the data output is maintained without loss.

Figure 2 (d) shows the voltage level at VVDD3 and VVSS3 when circuit falls in sleep mode and active mode. Here, the recycled charge happens to both header and footer switch at switching moment from active to sleep mode. It means that a large amount of lost charge can be recycled at the switching moments from active to sleep mode and vice versa. At active to sleep moment, the VVDD3 is going down quickly to threshold voltage of MP4 and VVSS3 is going up quickly to threshold voltage of MN2 because of charge sharing with PSW and NSW, respectively. Both nodes get saturated at a certain voltage level to maintain data without loss during sleep time. Here, MN2 and MP4 have larger channel width than the others to make active speed same with the conventional PG and single CRPG. Thus, voltage swing on both header and footer is smaller than that on only single footer. Amount of switching power at active to sleep and sleep to active moment can be saved due to this smaller voltage swing.

3. Simulation Results

We are not aware of an AR system specifically aimed at helping autistic children interact with strangers but there is one specific system made to encourage pretend play in autistic children, which proved that a system whose major interaction was through a screen is successful and is used with ease by the child.

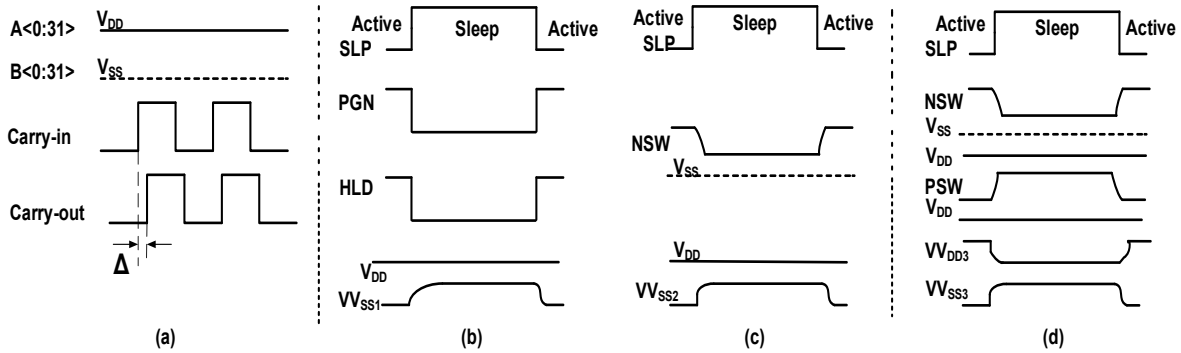


Figure 2. (a). Waveforms of critical path delay during active time **(b).** Virtual ground waveforms of the conventional PG at active to sleep time **(c).** Virtual ground waveforms of the single recycled charge PG from active to sleep time and vice versa **(d).**Virtual ground waveforms of dual recycled charge PG from active to sleep time and vice versa.

In this section we present the simulation results of the conventional 32-bit CLA circuit and the single recycled charge 32-bit CLA circuit. We have implemented this simulation with 45nm Predictive Technology Model11 and the supply voltage at 1.1V.

Figure 3 shows comparisons of critical path delay of the 32-bit CLA adder at the conventional PG, the single recycled charge PG, and dual recycled charge PG. Here, critical path delay is defined by time difference between Carry-out and Carry-in signal as analyzed in Figure 2 (a). The critical path timing delay ( ) is simulated as in Figure 3. We assess the delay timing of these three schemes to have a fair comparison in the leakage power consumption of various PG techniques. The channel width of NMOS switches is designed at 12% total channel width of 32-bit CLA logic block (shown as A line). The grey dashed line named A illustrates the timing delay of 32-bit CLA adder at switch area of 12% total channel width. Based on the Figure 3, we can realize the timing delay relatively equal in two cases of the conventional PG and single recycled charge PG.

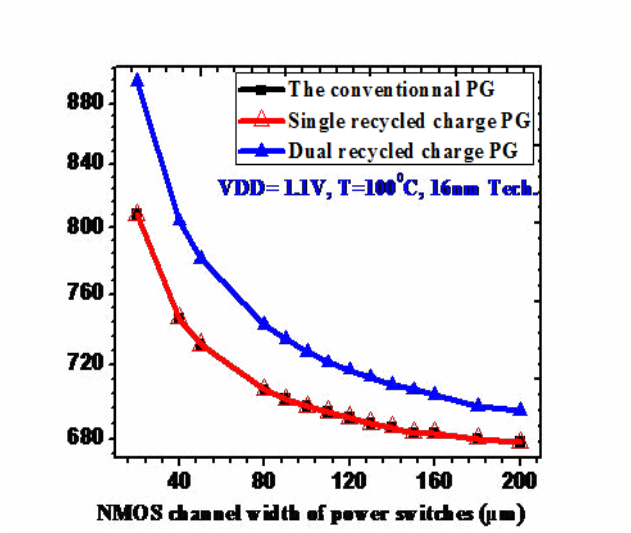


Figure 3. Comparison of critical path delay of 32-bit CLA in the conventional PG and the single recycled charge power gating and dual recycled charge power gating at temperature of 27 oC. A named line is designed at NMOS switch of 12% total channel width of 32-bit CLA adder.

This is because these two schemes use same size of NMOS footer to switch ON/OFF the power lines. Dual recycled charge is implemented by both NMOS and PMOS switch, thus critical path delay is a little slower than others. To have a fair comparison in term of critical path delay, we have to re-size the NMOS footer and PMOS header in case of dual recycled charge. A grey dashed line cross critical timing delay curves illustrates that if NMOS switches of the conventional PG and single recycled charge PG is designed at 100 µm (12% total channel width of 32-bit CLA), that of dual recycled charge PG should be 180 µm at least. It means that PMOS switch should be 360 µm. Then, this effective channel width (W effective) of dual recycled charge PG is

W effective = W NMOS footer + ½ W PMOS header.

It leads that power switches occupy 43% total channel width of 32-bit CLA. Thus, the dual recycled charge PG has 21% area overhead compared to the conventional and charge recycling PG.

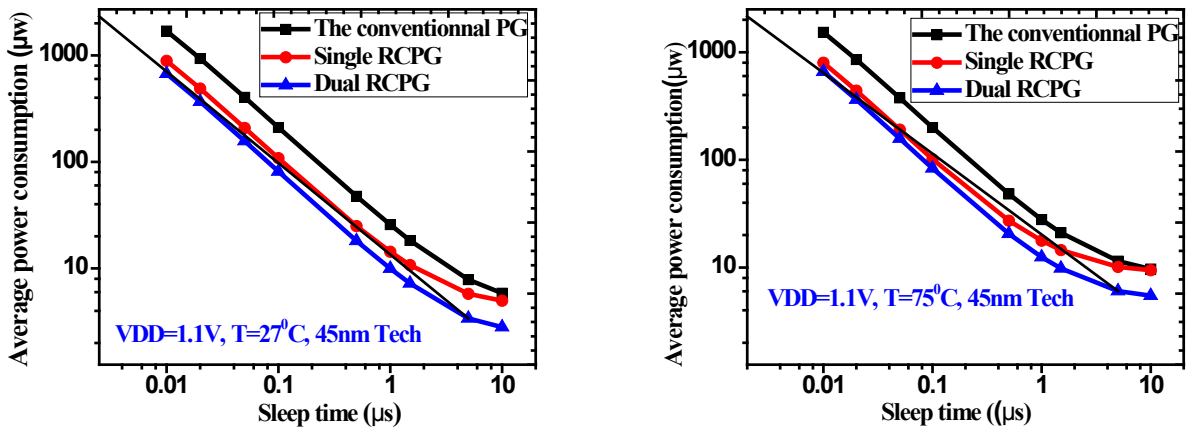
After ensuring that delay timing is approximately equal in active time among three schemes. Figure 4 (a) shows amount of power consumption of the 32-bit CLA adder power according to various sleep times at temperature of 27oC. At short sleep time of 0.01µs, the conventional PG consumes 1690µW, the single recycled charge PG only consumes 889µW, while dual recycled charge PG is 671µW for average consumption power. At long sleep time of 10 µs, amount of power consumption is 5.9 µW, 5 µW, 2.8 µW for the conventional PG, single recycled charge PG, dual recycled charge PG, respectively. Here, active time is much shorter than sleep time. In detail, the active time is analyzed at pulse width of 0.005µs. Thus, we can be noted that the total power dissipation can be considered as the portion of only leakage power. This dual RCPG realizes a 60% and 53% saved power consumption than the conventional PG and SRCPG in short sleep time and long sleep time, respectively. Compared to single recycled charge PG, dual RCPG saves up to 25% and 44%, in short sleep time and long sleep time, respectively.

Similarly, Figure 4 (b) shows the advantage of the dual RCPG compared to the conventional PG and single RCPG to various sleep times at temperature of 75oC. In case of short sleep time at 0.01µs, the conventional PG consumes 1530µW, the single RCPG consumes 798µW, while dual RCPG is 659µW for average power. It realizes a 48% and 18% saved power consumption than the conventional PG and single RCPG in short sleep time, respectively. When sleep time is as long as 10 µs, the dual RCPG can save up to 44% and 42% compared to the conventional PG and single RCPG, respectively. The Figure 4 (b) illustrates that the single RCPG tends to approach the conventional PG, while the dual RCPG can get more advantages in term of saving leakage power in long sleep

time. This is because body effect of dual RCPG happens to both PMOS and NMOS switches instead of only NMOS switch in the conventional PG and single recycled charge PG. Thus, the leakage power of dual RCPG is suppressed much more than the conventional PG and single RCPG.

ISCAS-85 benchmark circuits consisting of C432, C499, and C880 are analyzed in comparison of power consumption at different sleep times as shown in Table 1. Here, power consumption values are normalized according to power consumption of the dual RCPG. The percentage of saved power depends on various sleep times. As seen in Table 1, the average consumption power of the dual RCPG can be saved in short sleep time more than in long sleep time. This is because charge sharing phenomenon just happens at the moment from active to sleep time. Thus, a large amount of average consumption power can be saved at short sleep time. For an example of C432, C449 and C880 benchmark circuit, the average consumption power of dual recycled charge PG is 75%, 76%, 75% lower than the conventional PG. When sleep time is long, the percentage of our advantage is up to 57.5%, at temperature of 27oC and the sleep time of 0.01µs.

One more thing is realized that that the conventional PG scheme uses the diode- connected-PMOS to retain data in sleep time. By doing so, the conventional PG has its area overhead compared to the two other the 32-bit CLA adders to implement this retention mode. Moreover, the conventional PG needs a HLD signal to control the MP0 -PMOS switch as shown in Figure 1 (a). It means that the conventional PG increases complexity of design



(a) (b)

Figure 4. Power consumption of 32-bit CLA according to various sleep times.

Table 1. Comparison results of the dual recycled charge PG (DCRPG) compared to the conventional PG (CPG) and single recycled charge PG (SCRPG) at 27oC, 45nm PTM on blocks. Normalized values are shown as following

Time (µs)	C432			C499			C880		
	CPG	SC RPG	DC RPG	CPG	SC RPG	DC RPG	CPG	SC RPG	DC RPG
0.01	3.98	1.37	1	4.16	1.37	1	3.97	1.35	1
0.1	3.97	1.31	1	4.18	1.35	1	4.03	1.32	1
1	3.45	1.33	1	3.66	1.4	1	3.59	1.43	1
5	2.65	1.61	1	2.74	1.55	1	2.81	1.69	1
10	2.35	1.71	1	2.41	1.61	1	2.53	1.78	1

compared to the single recycled charge and the proposed CLA adder.

4. Conclusion

In this paper, we have applied a dual recycled charge power gating technique to the 32-bit CLA adder scheme to retain the logical state during sleep period. We have compared the three power gating 32-bit CLA schemes in term of power consumption with a fair timing comparison. This proposed 32-bit CLA adder can reduce the standby leakage power consumption up to 25% in short sleep time and 44% in long sleep time compared to single recycled charge, and up to 60% in short sleep time and 53% in long sleep time compared to the conventional PG. The simulation results are implemented at 45nm PTM, VDD=1.1V. The ISCAS-85 benchmark circuits are also applied to make conclusion in term of leakage power consumption.

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