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Extensible On-Chip Interconnect Architecture and Routing Methodology for NOC

Y. L. Ajay Kumar[1], D. Satyanarayana[2] and D. Vishnu Vardhan[1]

[1]Department oF E.C.E, Jawaharlal Nehru Technological University Anantapur, Anantapur – 515002, Andhra Pradesh, India; ajaykumarphd@gmail.com, Vishnu.ece@jntua.ac.in
[2]Department of E.C.E, Rajeev Gandhi Memorial College of Engineering and Technology, Nandyala – 518501, Andhra Pradesh, India; dsn2003@rediffmail.com

Abstract

Network-On-Chip (NOC) plays an important role in improving the performance of multi-core systems. **Objectives:** This paper proposes an alternative architecture for Networking-On-Chip which will improvise the Routing Efficiency of Network-On-Chip. **Methods/Statistical Analysis:** In the presented alternative architecture, we used a routing technique which uses Agents which are designed and made as a part of routing logic. We designed Hand-shake and multi-point packet injection systems. **Findings:** We introduced a Global routing mechanism and Temperature parameters in the design. This design is scalable to Hetero-generous and Homogeneous networks, it is power efficient. The experimental results reduces the Area, Power and Latency, And increases the Efficiency of the system. **Application/Improvements:** Routing efficiency for Heterogeneous Mp**SOC**.

Keywords: Agents, Global Routing, Network On Chip (NOC), Processing Elements, Routing Techniques

1. Introduction

To meet the growing computation-intensive applications with the quick development of promoting Nano-meter technology reducing transistor dimensions continuously results to allow designers to integrate high number of processors on a chip. NOC share many signals that are linked with more wires. Comparison of different proposals and options are needed for the development of NOC. Point -to - point communications are not suitable to design NOC because of poor flexibility. Within the large multi-core systems the NOC emerges the scalable and promising solutions for global communications. NOC have advantages like more flexibility, large bandwidth to communications. Earlier, packets are transmitted on packet switching connections against long setup delay of circuits. On the whole chip NOCs accounts for high ratio of total power consumption. Here we proposed a novel routing architecture, which will improve the efficiency of NOC. Even though the current network technologies are well developed and their supporting features are excellent, their complicated configurations and implementation complexity make it hard to be adopted as an on-chip interconnection methodology. Though the network technology in computer network is already well developed, it is almost impossible to apply to a chip-level intercommunication environment without any modification or reduction. For that reason, many researchers are trying to develop appropriate network architectures for on-chip communication.On the other hand, to apply the prevailing mobile environment; it should be low-powered. In order to be low powered one has to consider many parameters such as clock rate, operating voltage, and power management scheme. Future NOCs need to overcome the limiting factor of on-chip interconnections such as Physical constraints (which reduces functional unit utilization and slows down inter-communication), Limited bandwidth inter-resource,

* *Author for correspondence*

Inefficient synchronization schemes, Access-pattern-dependent throughput, Inability to hide the latency of the internal network, Poor parallel-computing models and Energy consumption.

2. Objective

In the design of NOC, processing elements, Agents, Routing architecture plays an important role. The presented paper main objective is to improvise the routing efficiency in a 3*3 mesh Network on Chip (NOC). In fact, Here we split the router logic and distribute them among the processing elements. In processing elements we have agents and core logic, which will perform the generation of router inside the processing element itself. The main job of the processing element is to route the packets by having the awareness of the state of neighboring elements. Sothat we can remove the router in NOC and we can design Router free architecture for the NOC. In this section, we discussed in detail about the Router free architecture for NOC. In the next following we arrange like in Chapter 2 Related work, In Chapter 3 Existing Work, In Chapter 4 Proposed architecture, in chapter 5 Experimental results and finally Chapter 6 with Conclusion and Future Scope.

While designing NOC's, We are having several issues to be concerned with, like Routing algorithms, topologies, performance, latency, complexity etc., If we take topology we have different topologies like 2D tours, C-tours, Butterfly etc. The only difference is that the switches at the edges are connected to the switches at the opposite edge through wrap-around channels. In[1] have proposed the OCTAGON MP-SOC architecture with a basic octagon unit consisting of eight nodes and 12 bi-directional links. Each node is associated with a processing element and a switch. Communication between any pair of nodes takes at most two hops within the basic octagonal unit. In virtual circuit switching, which is a combination of both circuit switching and packet switching. Here by proper control of virtual channels, network flow control can be easily implemented[2]. Also to increase the fault tolerance in network, the concept of virtual channel has been utilized[3-4].

In order to obtain a high throughput, low computing latency system on a chip, this paper proposes a new congestion sensing and control methods: a congestion controlling dynamic routing method based on dynamic routing Table[5]. To overcome fault problems, conventional fault-tolerant routing algorithms employ fault information and buffer occupancy information of the local regions. However, the information only provides a limited view of traffic in the network, which still results in heavy traffic congestion. To achieve fault-resilient packet delivery and traffic balancing, this work proposes a Path-Diversity-Aware Fault-Tolerant Routing (PDA-FTR) algorithm, which simultaneously considers path diversity information and buffer information[6]. In this paper it is stated that[7], requirements such as network infrastructure standardization and compatibility are less restrictive in NOC projects, where only end nodes need standardization. Then, NOC projects tend not to follow an implementation pattern, with their customized architectures for applications and SOC designs. Mathematically NOCs are modeled and simulations are carried out to evaluate the performance of the NOC[8]. All these simulations are dependent on assumptions which limit their accuracy to some level. Hence hardware implementations using applications specific ICs and FPGAs are used to create the prototype to model the NOC in physical level. In comparison to ASICs, FPGAs offer less implementation cost and more design flexibility.

In one of the architecture the concept of borrowing the buffers from the neighbor channels which are not in use at particular time is used. It decreases the large buffer depth requirement. This architecture improves the overall performance of the router. The proposed architecture allows reconfiguring the different buffer size for each channel. According to the need of the buffer depth the neighboring channel occupies the empty buffers of that channel. By using the empty buffer slots of the neighbor connection cost gets reduced. In such a way each channel may have up to three times more buffer slots than its original buffer with the size defined at design time[9]. Two fault-tolerant routing algorithms were presented which improve the NOC throughput performance for complex traffic conditions under fault patterns[10]. Two representative general purpose NOC implementations (virtual channel and simple physical channel) to demonstrate how real applications would perform under a range of network loads[11]. FPGAs and reconfigurable computing allow users to configure and combine pre-existing IP to create complex designs. From this work, it is clear that the chosen configuration of a network on chip greatly determines whether a design will meet area and performance constraints.

Table 1. Area Efficiency Benchmark Report

ROUTER	XY	OBL	NOP	RCA	PACR	PROPOSED ROUTING
Max. Frequency(G.Hz)	0.80	0.71	0.63	0.63	0.63	0.62
Avg. Throughput(Gbps /node)	2.41	2.71	2.78	2.94	3.18	3.25
Area Efficiency(Gbps/node/mm^2)	41.12	42.04	43.84	47.95	55.70	56.66
Total Area(nm^2)	58.61	64.09	64.48	61.27	57.08	57.00

3. Existing System

In NOCs, Routers plays an important role in communicating between two (or) more IP's (Intellectual Property) (or) Processing Elements (PE)[12]. If Processing Elements are more, then data to the Router is more, and queuing is more at the Router and there will be more chances to lose the data (or) information, For that purpose we need buffer, like these we have a lot of problems, such as, The systems route the packets without awareness of the state of the neighboring elements, Temperature of the given core is not taken into consideration and hence, there are possibilities of processing elements will be overloaded if more packets are routes toward it, Routers should implement complex routing algorithms for transfer unprocessed packets to other processing elements. It takes additional logic and routing and power costs are increased thus paving way for congestion and loss of data packet though it solves one problem of routing efficiently. Too many connections and ports per processing element can be inferred from above solutions. This will have direct effect on speed of operation and causes congestion thus affecting the throughput. Moreover it is difficult achieve a good FPGA implementation with the above flaws as they will lead to routing congestion and timing problems[13]. Since lot of implementation effort goes into routing in FPGA, logic utilization cannot reach 100% in many of the FPGA families, If the core processing logic needs to be changed, the routing paradigm has to change every time. Scale-up modality is weak, if the packet for any reason does not get processed, it is not sent back to the host. It is lost. Because of this, even though some of the architectures proposed have achieved high bit rate, there is an equally high rate of data loss. Some of the other problems include, Energy performance, having complex algorithms in the router will require many decisions to be made and thus a lot of transitions. More connections are another reason which will affect energy performance. Critical path, Caused due to heavy logic of the routers. Cross talk, though not much of a problem in FPGA, number of connections can create crosstalk. Timing violations and slack, Place and route during implementation of the design either for FPGA or ASIC can create setup and hold violations. It should also be noticed that most proposals are simulation based and thus there is a great need to analyze many of the situations discussed above should be researched through implementation strategies.

How deadlock situations can be manages has not been addressed. Though many papers focus on the internals of the NOC routing, very less importance is given to the hosts that use the NOC to achieve certain tasks and how they can utilize the NOC resources. A perspective study from the external circumstances should be made. Such as how data rates can be addresses as the NOC processing rate and input data rate and output read out rate can be different, How multiple applications can run in a given NOC is not addressed, How to balance the load amongst the network elements is not addressed, Many NOCs are targeted to a specific technology and they are rigid in their configuration demanding a minimum size of the FPGA. The elements should be designed such that we can configure the number of processing elements based of the FPGA. Mechanism for knowing the internal environment in the NOC is done by Routers which is in Figure 1.

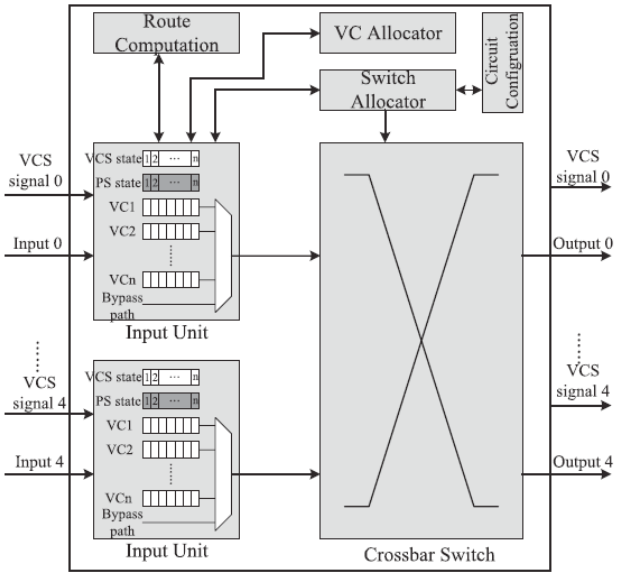

Figure 1. Architecture of Router Using Cross Bar Switch.

4. Proposed Efficient Routing 3*3 Mesh Network on Chip(NOC)

In this approach,we can attempt to improvise most of the problems by incorporating the following characteristics in the design and carefully tweaking it to achieve the objectives. For all practical purposes, we will use a 3x3 NOC matrix with a simple cryptography functional core. In which, Split the router logic and distribute them amongst the processing elements[14]. The above said logic can consist of agents that can separately handle input packets and output packets. A separate input bus and output bus will handle the incoming and outgoing packets. Improvise data framing by adding more informative headers. This will help recognize the packets belonging to multiple applications or the process status of each packet. Provide a global line so that farthest elements can be accessed easily without hopping. This alone solves complex routing algorithms in routers. Provide buffers. This will make up for the data rate mismatch issues. Provide global write-in, read-out and flush logic for neat load balancing[15]. Provide handshake protocol based data transfer between processing elements. Consider the temperature co-efficient for transfer of data packets between elements. Design by keeping in mind the scalability and heterogeneous nature of some applications. This means that each block should with minimal change should be capable of implementing different core logic. Make processing elements self contained so that they can be individually controlled. This helps in scalability and when not required they can be turned off so that power can be saved. To meet the above points, here we are Realizing the design considering the above said point using Verilog RTL Design. Developing appropriate test bench to inject packets and analyze them. A fully functional model of NOC in Verilog to be simulated and synthesized. NOC will be implemented using a 3x3 Mesh topology. A functional core will implement the simplified AES algorithm. Round robin algorithm will be used to scan various ports. Control logic will be implemented to synchronize the functions of agents and core logic. Measure the area, power, speed, frequency and other parameters such as: throughput, injection rate, latency, performance on various FPGA families, etc.

5. Experimental Results

In the proposed method we tested 3*3 mesh network is in Figure 2. The NOC architecture contains Processing Element, Agents, Buffers and Core Logics, which we already discussed in previous sections. Figure 3. 3*3 mesh Network and whole experimental work is completed by using Xilinx 14.4 version and verified on different FPGA families.

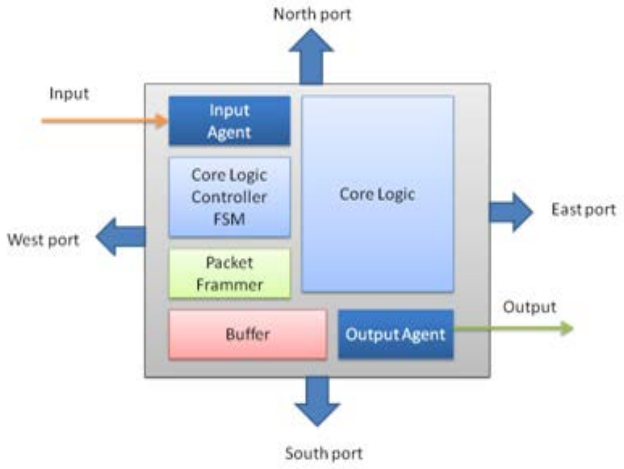

Figure 2. Shows the Architecture of the Processing Element with Core Logic.

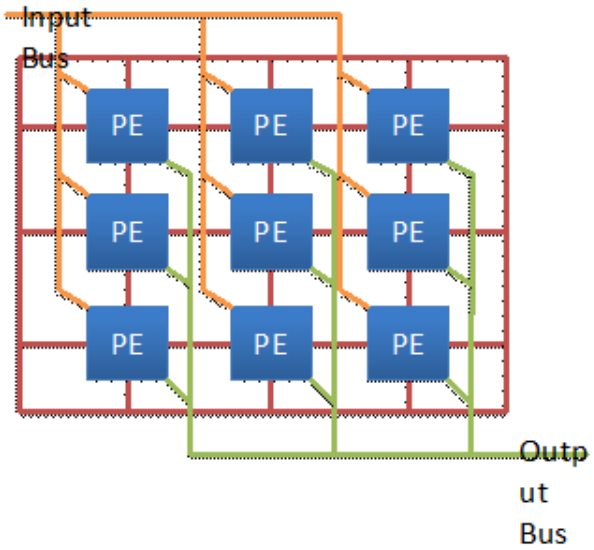

Figure 3. Shows the NOC arrangement in 3x3 Matrix with Global Transmission and Separate Input and Output Busses.

5.1 Performance Analysis

As per the data injected to the network, network is operated. Suppose if we inject low data it will execute with in 3 clock cycles, if we allow high data it will direct to the global routing path and again it will take 3 clock cycles only. Like these it will maintain high constant speed for low and high data. As per the synthesis report Area is in Table 2. Throughput, Efficiency and frequencies are tabulated.

Table 2. Synthesis Report

Resources	Original Router Architecture	Proposed Router Architecture
Slices	92	90
LUTs	235	202
Flip Flops	92	90
Bonded IOBs	201	88

6. Conclusion and Future Scope

In this paper, we improvise the routing Efficiency of Network on Chip (NOC). Therefore the main objective of this paper is to design Router free architecture for NOC by using Agents in the Processing elements, by depending on Temperature co-efficient, we avoid dead locking in NOC. Finally we improve the Efficiency of Network on Chip. Efficiency in the sense, the Power, Area, Latency, Speed, Frequency, Throughput and Injection rate. In future, we would like to extend the work by 3*3 3D Mesh Network on Chips (NOC's) with real-time IP Cores and we would like to improve the Performance of Multi-core systems.

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