Design of Low EMI Power Supply using Resonant Converter

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Abstract

Objectives: There are several applications where even a temporary power failure can cause a great deal of public inconvenience leading to large economic losses. **Methods/Analysis**: In this paper the electrical power utilization will give an indirect idea of the economic growth of any country. For such critical loads, it is of paramount importance to provide an Uninterruptible Power Supply (UPS) system, as to maintain the continuity of supply in cases of power outage. **Findings**: Here a new UPS system with Unity Power Factor (UPF) and low Electro Magnetic Interference (EMI) has been proposed. The circuit diagram of the proposed scheme has been modeled and simulated in SIMULINK Block of the MATLAB software and the waveforms have been taken accordingly. These waveforms give a clear picture of the working and the advantages of the proposed method. **Novelty of the study**: The study presents a novel UPS with UPF and transformer separation by a high-frequency connectivity in the circuit. The theme was evolved for presenting a lower EMI for soft switching, besides, incorporating frequency content of switching waveforms, especially those related to the input and output of the UPS. **Conclusion/Application**: A 1 phase, 230V, 50Hz, simulation circuit, withstanding loading up to 3.2kW, has been presented, and the measurements indicate that lower EMI is possible, and a measurement of Power Factor of 0.996 was attained.

Keywords: EMI, UPS, ZCS, ZVS, Noise

1. Introduction

On-line UPS finds wide applications today, in critical loads like computers, hospitals and airline reservation system need Uninterruptible Power Supply. UPS provides protection against power outage as well as voltage regulation during power line over voltage and under voltage conditions. However it may generate EMI and input power factor can be very poor. EMI is the degradation in the performance of a device, or equipment caused by an electromagnetic disturbance. Power factor also has another serious and undesirable effect on the power supply. Therefore we have to reduce EMI and improve the power factor. Historically, instantaneous solutions to EMI and volatile power factor have been proposed by way of filters and pre-regulator to existing equipment¹. However, this jacked up the system cost and output link voltage, thereby making the EMI

observation even more complicated. This paper presents a frame work for UPS, incorporating both the Unity Power Factor and low EMI. This scheme is based on the concept of ZCS and ZVS apart from internal waveform shaping the modules.

1.1 Conventional UPS

Figure 1 shows the block diagram of a typical UPF On-line UPS with galvanic isolation. To secure unity power factor, the design incorporates a pre regulator on the input subsequent to the main rectifier which generates the current waves through high frequency modulation. In the process, the rectified input voltage is converted to a dc voltage. This dc voltage is inverted to a high frequency transformer, which also provides galvanic isolation. The secondary voltage is rectified to charge the battery and supply the output dc link voltage. This voltage is inverted

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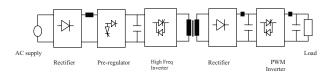


Figure 1. Conventional On –line UPS block diagram.

by a pulse-width modulation inverter to supply 230 V at 50 Hz, to the load⁹⁻¹¹.

2. Low-EMI and UPF UPS

2.1 Block Diagram of Low-EMI and UPF UPS

Figure 2 shows the block diagram of the low EMI and UPF UPS. The main input voltage is rectified to dc voltage by input rectifier. Then the dc voltage is inverted by a dc-to-dc converter, and the Partial Series Resonant Converter (PSRC)², to a high frequency ac voltage, which passes through a transformer to provide galvanic isolation. A low frequency inverter providing the load then inverts the pulsed dc voltage to 50 Hz, 230 V is alternating supply. A bidirectional dc – to – dc converter linked in tandem to the capacitor (C_4) absorbs reactive power, which acts as a compensator with typical voltage and current waveform. The second function of this bidirectional inverter is to charge the battery and, in the event of a mains failure, to provide power to the load. This converter will be referred to as "dynamic compensator".

3. Analysis of Converter

This section illustrates the functioning of sub converters including its switching pattern.

3.1 Partial Series Resonant Converter (PSRC)

Figure 3 shows the block diagram of Partial Series Resonant Converter. Partial series resonant technique allows one to increase the switching frequency, reducing the size of the input inductance. In particular, ZVS topologies are well suited for high frequency application; but they are affected by minimum load constraint that makes their use difficult. On the contrary, zero current switching topologies require that the load does not exceed a maximum value given by the input voltage level and circuit parameters. This limitation fits very well the features of the UPS, making ZCS-Partial Series Resonant converter4. It consists of a resonant converter and one high frequency rectifier and also a transformer for the isolation purpose. Resonant network consists of two resonant capacitors (C_2, C_3) and a resonant inductor (L_1) . Each switch in such a converter requires a current commutation circuit, which turns the main switch OFF, by forcing the current through its to go zero, because of the complexity and substantial losses in the commutation circuits. An important observation is that at zero voltage turn OFF, a switch and a capacitor are connected directly across the switch. Therefore the switch must be turned ON only at zero voltage; otherwise the energy stored in the capacitor will be dissipated in the switch³. Therefore the diode in anti parallel with the switch must conduct prior to the closing of the switch. The power dissipation in the switch during

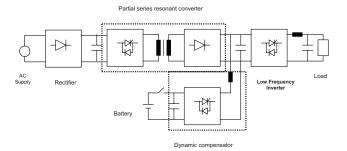


Figure 2. Block diagram of low EMI and UPF UPS.

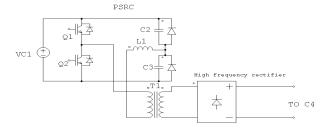


Figure 3. Partial series resonant converter.

switching transition occurs because during transition the voltage across the switch and current through it has non-zero finite values. The power dissipation at an instant during the transition is the product of the instantaneous current or the voltage is zero. Therefore the switch is turned ON and OFF at zero voltage and zero current by this resonant converter. In this way the switching can be increased without increasing the power loss^{5,11}.

When Q₁ is ON, and Q₂ is OFF, resonant capacitor charged up to V. First switch Q, is turned OFF. Transformer magnetizing current continuous to flow through capacitor (C₂). Both diodes which across the switches, latch in, which provides a short circuit across the secondary and hence across the primary. At this point, the energy stored on the top end C₃ discharges through the short circuit primary, through the resonant inductance L₁ through the bottom filter capacitor C₂ and back in to the bottom end of C₃. Since there are no resistors in this path, the discharge losses are less. The negative resonant voltage impulse right hand of L, pulls the junction of C, and C₃ down to ground and now Q₁ is turned ON at zero voltage. Capacitor C2 slowed up Q1 voltage fall time sufficiently so that there is simultaneously high voltage and current during its turn OFF. During each half switching cycle, different sub cycles exist wherein the circuit operation can be defined. The sequence of different sub cycle during operation is dependent to a certain extent on the output voltage. Since the output filter capacitor C₄ is large, the output voltage will not change in steady state.

The voltage limit across the resonant capacitors which is introduced by D₇ and D₈ also limits the voltage stresses, which is an important improvement regarding cost and reliability, especially at high power levels.

Energy stored in the resonant capacitors is given by

$$E_{c} = \frac{1}{2} \cdot C_{r} \cdot V_{c1}^{2}(t) \tag{1}$$

Where, C_r - resonant capacitors (C_2+C_3) in Farads. $V_{c1}(t)$ - input across C_1 in volts.

When some of the energy contained in C_2 and C_3 is fed back to the supply, that is commutation of the phase arm before the entire energy pulse is transferred to the output, will not be valid and a larger switching frequency for a given output power will be obtained and is transferred to output during each half switching^{3,6}. This result which is in the output power of the PSRC is given by

$$P_{out}(t) = E_{c}.2f \tag{2}$$

$$P_{out}(t) = C.V_{r-c1}^{2}(t).f$$
 (3)

where

 $P_{\text{out}}(t)$ - output power of the PSRC in watts *f* - Operating frequency of the PSRC in Hertz.

Periodically, whenever the power levels fall the converter gets switched ON and OFF in bursts or multiples. Therefore, control of burst of the 50 Hz mains supply and keeping tab on full sinusoidal cycles of the 50 Hz mains voltage during these positions of ON and OFF are highly necessary. This ensures a high power factor by maintain minimum harmonic distortions in the current from the supply. Since the power level is low, it should not play an important role on the flicker value it would generate. An opening in chassis near the high frequency transformer mounting was closed using copper adhesive tape. In the addition the inter-winding wires between power factor correction and dc-to-dc converter circuit were shielded with using copper tape. This arrangement resulted in a reduction of radiated emission levels⁶. PSRC becomes not only a means of reducing EMI¹⁶, but reducing the switching losses also¹⁷.

3.2 Dynamic Compensator

The dynamic compensator's functioning consists of two operations consisting of current compensation and the resonant current reversal

3.2.1 Resonant Current Reversal

In case of a reactive or non linear load, the load current $I_{load}(t)$ will not be equal to zero during a voltage zero crossing. Whenever there is a reactive current in the load, the current at mains equal zero voltage crossing. Therefore, the compensating current $I_{\text{comp}}(t)$ could move from positive to negative. By means of a resonant cycle, this current could be reversed and this is realized by scrupulously choosing C_4 and L_2 . However, the chief factor is the admissible voltage overshoots across C_4 , as its value is predetermined to the minimum ripple voltage of the converters is usual functioning¹²⁻¹⁴.

The value of the output capacitor C_4 decides the main value of the voltage ripple. The sources for the ripple voltage include the PSRC at first and the dynamic compensator. The value of C_4 is given by

$$C_{_{4}} = \frac{Q_{_{PSRC}} + Q_{_{COMP}}}{\Delta V_{_{CA}}} \tag{4}$$

Where,

 Q_{PSRC} - charge of PSRC into C_4 (C)

Q_{COMP} - charge of dynamic compensator (C)

 Vc_4 - maximum output voltage ripple on C_4 (V)

 $\triangle Vc_4$ - output capacitance (F)

$$VC_{4}(t) = I_{trans} \cdot \sqrt{\frac{L}{C_{4}}} \cdot Sin(\frac{t}{\sqrt{L_{2} \cdot C_{4}}})$$
 (5)

The voltage across C_4 during the resonant period is given by

Where,

Vc₄ - peak overshoot voltage across C₄ in volts

 I_{trans} - amplitude of inductor current to be reversed in Amps

L₂ - value of inductor in Henry

The peak voltage overshoots during the resonant period id given by

$$VC_{4} = I_{trans} \cdot \sqrt{\frac{L_{2}}{C_{4}}}$$
 (6)

and the current in the inductor L_2 during the resonant phase arm is given by

$$I_{comp}(t) = I_{trans} \cdot COS(\frac{t}{\sqrt{L \cdot C_{\frac{1}{2}}}})$$
 (7)

The resonant period is given by

$$t = \pi \cdot \sqrt{L_{2} \cdot C_{4}} \tag{8}$$

where t_{r} is the resonant current reversal period in seconds.

The current reversal period is small (say 4% of a 50 Hz) and its impact is meager on the harmonic distortion on the main supply current. As a consequence of current reversal in the dynamic compensator, the input current has dead time. Besides bringing down the cost, the dynamic compensator also improves the response of UPS while there is a change in load factor¹⁵.

3.3 Output Inverter

A 100 Hz pulsed DC voltage V_{C4} feeds the inverter. The inverter switches at 50 Hz, alternatively switching the diagonal pairs Q_s and Q_o ON for the positive cycle, keeping the Q₆ and Q₇ OFF. As for the negative cycle the process gets reversed. At the zero voltage crossing of the mains supply, the switching takes place and the sinusoidal voltage gets reconstructed and transmitted to the load. The switches Q_6 and Q_8 are turned ON, while Q_5 and Q_7 remain OFF during the resonant reversal period. This enables the inductor current $I_{\text{comp}}(t)$ to be reversed and the load current to continue running. Output filtering of L_3 and C_6 filters out the high frequency on C_4 and smooth out the zero crossing transition on the output voltage7. The filtered output of the inverter has very low harmonic distortion, despite the nonlinearity of the dominant loads, thereby supplying more harmonic currents into the UPS. The output voltage harmonic content is specified by a term called Total Harmonic Distortion (THD), which was defined by

%
$$THD = 100 \times \frac{\sum_{h=2}^{\infty} V^2}{V}$$
 (9)

Where

V₁ is the fundamental frequency rms value of the output voltage and

 V_h is the rms magnitude at harmonic of order h.

Typically, THD is specified to be less than 5%; each harmonic voltage as a ratio of V_1 is specified to be less than 3%.

4. Simulation and Results

4.1 MATLAB Simulation

The below presented Figure 4 shows the circuit diagram for the low-EMI UPS system, that has been taken for analysis in the thesis. The simulator has been performed using MATLAB software. The components PSRC, in the circuit has been enlarged and represented in the Figure 5.

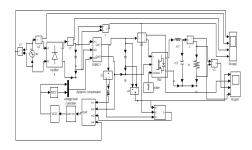


Figure 4. MATLAB circuit model for low EMI UPS.

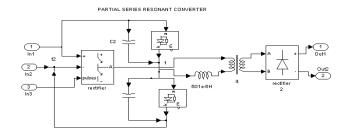


Figure 5. Partial series resonant converter.

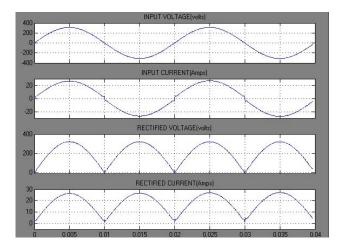


Figure 6. Input and output waveforms during power supply.

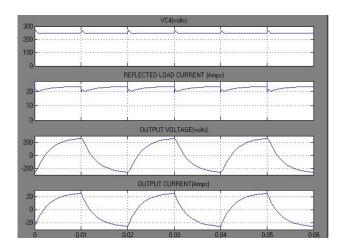


Figure 7. Output waveforms during power failure.

4.2 Results

The design parameter values of the above circuit are

$$C_1 = 1 \mu F,$$
 $C_2 = 220 \text{ nF},$ $C_3 = 220 \text{ nF},$ $C_4 = 43 \mu F,$ $C_1 = 6.1 \mu H,$ $C_2 = 88 \mu H$

Figure 6 shows the resultant waveform of the main circuit at supply ON condition and the Figure 7 shows the resultant waveform at power failure condition.

From the results it has been inferred that, power factor is 0.994 and conducted EMI is very less and the efficiency is calculated from following measures, the input voltage, current and power are as follows:

$$V_{in} = 229.8 \text{ V}, \qquad I_{in} = 17.78 \text{ A}, \qquad P_{in} = 4080 \text{ W}$$

The output voltage, current and power is as follows:

$$V_{load} = 208 \text{ V}, \qquad I_{load} = 19.1 \text{ A}, \qquad P_{load} = 3950 \text{ W}$$

The efficiency of the system under normal operating conditions is measured as 96.2%.

5. Conclusion

This paper has proposed a new UPS configuration that features UPF, separating transformer through a high-frequency connectivity in the circuit. The theme was developed by producing lower conducted EMI for soft switching, but also for having the frequency content of switching waveforms, specifically those related to the output and input of the UPS. What is eventually being offered is a single phase 230 V, 50 Hz, simulated circuit that can withstand load up to 3.2 kW. Calculations show lower EMI is possible, and a power factor of 0.996 was

measured by way of simulated waveform using MATLAB software.

6. References

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