

# Buck Converter with a Variable Number of Predictive Current Distributing Method

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## Abstract

This paper reports that the converter efficiency can be achieved by dynamically changing the number of active phases depending on the load. We provide solution related to the transient response of the converter when the number of active phases is changed. The problem arises because the current in the individual phases of the interleaved Buck converter will not be equal immediately after the controller has changed the number of active phases. The current equalisation scheme relies on the measurement of the output current and the knowledge of a few converter parameters and it does not require a measurement of the current in each phase. A digital PWM modulator has been designed that allows the current equalisation scheme to work. Simulations and measurements for a four phase interleaved Buck converter are presented in this paper.

**Keywords:** PWM-Pulse Width Modulation, PID-Proportional Integral Derivative, ADC-Analog to Digital Converter, MOSFET-Metal Oxide Semi Conductor Field Effect Transistor.

## 1. Introduction

The efficiency of interleaved Buck converters is falling considerably at light load because of the switching losses in each of the phases in the interleaved Buck converter. It is therefore advantageous to reduce the number of active phases of an interleaved Buck converter at light loads to increase efficiency [1]. Reference [1] presented the mathematical analysis for improving the converter efficiency through changing the number of active phases depending on the load current but the experimental results presented showed some room for improvements. The main problem of turning a phase in an interleaved converter either ON or OFF is that the currents in the phases will not be equal immediately after the change occurs, which will cause the output voltage to deviate from the steady state output voltage.

This paper is to develop a digital control method for an interleaved Buck converter with a variable number of

active phases, which ensures equal average phase currents in a very short time span after a change in the number of active phases. The proposed current equalisation scheme does not rely on the measurement of each phase current but uses a predictive algorithm to determine the duty cycle of each phase, which will result in equal currents in the active phase.

## 2. Current Sharing During Phase

Predictive current equalisation relies on sampling the output current and determining when to change the number of active phases based on the output current level. Under the assumption that the converter phases are perfectly matched the average current of each active phase is at any time equal to the output current divided by the number of active phases. The concept relies on determining the duty cycle for each phase, which provides equal average inductor current in all phases when the digital control

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scheme changes the number of active phases. The change in average current in any phase can be expressed as:

$$\Delta i_{L,x} = \frac{I_{out}}{n_{phases}} - I_{avg,x} \quad (1)$$

where,  $\Delta i_{L,x}$  is the change in current of phase  $x$ ,  $I_{out}$  is the output current, and  $I_{avg,x}$  is the average current in phase  $x$  before the number of active phases is changed.

The predictive current equalisation scheme works best if the load current changes slowly. For load steps with fast slew rate the predictive current equalisation scheme will not be able to equalise the phase currents perfectly because the load current is not exactly equal to the value that the predictive current equalisation scheme assumes when calculating the duty cycle command for each active phase.

The advantages of the predictive current equalisation scheme are that the phases share the current almost instantaneously after the number of active phases has been changed thereby limiting the stress on the individual phases. The transient response on the output voltage should also be smaller than it would be without the current equalisation scheme.

The inductor current slew rate of each phase for the ON and OFF period of the phase PWM signal is given by equation (2) and (3) and the average slew rate over one switching period is given by (4). Based on equation (4) it is possible to determine the change in the average inductor current as a function of the duty cycle  $D$  (5). Equation (5) can be also written as (6), which gives the required duty cycle to achieve a given change in the average inductor current,  $\Delta iL$ .

$$\alpha_{ON} = \frac{di}{dt} = \frac{V_{in} - V_{out}}{L} \quad (2)$$

$$\alpha_{OFF} = \frac{di}{dt} = \frac{-V_{out}}{L} \quad (3)$$

$$\alpha_{avg} = \left\langle \frac{di}{dt} \right\rangle_{T_{sw}} = \frac{D \cdot V_{in} - V_{out}}{L} \quad (4)$$

$$\langle \Delta i_L \rangle_{T_{sw}} = T_{sw} \cdot \frac{D \cdot V_{in} - V_{out}}{L} \quad (5)$$

$$D = \frac{\Delta i_L \cdot L}{T_{sw} \cdot V_{in}} + \frac{V_{out}}{V_{in}} \quad (6)$$

The above expression for the duty cycle,  $D$ , can be divided into a change in duty cycle,  $\Delta D$  (see (7)), plus a steady state value,  $D_{SS}$  (see (8)). The steady state value of the duty cycle will be equal to the output of the digital PID

compensator before the number of active phases is changed and the change in duty cycle is a fixed value for a specific set of parameters, i.e. input voltage  $V_{in}$ , inductor size  $L$  and PWM time period  $T_{sw}$ .

$$\Delta D = \frac{\Delta i_L \cdot L}{T_{sw} \cdot V_{in}} \quad (7)$$

$$D_{SS} = \frac{V_{out}}{V_{in}} \quad (8)$$

The predictive current equalisation scheme works by measuring the output current, and when a change in the number of active phases is necessary it reads the appropriate values of  $\Delta D$  from a lookup table and adds them to the duty cycle command on the output of the digital PID controller during the equalisation period. Under steady state operation the duty cycle command calculated by the digital compensator determines the duty cycle for all active phases. Depending on the converter specifications it will be possible to equalise the phase currents within one or two PWM periods. If the equalisation scheme has to run over two PWM periods, it will be necessary to calculate the appropriate  $\Delta D$  for each PWM period.

The duty cycle of a phase that is turned ON has to be higher than the steady state duty cycle and the duty cycle of the other active phases has to be lower than the steady state duty cycle for the phase currents to be equalised. The output voltage of a typical synchronous Buck converter used in Point of Load converter applications is typically much lower than the input output voltage. This means that the converter operates with a low steady state duty cycle. Since the duty cycle can not be lower than zero it will in certain situations not be possible to reduce the current in a phase to the new average current in a single PWM cycle.

In that situation it will be necessary to let the predictive current equalisation scheme equalise the current in two or more PWM cycles. The basic operation is the same but the change in duty cycle,  $\Delta D$ , is divided by the number of PWM periods and applied to the relevant phases in consecutive PWM periods until equalisation has been achieved.

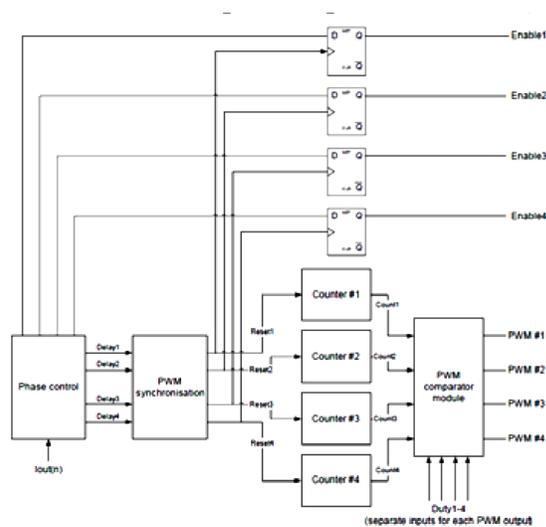
It should be mentioned that the purpose of the predictive current equalisation scheme is to achieve an equalisation of the average inductor current when the number of active phases is changed. If general current sharing in steady state operation is required it must be implemented separately.

### 3. PWM Modulator for Current Equalisation

The PWM modulator for the interleaved Buck converter (see Figure 1) has been designed to accommodate the predictive current equalisation scheme. The PWM modulator consists of four independent counters which are controlled by the 'PWM synchronisation' block. The 'PWM synchronisation' block controls the timing of the active PWM signals for the active phases to ensure that the phase shift between the phases matches the number of active phases.

If for instance three phases are active the 'PWM synchronisation' block will generate reset signals for counters #1, #2 and #3 that are 120 degrees out of phase. The PWM synchronisation block receives the phase shift information from the 'Phase control' block. The 'Phase control' block determines the number of active phases based on the sampled output current  $I_{out(n)}$ .

An enable signal for each phase is generated by a D flip-flop. The D flip-flop is used to synchronise the enable signal with the rising edge of the PWM signal for the phase. Synchronisation of the enable signal is important for the predictive current equalisation scheme to work. If the enable signal is not synchronised to the PWM signal the average current of the phase which is activated will not reach the correct value in the first PWM cycle. Synchronisation is achieved by setting the enable signal high on the D-input of the flip-flop before the reset signal is set. The D flip-flop



**Figure 1.** Current Equalisation Scheme with PWM Modulator.

will set the enable signal on the rising edge of the reset signal from the 'PWM synchronisation' block.

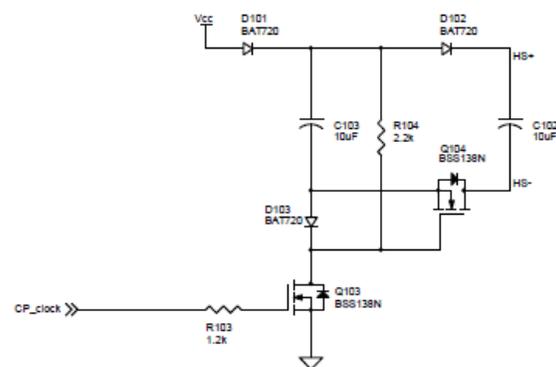
The 'PWM comparator module' generates the PWM signals for the four phases by comparing the output of the four counters with the duty cycle command for the respective phases.

The PWM modulator shown in Figure 2 has many similarities to other digital multiphase PWM modulator implementations [2-4]. The PWM modulators of [2] and [3] have only one duty cycle command input which is used to determine the duty cycle of all phases. The advantage of this approach is that the complexity and size of the PWM modulator is low but with limitation that the duty cycle cannot be controlled individually for the separate phases. The PWM modulator of [4] has separate duty cycle command inputs for each phase but it does not generate enable signals for each phase.

### 4. Charge Supply for Drive

In order for the predictive current equalisation scheme to work it is important that each phase of the interleaved Buck converter can start immediately when the enable signal generated by the digital controller is activated.

A charge pump supply for the high side driver of the gate drive ICs has therefore been added to be able to turn ON the high side MOSFET immediately after the gate drive IC has been enabled [5]. A schematic of the charge pump supply is shown in Figure 2. The charge pump is controlled by the signal  $CP\_clock$  which is generated by the digital controller. The frequency of  $CP\_clock$  is the same as the switching frequency and it has a duty cycle of 50%. The output voltage lies across C102 which is connected to gate drive ICs bootstrap input.



**Figure 2.** Charge supply for gate drive.

The charge pump supply ensures constant supply voltage for the high side gate drive. An identical charge pump circuit has to be used for each phase which increases the component count and complexity of the interleaved Buck converter.

## 5. Control Methodology

Figure 3 shows a block diagram for the control system for the four phase interleaved Buck converter with the predictive current equalisation scheme. The digital control scheme has been implemented in an FPGA and it can be divided into three main blocks. The PWM modulator has already been described in section III. The digital compensator is a PID compensator with the transfer function:

$$G_{comp}(z) = \frac{b_0 + b_1 \cdot z^{-1} + b_2 \cdot z^{-2}}{1 - z^{-1}} \quad (9)$$

The digital compensator has been implemented as a state machine it can calculate the duty cycle command in just three clock cycles from the time it reads the sampled output voltage from the ADC [6]. The final block of the digital control scheme is the Duty cycle Look-up table which is controlled by the PWM modulator. The Duty cycle Look-up table is controlled by the PWM modulator which determines when the number of active phases must be changed and gives the appropriate command for the Look-up table. When the converter operates in steady state with a fixed number of active phases the Duty cycle Lookup table is inactive and passes the duty cycle  $D_{ss}(n)$  directly to all phases. During a transient condition when the number of active phases is changed the Duty cycle Look-up table adds a term to each duty cycle command to ensure current equalisation. The terms added to the duty cycle command have been calculated based on (7) and a set of  $\Delta D$ s for each possible change in the number of active phases, i.e. an

increase or decrease of the number active phases, are stored in the Duty cycle Look-up table.

The system uses two ADCs to sample the output voltage and output current of the interleaved Buck Converter. The ADC that samples the output current is an 8-bit 1 MSPS Successive Approximation ADC with an input voltage range from 0 to 3.3V. The ADC sampling the output voltage is a 10-bit 50 MSPS pipelined ADC with an input voltage range from 0.95 to 1.95V. The reason for using two ADCs is that the requirements for the two ADCs are different.

The ADC sampling the output current must be able to sample current levels over the full output current range but it does not have to be very fast since a small delay in determining when to change the number of active phases is of small consequence. The speed of the ADC sampling the output voltage on the other hand is important because it affects the control loop bandwidth and stability. A fast ADC with a small delay makes it possible to achieve a high control loop bandwidth which leads to a faster transient response.

Ideally the predictive current equalisation scheme should be extended to include a measurement of the converter input voltage. The average inductor current slew rate is a function of the input voltage as expressed in (5). The  $\Delta D$  values stored in the Duty cycle Look-up table have been calculated at the nominal input voltage and the predictive current equalisation scheme will therefore work well at nominal input voltage but the performance deteriorates when the input voltage different from the nominal value. If the Duty cycle Look-up table was extended to include different set of  $\Delta D$ s for different input voltage levels the predictive current equalisation scheme would have consistent performance over the full input voltage range.

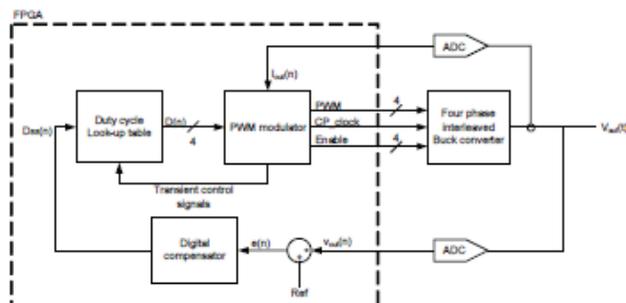


Figure 3. Block diagram of the control methodology.

## 6. Simulations Results

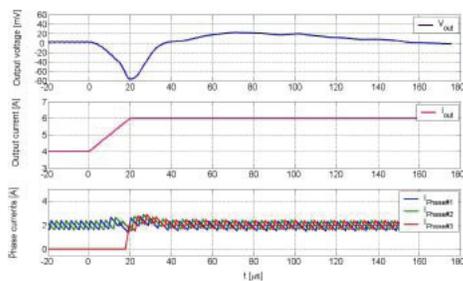
A four phase interleaved Buck converter was designed to test the proposed predictive current equalization scheme. The output current is measured through a current sense resistor and it is sampled at the per phase switching frequency. The output current range is divided into four ranges where only one phase is active in the lowest range; two phases are active in the second range and so on. A small hysteresis band was added around the current levels at which the number of phases changes to ensure stable operation.

Figure 4 shows a simulation and the corresponding measurement of a load step for the multiphase interleaved Buck converter without the predictive current equalisation scheme. The output voltage drop is approximately 50mV in the simulation and it is close to 80 mV for the measurement. The phase currents slowly converge towards the same average current due to the series resistance of the inductors.

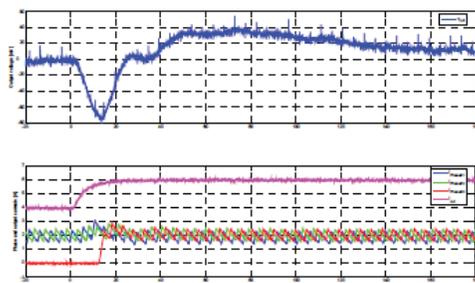
Figure 5 shows simulation and measurement for the same load step but this time the predictive current equalisation scheme is active. The output voltage drop due to the load step has become worse for the simulation whereas the measurement is similar to the measurement of Figure 6.

There are two reasons why the predictive current equalisation scheme does not reduce the transient on the output voltage when the number of active phases is changed. The first reason is that there is a short delay between the time the load current passes the 5A threshold and the time the number of active phases is changed.

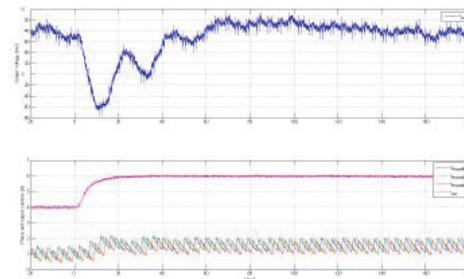
It appears that no improvement has been achieved with the current equalisation scheme during a load step where the number of active phases is changed at least not on the transient response of the output voltage. It must however be noticed that by equalising the phase currents the com-



**Figure 4.** Simulation of load step from 4 to 6A with predictive current sharing.



**Figure 5.** Measurement of load step from 4 to 6A with predictive current sharing.



**Figure 6.** Measurement of load step from 4 to 6A with all phases active.

ponent stresses are the same for all phases, thus minimizing the stress of each phase.

In Figure 5 and Figure 6 the load current is held constant at 5A while the number of active phases is changed from 2 to 3. The purpose of these measurements is to show the output voltage response to a change in the number of phases under a constant load. The output voltage overshoot is smaller with the predictive current equalisation (Figure 4) than without the predictive current equalisation scheme (Figure 5). The digital controller changes the number of active phases in a periodic manner in the measurements of Figure 5 and Figure 6. Under normal operating conditions the digital controller will not change the number of active phases if the load current is constant.

## 7. Conclusion

In this paper the predictive current equalisation scheme for an Buck converter with a variable number of active phases has been presented. The digital control scheme equalises the phase currents by adding a value, which has been calculated in advance, to the duty cycle command of each PWM signal that controls the active phases, depending on the number of active phases and the output current level. Experimental results and simulations show similar responses to a load step, which forces a change in the number of active phases from 2 to 3.

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