# RF Performance Evaluation of Nanoscale FD-SOI MOS Transistors

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### Abstract

**Objectives**: In this work, the performance of single-gate and double-gate FD-SOI MOSFETs has been investigated in order to find out its utility RF applications. **Methods/statistical analysis**: The small-signal equivalent model is utilized to obtain the Y parameter of the devices and from which the minimum noise Figure and S parameter of the devices are derived and provides its applicability in the design of RFICs. The analysis is carried out using the Silvaco 2D ATLAS tool. **Findings**: The simplified small-signal equivalent models for both the devices are developed to analyze its high-frequency response more accurately, and to extract other important high-frequency (RF) parameters. **Application/improvements**: The derived S parameters are used to evaluate its high-frequency (RF) losses. In the SG FD-SOI MOSFET, the Insertion loss is 2.47 dB, the Transmission loss is 2.48 dB and the Reflection loss is 1.02 dB lower in comparison to DG FD-SOI MOSFET while its Return loss is 0.05 dB higher in comparison to that of DG FD-SOI MOSFET.

Keywords: FD-SOI MOSFET, RFICs, Leakage Current, Power Dissipation, RF Frequency

## 1. Introduction

The demand for high-performance wireless and RFIC applications with low power consumption is increasing day by day. This increasing demand leads to the need for very-high density on-chip integration in annexation with optimum performance.<sup>1</sup> To achieve these properties, the CMOS technology is clamped into the tenth of the nanometre range.<sup>2</sup> However, it becomes very arduous to preserve the behaviour of such semiconductor devices when its physical dimensions are reduced to a tenth of the nanometer range. The challenges arise due to the adverse effect imposed by the small geometry devices (SCEs).<sup>3–6</sup>

To overcome the forestated hindrances, since last two decade researchers are making great effort and even various device designs already have been proposed.<sup>Z-13</sup> SOI technology out of several MOS technology is preferred due to its several advantageous features like it highly suppress the leakage currents by using a buried oxide (BOX) insulating layer underneath the channel region and also its fabrication is easy and cost-efficient.<sup>14–17</sup> Considering the FD-SOI MOSFETs, In the Radiofrequency operating range several losses take place, so it is very essential to analyse these losses for more accurate characterization. $\frac{18}{18}$ 

In the field of RF applications using FD-SOI MOS devices, a number of researches have already been carried out.19-22 Lázaro & Iñiguez compares the RF/HF and noise behaviour of single-gate (SG) as well as double-gate (DG) FD-SOI MOS devices and found that  $f_{\rm T}$  of the DG SOI is greater in comparison to the SG-SOI and hence DG -OI has larger BW in comparison to the SG-SOI for RF applications<sup>23</sup> stated the impact of engineering in channel doping and gate electrode material on its analog & RF/HF performance of FD-SOI MOS device and obtained that gate engineered device has improved  $f_{\rm T}$  and  $f_{\rm MAX}$  while channel engineered device has reduced  $f_{\rm T}$  with respect to single metal double-gate (DG) MOSFET.<sup>24</sup> Later, in the DG MOS device the impact of gate electrode engineering on it is analog & RF/HF performance. The work concludes that the use of a triple metal gate electrode results in peak horizontal electric-field deviation at the source/ channel interface region. This phenomenon improves the carrier transference efficiency and hence provides higher 1-decibel compression point when compared to that of the single metal DG and double metal DG MOSFET making it suitable device to achieve high linearity when used to design a ultra-wide band (UWB) LNA circuit<sup>25</sup> the influence of stacking high-k gate insulating dielectric material over a silicon dioxide material on RF/HF performance of the nanoscale DG FD-SOIMOSFET and concluded that gate stacking using Silicon Nitride (Si<sub>3</sub>N<sub>4</sub>) as high-k dielectric material exhibit improved DIBL, reduced subthreshold slope (*SS*), better  $f_{\rm T}$  and gain as compared to that of the other high-k dielectric material making it primary choice for large BW analog and RF/HF applications.<sup>26</sup>

The analog and RF analysis of the above-reported literature only deals with BW, short channel effects or power dissipation and their associated leakages. The losses in devices operating at the RF range have not been discussed by any of the earlier researchers. In this work, an investigation on the RF/HF performance of the single and double gate FD-SOI MOSFET is carried out combined with their associated high-frequency losses. The key Figure-of-merits (FOMs) utilized for the RF/HF performance investigation of the MOS devices includes intrinsic capacitances ( $C_{gs} \& C_{gd}$ ), cut-off or unity current gain frequency  $(f_{\rm T})$  and frequency transconductance gain product (FTGP). The results obtained for RF analysis of the designed devices have been compared & contrasted to that of the recently reported literature. Also, for the first time, a simplified small-signal high-frequency equivalent circuit model for the DG FD-SOI MOS device has been proposed to extract its essential RF/HF parameters.

# 2. Device Descriptions

The structure of both MOS devices is represented in Figures 1 and 2 respectively. Silicon dioxide (SiO<sub>2</sub>) is used as an insulating material for the gate as well as for the buried-oxide (BOX) regions in both devices.<sup>27</sup> The source and drain diffusion regions are n-type regions doped with the Gaussian doping profile whereas the channel region is uniformly doped p-type region. The analysis is done by using a powerful Atlas 2D simulator. The physical model implemented for the MOS device simulation includes the common mobility model (CONMOB) to define the mobility of the device, for carrier recombination model, Shockley-Read-Hall (SRH) model is used and Boltzmann static (BOLTZMAN) as a static carrier transport model.<sup>28</sup>

The physical parameters used in the designing of SG-and DG-FD-SOI MOS devices are described in Table 1.



Figure 1. Structure of designed SG FD-SOI MOSFET.



Figure 2. Structure of designed DG FD-SOI MOSFET.

**Table 1.** Parameters used in the design of SG FD-SOIand DG FD-SOI MOS devices

Symbol	Parameter	Value
L	Channel length	20nm
t <sub>ox</sub>	Gate oxide thickness	1nm
t <sub>box</sub>	Buried oxide thickness (BOX)	3nm
t <sub>si</sub>	Silicon substrate thickness	10nm
W	Width	50nm
$N^+$	Drain/Source doping concentration	1e20cm <sup>-3</sup>
Na	Channel doping concentration	1e15cm <sup>-3</sup>

# 3. Small Signal Analysis

The small signal analysis is essential to examine the RF/HF response of the MOSFETs more precisely and also to easily extract other important high-frequency parameters.<sup>29,30</sup> In the small signal analysis, the Source and Substrate (Body) terminal are shorted together in order to realize the effective configuration as a two-port network. This method is the simplest method used for extracting the parasitic components of the MOS devices which are utilized in accurate RF measurement. For common two port-networks, a particular current and voltage values are assigned to each of these ports. For a two-port analysis of the MOS devices, Source and Gate terminal are considered as an input port while the Source and Drain terminal is considered as an output port. For a two-port network if V2, I2 and V1, I1 are considered as voltages and currents at the output port and input port respectively, then it's short-circuited admittance parameter can be expressed as:

$$Y_{11} = I_1 / V_1 | V_2 = 0$$
 (1)

$$Y_{12} = I_1 / V_2 | V_1 = 0$$
 (2)

$$Y_{21} = I_2 / V_1 | V_2 = 0$$
 (3)

$$Y_{22} = I_2 / V_2 | V_1 = 0$$
(4)

The two-port admittance of the network is given by:

$$Y = \begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix}$$
(5)

These Y parameters can be utilized to obtain the effective S parameters which are further used for high-frequency analysis of the designed MOS devices. The Y parameters are used in the analysis because it is also known as the "Transadmittance parameter" i.e., voltage-controlled current source (VCCS) and it is a known fact that the MOSFET is inherently the VCCS.

The high frequency small-signal equivalent circuit model for SG FD-SOI MOSFET<sup>31</sup> is shown in Figure 3 in which  $C_{\rm gs}$ ,  $C_{\rm gd}$ ,  $C_{\rm sb}$ ,  $C_{\rm db}$  and  $C_{\rm gb}$  are the gate-to-source, gate-to-drain, source-to-body, drain-to-body and gate-to-body capacitances respectively. The  $R_{\rm s}$ ,  $R_{\rm d}$ ,  $R_{\rm g}$  and  $R_{\rm sub}$  are the source, drain, gate and substrate resistances respectively.

The small-signal high-frequency equivalent circuit model for the representation of double gate FD-SOI



**Figure 3.** Small signal equivalent circuit for SGFD-SOI MOSFET.

MOSFET is shown in Figure 4 represents the high frequency in which gate-to-source capacitance ( $C_{\rm gs}$ ) is a combination of  $C_{\rm g1s}$  and  $C_{\rm g2s}$ , while gate-to-drain capacitance ( $C_{\rm gd}$ ) is a combination of  $C_{\rm g1d}$  and  $C_{\rm g2d}$ ,  $C_{\rm g1g2}$ 



**Figure 4.** Small signal equivalent circuit for DGFD-SOI MOSFET.

is the capacitance between Gate1 and Gate2 terminals,  $R_{g1}$  and  $R_{g1}$  are the resistances across the Gate1 and Gate2 terminals respectively and  $R_s$ ,  $R_d$  and  $R_{sub}$  are the resistances across the source, drain and substrate terminals.

The  $C_{\rm gd}$  and  $C_{\rm gs}$  are due to overlapped structure of gate electrode on the drain as well as source diffusion regions which depend upon the height of the gate-electrode terminal and responsible for fringe capacitances at the source as well as drain edges. Both the maximum frequency of oscillation  $f_{\rm max}$  and the transition-frequency  $f_{\rm T}$  have an inverse relationship with all these capacitances and hence increase in capacitances results in a decrease in  $f_{\rm T}$  and  $f_{\rm max}$ . Therefore, the value of these capacitances required to be low in order to achieve better RF/HF behaviour. For distributed contact-resistance model,<sup>32</sup> the source and drain resistance is given by:

$$R_{Source} = R_{Drian} = R_C + \frac{L_{S/D}}{q\mu_o WNt_{si}}$$
(6)

where,  $R_{\rm C}$  represents the contact resistance,  $L_{\rm S/D}$  represents the length of the source or drain electrode (for symmetric MOSFET), *W* is the channel region width, the electron charge is *q*, *N* is doping concentration of source or drain diffusion region,  $t_{\rm si}$  represents the thickness of the silicon film and  $\mu_{\rm o}$  is electron mobility under no bias condition.

## 3. Results and Discussions

The transfer characteristics for both SG and DG FD-SOI MOSFETs are obtained and shown here in Figure 5. For all the figures shown here, the line with square mark denotes the behaviour of SG FD-SOI MOSFET and the line having circular mark denotes the behaviour of DG FD-SOI MOSFET. The gradual increase in gate-to-source voltage results in a larger increase in the value of the drain current (I<sub>D</sub>) in the DGMOS device in comparison to the SG MOS device. The leakage current in DG FD-SOI MOSFET is found to be 0.15 A/µm while it is equal to 0.09 A/µm in the single gate FD-SOI MOSFET. The Ion/ *loff* is  $1.5 \times 10^6$  in double gate FD-SOI MOSFET and  $10^3$ in the SG MOS device. One can observe that the Ion/Ioff and the leakage current for the DG MOS device are larger which implies that it has high switching speed with high power dissipation. The intrinsic-capacitances ( $C_{gd}$  and  $C_{\rm gs}$ ) of the devices are extracted by using small signal AC



Figure 5. I<sub>D</sub> versus V<sub>GS</sub> characteristic.

analysis after performing the DC analysis. In this work, the intrinsic capacitances ( $C_{\rm gd}$  and  $C_{\rm gs}$ ) are obtained by performing AC analysis at 1 MHz frequency with DC sweep voltage of 0V to 1.5V. Figure 6 represents the  $C_{\rm gd}$  and  $C_{\rm gs}$  variations at different gate-to-source voltages. For the double gate, FD-SOI MOSFET reduced value of both intrinsic capacitances ( $C_{\rm gs}$  and  $C_{\rm gd}$ ) are observed in comparison to that of the single-gate FD-SOI MOSFET. A smaller value of intrinsic capacitances implies that it has high transconductance value and hence it is more suitable for high-frequency applications.

The  $f_{\rm T}$  can be evaluated by using Eq. (7). In Figure 7, the value  $f_{\rm T}$  for DGFD-SOI MOSFET is found to be larger



**Figure 6.** Behavior of  $C_{gs} \& C_{gd}$  versus  $V_{GS}$ .

in comparison to the SGFD-SOI MOSFET which reflects the higher gate electrode controllability over the channel with higher transconductance ( $g_m$ ) value and with lower  $C_{gd}$  and  $C_{gs}$  as explained above.

Another key parameter for used in analog & RF/HF performance evaluation of the MOS devices is known as frequency transconductance gain product (*FTGP*) which is formulated in Eq. (8). *FTGP* shows the trade-off between switching speed and intrinsic voltage gain. For high-speed operation, we have to compromise with the voltage gain. When voltage gain increases, the lower limit of the drain current increases and the upper limit remains the same which shows that its Ion/Ioff ratio decreases and hence its switching speed decreases.

$$f_T \approx \frac{gm}{2\pi (C_{gs} + C_{gd})} \tag{7}$$

$$FTGP = f_T \times \left(\frac{gm}{I_D}\right) \times \left(\frac{gm}{g_d}\right) = FTP \times A_V \tag{8}$$

The variation of Y parameter (short circuit admittance parameter) with respect to the frequency up to 1 THz is represented from Figure 8–11. In Figures 8 and 9, it is clearly observed that *Real* ( $Y_{11}$ ), *Real* ( $Y_{22}$ ), *Real* ( $Y_{12}$ ) and *Real* ( $Y_{21}$ ) values for both the devices are frequency-independent which implies that it is less sensitive to the high-frequency signals.

The variation of *Img*  $(Y_{11})$ , *Img*  $(Y_{22})$ , *Img*  $(Y_{12})$  and *Img*  $(Y_{21})$  values with respect to frequency for both the devices are shown in Figures 10 and 11. It is evident that the electrical characteristics exhibit by both the devices



**Figure 7.** Behaviour of  $f_T$  and FTGP versus VG<sub>S</sub>.



**Figure 8.** Real  $(Y_{11})$  and Real  $(Y_{22})$  versus frequency.



**Figure 9.** Real  $(Y_{12})$  and Real  $(Y_{21})$  versus frequency.



**Figure 10.** Img  $(Y_{11})$  and Img  $(Y_{22})$  versus frequency.



**Figure 11.** Img  $(Y_{12})$  and Img  $(Y_{21})$  versus frequency.

is almost independent of the frequency up to several 100 GHz and beyond this, it changes abruptly. The plots for Y parameters reveal that both the devices are exhibit almost similar performance in terms of frequency sensitivity.

Figure 12 represents the variation of minimumnoise Figure m for a different range of frequencies and it is observed that up to 100GHz of frequency range it is almost negligible and beyond this it increases abruptly. For single gate FD-SOI MOSFET, this increase is larger as compared to the double gate FD-SOI MOSFET.

Figure 13–16 represents a variation of the S-parameters for different frequency ranges. The Y-parameters of the devices (Eq. (9) to Eq. (12))<sup>19</sup> are utilized to derive the S-parameters. From the plot, it is observed that all the parameters are frequency-independent up to 10GHz of



Figure 12. Minimum noise figure versus frequency.



**Figure 13.** Real  $(S_{11})$  and Real  $(S_{22})$  versus frequency.



**Figure 14** Real  $(S_{12})$  and Real  $(S_{21})$  versus frequency.

frequency range and beyond this, the change is gradual in nature.

$$S_{11} = \frac{(1 - Y_{11})(1 - Y_{22}) + (Y_{12} - Y_{21})}{(1 + Y_{11})(1 + Y_{22}) - Y_{12}Y_{21}}$$
(9)

$$S_{12} = \frac{-2Y_{12}}{(1+Y_{11})(1+Y_{22}) - Y_{12}Y_{21}}$$
(10)

$$S_{21} = \frac{-2Y_{21}}{(1+Y_{11})(1+Y_{22}) - Y_{12}Y_{21}}$$
(11)

$$S_{22} = \frac{(1+Y_{11})(1-Y_{22}) + Y_{12}Y_{21}}{(1+Y_{11})(1+Y_{22}) - Y_{12}Y_{21}}$$
(12)

In the high frequency operating range, several losses take place, so it is very essential to analyse these losses in order to characterize the device more accurately. Some of the important losses associated with the devices in the microwave frequency range are as follows (Eq. (13) to Eq. (16))<sup>19</sup>:

**Insertion loss:** 

$$10\log\frac{P_i}{P_o} = 20\log\frac{1}{|S_{21}|} = 20\log\frac{1}{|S_{12}|}$$
(13)

**Transmission loss:** 

$$10\log\frac{P_i - P_r}{P_o} = 10\log\frac{1 - |S_{11}|^2}{|S_{12}|^2}$$
(14)

**Reflection loss:** 

$$10\log\frac{P_i}{P_i - P_r} = 10\log\frac{1}{1 - |S_{11}|^2}$$
(15)



**Figure 15.** Img  $(S_{11})$  and Img  $(S_{22})$  versus frequency.



**Figure 16.** Img  $(S_{12})$  and Img  $(S_{21})$  versus frequency.

**Return loss**:

$$10\log\frac{P_i}{P_r} = 20\log\frac{1}{|S_{11}|}$$
(16)

Figures 17–20 represent the losses associated with the devices at an RF frequency range. From Figures 17 and 19 it is found that both Insertion losses and the reflection losses in the SGFD-SOI MOSFET is smaller in comparison to the double gate FD-SOI MOSFET while from the Figures 18 and 20 is found that the transmission loss and the return losses in the single gate FD-SOI MOSFET is larger as compared to the of double gate FD-SOI MOSFET.

It is obtained that the leakage current in SGFD-SOI MOSFET is lower in comparison to the DGFD-SOI MOSFET which implies that the power-dissipation (static) in the former device is lower. The transconductance and Ion/Ioff ratio of the DG MOS device is greater than that of



Figure 17. Insertion Loss versus frequency.



Figure 18. Transmission Loss versus frequency.



Figure 19. Reflection Loss versus frequency.



Figure 20. Return Loss versus frequency.

the SGMOS device and implies that the DGMOS device is suitable for fast switching and large BW applications.

Table 2 represents the RF/HF performance comparison of the designed MOS devices to that of the recently

reported MOS devices. It is found that with decrease in the channel length, (0.25  $\mu m$  in Ref. [31], 40 nm in Ref. [26] and 20 nm in this work) the value of  $g_m$  increases due to which  $f_T$  of the device also increases and follows the 1/L (L = channel length) trend, but in contrary to this it is found that the value of *FTGP* highly decreases which implies that the gain of the device decreases while switching speed increases.

## 4. Conclusion

An analysis of the RF/HF performance of the single and double-gate FD-SOI MOSFET is carried out. Also, the small signal equivalent circuits are developed in order to analyse the RF response of the device more accurately and to extract other important RF parameters.

The important FOMs used to investigate the RF/HF performance of the MOS devices are intrinsic  $C_{gs}$  &  $C_{gd}$ ,  $f_{\rm T}$  and *FTGP*. It is observed that the value of  $g_{\rm m}$  for DGFD-SOI is 38% larger than that of SGFDOI, 97% larger than GSDGFD-SOI and 89% larger than SGFD-SOI. The  $f_{\rm T}$ for DGFD-SOI is 37% larger than that of SGFDOI, 99% larger than GSDGFD-SOI and 100% larger than SGFD-SOI. The leakage current in single gate FD-SOI MOSFET is 39% smaller in comparison to the double gate FD-SOI MOSFET which implies that the static-power dissipation in the former MOS device is lower. The Ion/Ioff ratio of the double gate FD-SOI MOSFET is 103 times greater than that of single gate FD-SOI MOSFET and implies that its switching speed is higher. The derived S parameters are used to evaluate its high-frequency losses. It is observed that in the SG FD-SOI MOSFET the Insertion loss is 2.47 dB, the Transmission loss is 2.48 dB and the Reflection loss is 1.02 dB lower than that of DG FD-SOI MOSFET while the Return loss is 0.05 dB higher as compared to that of DG FD-SOI MOSFET.

 Table 2.
 The RF/HF performances comparison of the designed MOS devices to that of the recently reported MOS devices

References	Device	$V_{\rm G}(V)$	$V_{\rm D}(V)$	$C_{\rm gs}(fF)$	$C_{\rm gd}$ (fF)	$g_{\rm m}(S)$	$f_{\rm T}$ (THz)
Ref. [31]	SGFD-SOI	1.0	1.50	32.1	14.50	0.012	0.04
Ref. [26]	GSDGFD-SOI	1.0	0.50	0.771	0.301	0.003	0.52
This Work	SGFD-SOI	1.0	0.80	0.230	0.170	0.064	25.9
	DGFD-SOI	1.0	0.80	0.210	0.181	0.102	41.2

Where, SGFD-SOI = single gate FD-SOI MOSFET, DGFD-SOI = double gate FD-SOI MOSFET and GSDGFD-SOI = gate stack double gate FD-SOI MOSFET (with  $Si_3N_4$  as high-k dielectric material)

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