ISSN (Print): 0974-6846 ISSN (Online): 0974-5645

Thermal and Energy Efficient RAM Design on 28nm for Electronic Devices

Diksha Singla*, Meenal Sachdeva, Divya Malhotra and Harshmeet Singh

Chitkara University, Chandigarh-Patiala National Highway (NH-64),Punjab - 140401, India; singla145@gmail.com, meenal.official@gmail.com, malhotra95divya@gmail.com, harshmeet.28@gmail.com

Abstract

In this paper an approach is made to design a Thermal and Power efficient RAM for that reason we have used DDR3L, DDR4 and DDR4L memories and four different members of HSTL I/Os standards on 28nm technology. Every electronic device which needs read and write operation requires most energy efficient electronic system and for that very purpose we have designed the most energy efficient RAM. In this design we have taken 3 main parameters, Frequency, Temperature and Voltage. We have done our analysis using the above stated 3 parameters. We have kept the environment constant. For the simulation of the logic, Xilinx is used with Verilog as hardware description language. For different ambient temperatures and I/O standards, we have done our analysis on DDR3L, DDR4 and DDR4L RAMs. When we scaled down from 313.15K to 273.15K, we observed maximum power reduction in DDR3L. We also observed maximum power consumption on chip was from DDR3L as compared to DDR4 and DDR4L. So we used DDR4 and DDR4L in place of DDR3L and observed maximum power reduction in DDR4L. Power consumed by DDR4L on chip is least as compared to DDR3L and DDR4.

Keywords: 28nm FPGA, DDR3L, DDR4L, Energy Efficient

1. Introduction

In this paper we are going to study the most thermal and energy efficient RAM design on 28nm FPGA1. RAM or Random access memory is a type of storage or memory, which is a core function and fundamental component in computers. RAM retains digital data with the help of technology consisting of data storage device (recording device) and computer components (which are used for arithmetic and logical operations). The main function of RAM is to read and write the data in a given time period regardless of the order of data. The time required by RAM to read and write data is directly dependent upon the physical location of the storage device. There are two types of circuit, Integrated and Discrete. In the present scenario RAM is used in the form of Integrated Circuit. Integrated circuits refer to set of electronic circuits on a single chip. RAM prefers Integrated circuits over Discrete because Integrated circuits occupy very less space as compared to discrete². In our paper we have considered 28nm, which means size of chip, is 28 nano meters. In this paper 28nm from Artix 7 has been considered. The gate density of 28nm is twice as of 40nm. The chip size of 28nm has been reduced to almost half the size of previous generation 40nm. We have done our analysis based on most thermal and energy efficient designs. Energy efficient design refers to reduce the amount of energy being supplied to the product but at the same time the output should not degrade. Thermal efficiency in this paper refers to which is the best temperature at which we can operate a RAM.

We have taken 32bit RAM where din and dout signifies input and output data. Readdress is 16 bit and is used to store address from re (read) and is used when data is to be read or displayed on the system via dout. The data written or inserted into the system is taken by wr (write) line and stored at Waddress, which is 16 bit via din. Below is the schematic diagram of RAM that we have designed and considered in our paper.

^{*} Author for correspondence

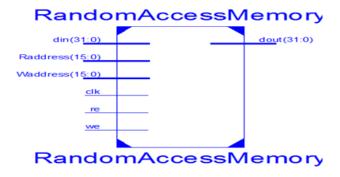


Figure 1. Schematic of Random Access Memory.

RAM is further classified into DRAM (Dynamic random-access memory) and SRAM (Static randomaccess memory)3. DRAM is a random access memory where each bit of data is stored in a separate capacitor in an IC (integrated circuit)4. SRAM is a semiconductor memory that uses bistable latching circuitry (Circuit that is stable in both the states) to store each bit. Capacitors are used to store energy. Both RAM's are used in computers. DRAM and SRAM both have their different functions depending upon their strength and capacity. DRAM has its role in primary usage when small amount of information is required. DRAM is cheaper as compared to SRAM and occupies less space therefore it is used by system memory in virtually all computers. SRAM has much faster access time and is used where small amount of work has to be done quickly or in a very short period of time. SRAM's primary usage is cache memory. Cache memory is mainly used for storing frequently used locations and instructions for faster access, which improves the overall performance of the system by reducing the time spent for searching files. SRAM is faster than DRAM because it does not require refreshing because SRAM has continuous power supply. As SRAM has more number of parts on the chip as compared to DRAM, which results in less memory per chip in SRAM. Due to this the SRAM is expensive also; this is the reason why DRAM is preferred over SRAM.

In this paper we have taken 7 series device family (Artix 7). In our paper we have considered an I/O (Input Output) standard which is HSTL. HSTL which stands for High Speed Transceiver Logic is an IO (Input Output) standard which is used for connectivity between multiple IC's (Integrated Circuits). The normal connectivity range is between 0 V to 1.8 V with variations. Connectivity or Signals both are the same things. Signals are divided into 2 types: Single-ended and differential. The device that we have considered supports only HSTL_I, HSTL_I_18, HSTL_II and HSTL_II_18 in the HSTL family. There are

total 4 classes of HSTL but we have considered only 2 classes (Class I and II)⁵.

Class I (unterminated, or symmetrically parallel terminated)

Class II (series terminated)

Class III (asymmetrically parallel terminated)

Class IV (asymmetrically double parallel terminated)

The operating voltages for the class and I/O standard that we have considered are 1.5V and 1.8V. HSTL_I and HSTL_II operate at 1.5V whereas HSTL_I_18 and HSTL_II_18 operate at 1.8V.

In our paper we have considered three types of memories: DDR3L, DDR4 and DDR4L

1.1 DDR3 SDRAM

DDR3 is defined as double data rate type three synchronous dynamic random-access memory. DDR3 is high speed successor to DDR and DDR2. This is a 3rd generation RAM. In our paper we have considered DDR3L which is a low Voltage RAM and operate at 1.35V. DDR3 operates between 800 MHz and 2400 MHz but we have done our analysis at 1600 MHz. DDR3 has increased memory clock rate, bus clock, data rate and transfer rate as compared to its successors DDR and DDR2. DDR3 has the capacity up to 8 GBs RAM per chip. It was introduced in ⁶.In Figure 2, two 4 GB RAM are used to make a 8 GB RAM.



Figure 2. DDR3 Memory.

1.2 DDR4 SDRAM

DDR3 is defined as double data rate type four synchronous dynamic random-access memory. DDR4 is high-speed successor to DDR, DDR2 and DDR3. This is a 4th generation RAM. In our paper we have considered both DDR4 and DDR4Lbecause both the memories can operate at 1600 MHz and also below the voltage range of DDR3L. DDR4L is a Low Voltage RAM and operate at 1.05V. 4th Generation RAM has increased memory clock rate, bus clock, data rate and transfer rate as compared to its successors DDR, DDR2 and DDR3.DDR4 has

a capacity up to 16 GBs with two 8 GBs in dual line memory. DDR4 was introduced in 2014. DDR4L is still under work but will work at 1.05V within the frequency range of 4th generation RAM whereas DDR4 operate at $1.2V^7$.In Figure 3, two 8 GB RAM are used to make a 16 GB RAM.



Figure 3. DDR4 Memory.

We have also done an analysis for DDR3, DDR4 and DDR4L memories without changing any I/O standard. In this analysis we have kept the default I/O standard.

When we scale down from 313.15K to 273.15K we observe there is 3.13%, 2.19% and 1.60% power reduction in DDR3L, DDR4 and DDR4L respectively as shown in Table 1.

Table 1. Analysis for default I/O standard

Temp.	DDR3L	DDR4	DDR4L
273.15K	4.665	3.746	2.939
283.15K	4.684	3.756	2.945
293.15K	4.711	3.771	2.954
303.15K	4.753	3.795	2.967
313.15K	4.816	3.830	2.987

When we are using DDR4 and DDR4L in place of DDR3L we observe at 273.15K there is 19.69% and 36.99% power reduction respectively. At 313.15K we observe there is 20.81% and 37.97% power reduction respectively as shown in Figure 4.

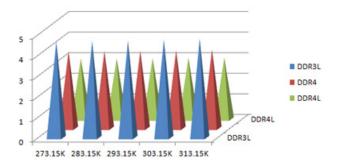


Figure 4. Power analysis for default I/Os.

2. Practical Applications of RAM

In present scenario, RAM plays an important role for every electronic device. Electronic devices, which requires read and write operations, RAM is required in such devices. RAM helps the system for fast, better and reliable performance. We use mobiles, laptops, computers and gaming devices all requires RAM. As the size of RAM increase, the performance of the electronic device also gets enhanced. Spacecrafts, Aero planes, navigator devices, robots etc. also require RAM. RAM has a very bright future. As the technology advances, the RAM also gets enhanced⁸.

Among all the memories we have considered DDR3L, DDR4 and DDR4L because a Low Voltage memory operates at the lowest voltage as compared to existing memories. Like DDR3L at 1.35V and DDR4L at 1.05V but between there voltages DDR4 also operate at 1.2V. These are the only 3 memories, which operate at these voltages. These are the RAMs, which operate below 1.35V.

3. Results and Analysis

In the result and analysis section we will discuss the total power consumption of DDR3L, DDR4 and DDR4L RAM. Here we will compare RAMs on the basis best memory in terms of power consumption and efficiency.

Below are the I/O standards that we have considered for the analysis.

3.1 HSTL I

When we scale down from 313.15K to 273.15K we observe there is 3.10%, 2.14% and 1.55% power reduction in DDR3L, DDR4 and DDR4L respectively as shown in Table 2.

Table 2. Analysis for 3 different RAM's for HSTL_I

Temp.	DDR3L	DDR4	DDR4L
273.15K	4.836	3.916	3.108
283.15K	4.855	3.926	3.114
293.15K	4.883	3.942	3.123
303.15K	4.926	3.966	3.136
313.15K	4.991	4.002	3.157

When we are using DDR4 and DDR4L in place of DDR3L we observe at 273.15K there is 19.02% and 35.73% power reduction respectively. At 313.15K we observe there is 19.81% and 36.74% power reduction respectively as shown in Figure 5.

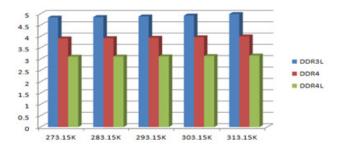


Figure 5. Power analysis for HSTL_I.

3.2 HSTL II

When we scale down from 313.15K to 273.15K we observe there are 3.08%, 2.13% and 1.55% power reduction in DDR3L, DDR4 and DDR4L respectively as shown in Table 3 and Figure 6.

Table 3. Analysis for 3different RAM's for HSTL_II

Temp.	DDR3L	DDR4	DDR4L
273.15K	4.900	3.979	3.171
283.15K	4.919	3.990	3.177
293.15K	4.947	4.006	3.186
303.15K	4.990	4.030	3.200
313.15K	5.056	4.066	3.221

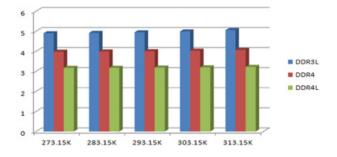


Figure 6. Power analysis for HSTL_II.

When we are using DDR4 and DDR4L in place of DDR3L we observe at 273.15K there is 18.79% and 35.28% power reduction. At 313.15K we observe there is 19.58% and 36.29% power reduction respectively.

3.3 HSTL_I_18

When we scale down from 313.15K to 273.15K we observe there are 3.07%, 2.14% and 1.55% power reduction in DDR3L, DDR4 and DDR4L respectively as shown in Table 4 and Figure 7.

 Table 4.
 Analysis for 3 different RAM's for

HSTL_I_18

Temp.	DDR3L	DDR4	DDR4L
273.15K	4.891	3.970	3.162
283.15K	4.910	3.981	3.168
293.15K	4.938	3.997	3.177
303.15K	4.981	4.021	3.191
313.15K	5.046	4.057	3.212

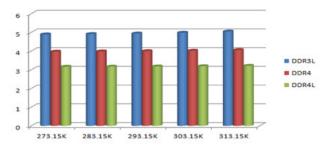


Figure 7. Power analysis for HSTL_I_18.

When we are using DDR4 and DDR4L in place of DDR3L we observe at 273.15K there is and 18.83% and 35.35% power reduction respectively. At 313.15K we observe there is 19.59% and 36.34% power reduction respectively.

3.4 HSTL_II_18

When we scale down from 313.15K to 273.15K we observe there are 3.07%, 2.14% and 1.54% power reduction in DDR3L, DDR4 and DDR4L.

When we are using DDR4 and DDR4L in place of DDR3L we observe at 273.15K there is 18.48% and 34.70% power reduction respectively. At 313.15K we observe there is 19.26% and 35.71% power reduction respectively as shown in Table 5 and Figure 8.

Table 5. Analysis for 3 different RAM's for HSTL_II_18

_			
Temp.	DDR3L	DDR4	DDR4L
273.15K	4.982	4.061	3.253
283.15K	5.001	4.072	3.260
293.15K	5.030	4.088	3.269
303.15K	5.073	4.112	3.282
313.15K	5.140	4.150	3.304

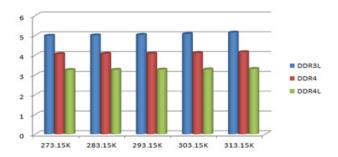


Figure 8. Power analysis for HSTL_II_18.

4. Conclusion

In our analysis we have considered only three RAM designs, which can operate at the least Voltages. We observed that DDR4L is the most power efficient RAM. DDR4L power consumption on chip at 273.15K and 313.15K are 35% and 36% approximately less as compared to DDR3L memory. When we compared the I/O standards, we found that HSTL_I is most power efficient at 273.15K and 313.15K as compared to considered I/O standards.

5. Future Scope

This design is implemented on 28nm FPGA. In future, we can go for ultra scale FPGA, System on Chip and 3D ICs based implementation. In this work, DDR4L RAM is taken for the analysis. There is an open scope to use LVTTL, LVCMOS, LVDCI, HSLVDCI, and I2C IO Standards. Using HSTL IO Standard, we can also design

Router, Microprocessors and Many more VLSI design on FPGA. RAM is not limited to any computers or laptops only, it can be used in mobiles, spacecrafts and many other electronic items.

6. References

- 1. Banijamali B, Bahareh B. Advanced reliability study of TSV interposers and interconnects for the 28nm technology FPGA. Electronic Components and Technology Conference (ECTC), IEEE 61st. IEEE; 2011.
- 2. Redwine DJ. Random access memory. U.S. Patent No. 5,008,214; 1991 Apr 16.
- 3. Parkin SSP, Roche KP, Samant MG, Rice PM, Beyers RB, Scheuerlein RE, O'Sullivan EJ, Brown SL, Bucchigano J, Abraham DW, Lu Y, Rooks M, Trouilloud PL, Wanner RA, Gallagher WJ. Exchange-biased magnetic tunnel junctions and application to nonvolatile magnetic random access memory. Journal of Applied Physics. 1999; 85(8):5828–33.
- 4. Okhonin S, Nagoga M, Sallese JM, Fazan P. A SOI capacitor-less 1T-DRAM concept. 2001 IEEE International SOI Conference, IEEE; 2001.
- 5. Esch GL, Manley RB. Theory and design of CMOS HSTL I/O pads. Hewlett Packard Journal. 1998; 49:46–52.
- 6. Kang U, Chung HJ, Heo S, Ahn SH, Lee H, Cha S-H. 8Gb 3D DDR3 DRAM using through-silicon-via technology. IEEE International Solid-State Circuits Conference-Digest of Technical Papers, ISSCC 2009, IEEE; 2009.
- Sohn, Kyomin, Na T, Song I, Shim Y, Bae W, Kang S, Lee D. A 1.2 V 30 nm 3.2 Gb/s/pin 4 Gb DDR4 SDRAM with dual-error detection and PVT-tolerant data-fetch scheme. IEEE Journal of Solid-State Circuits. 2013; 48(1):168–77.
- 8. Hiroyuki A, Shima H. Resistive Random Access Memory (ReRAM) based on metal oxides. Proceedings of the IEEE. 2010 Oct 21; 98(12):2237–51.