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A High Speed MOSFET for Switching Application

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Abstract

This work introduces a new super junction MOSFET. High switching speed is an essential parameter in this device. Negative resistance in gas electron between GaAs and AlGaAs is used to design this structure. The new designed device stores much less charges in its channel, because its junction and parasitic capacitance are small. As well, in on-state it has lower resistance relative to the traditional device. Therefore, the amount of $R_{DS} \times Q_C$ which is Figure of Merit (FOM) will decrease, enormously. The designed MOSFET has been applied in a 3–phase inverter and its performance for giving a sinusoidal output has been showed. All the simulations have been done in SILVACO software.

Keywords: Channel Charge, Inverter, Super Junction MOSFET

1. Introduction

Today, with advances in technology, foundation improvement is more important than ever. The essential note is considering power transformation and the quality of transmission to the consumer. Nowadays, there are too many advances in DC/AC converters[1–7]. A common point in all works; it is trying to reduce losses during conversion. Switching speed is an important factor in this case.

Switching losses can be divided into five parts: conduction losses, switching losses, turn off state losses, leakage current and drive losses. In most high voltage switching component applications, the latter two are negligible. Conduction losses can be reduced by reducing the on-state channel resistance. Transient time determines the switching losses, because voltage and current placed on the channel simultaneously. Increase in switching speed led to decreasing the losses. The parasitic capacitor must be very small in high speed switching devices. So, a lot of effort spent on improving the on-state resistance values of channel and parasitic capacitors. The successful generation of super junction MOSFET technology, has established a dramatic reduction in on-state channel resistance[8,9]. So, it is possible to reach the low dimension device and fast switching by decreasing the R_{DS} (on) and Gate Charge (Q_C).

However, fast transition in voltage and current in high frequency cause noise and EMI radiation[6]. To reach lower radiation, it is essential to use parasitic capacitor. There is chaotic interference between parasitic capacitor. According to recent systems procedure, increasing in efficiency is a significant goal; however, applying low speed switching in order to decrease the EMI noise is not a suitable solution. This paper discuss about charge balance in channel and procedure of device design and fabrication for fast switching.

Super junction device introduced 13 years ago and established a new foundation in high voltage power MOSFETs[10]. Drift doping and thickness in planar determine the breakdown voltage. The slope of electric field profile is proportional to drift penetration. So, thickness and low doping is an important parameter to increase the breakdown voltage[11].

Drift region play an important role in the value of on-state resistance. So the on-state resistance increases in higher voltage with low doping density and drift thickness, exponentially[11].

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Super junction technology has a deep p-type pillar in comparison to well-like traditional planar structure. Pillars limit the electric field in low density layers. Thanks to this p-type pillar, the resistance of n-type layer can reduce extraordinary in comparison to planar technology with the same breakdown voltage. This technology removes the limitations of silicon and decrease the on-state resistance to one thirtieth in each region in comparison to planar structure[12]. Also, this technology leads to non-linear parasitic capacitor and finally decreasing in switching power dissipations.

Most super junction devices use multi layers to fabricate the deep p-type pillar structure. In this structure, the important design parameters in association with on-state resistance determine with p-type pillars relative to each other and space between the cells. However, the more layers applied the more complicating and cost in the fabrication process. In this structure, decreasing the dimensions in a narrow cell is hard. High cell density effects on the on-state resistance. It's one of the multi-layer structure problems. To understand this method and lowering the cost, it has introduced the deep valley filled with crystal. In this technology, first it etched a valley in n-type layer then fills it with p-type crystal. In this way, the new technology reaches to a cell with higher active and simpler process. Filling deep valley, decrease the process steps up to 67% in relative to multi-layer[12]. Significant challenge in this technology is reaching to the uniformity after fabrication.

Crystal defect will move the electrical characteristics. So, precise control of the fabrication process is very important. After overcoming on all challenges, a super junction MOSFET device can be built which has lower on-state resistance about one fourth of super FETs, 40% smaller and the process steps are less. The lower on-state resistance, the lower on-state dissipations. In addition, because of smaller MOSFET size the whole package is smaller, finally. The aim of this work is to use carrier transfer in the real space between two materials. This feature was introduced in 1972 in a structure[13–21]. Carrier transport in the space between the two materials creates a negative resistance. In this work the GaAs/AlGaAs used to fill the tracks created in the channel. GaAs/AlGaAs and silicon are slightly different in lattice constant, so for consistency control channel MBE and MOCVD technology must be used.

2. MOSFETt Design

High voltage super junction devices decrease the on-state resistance by balanced charge theory. To design a super junction high speed MOSFET, depletion of channel is an essential parameter. Uniform electric field is another factor to consider. In super junction structure, p-type tracks in n-type channel are used to uniform the field. To depletion the channel and refine the electric field faster than traditional super junction MOSFET, the GaAs/AlGaAs materials are used in tracks instead of Si. GaAs/AlGaAs create negative resistance in channel by carrier transfer in real states between two materials. For the transfer of real space, the material with larger band gap energy must have a less mobility. This phenomenon results in a more uniform field and on-state resistance can be reduced. This is complicated and therefore no clear relationship exists. Proposed design is showed in following Figure. In this structure four tracks are intended. By increasing in tracks number and their density, channel resistance and parasitic capacitor are varied. Optimum structure earned by four tracks with 1×10^{18} cm^{-3} net doping.

Figure 1 shows the dimensions of tracks and MOSFET graphically. Now, in order to analyze the electricity characteristics in the new structure, the parasitic capacitor are considered. Because of the charge balance theory for a R_{DS} (on) with a standard MOSFET, technology offers a smaller size, it can be expected that the Super junction MOSFET parasitic capacitance is small. Figure 2 shows the input and output capacitance of new structure in comparison to traditional one. It is clear that negative resistance decreases the channel charge in order to decrease the capacitance. It's a very important characteristic in high speed switches. As it can be seen from the structure, the output capacitor value is less than old SJ MOSFET and latest SJ MOSFET. This also holds for the input capacitors and parasitic.

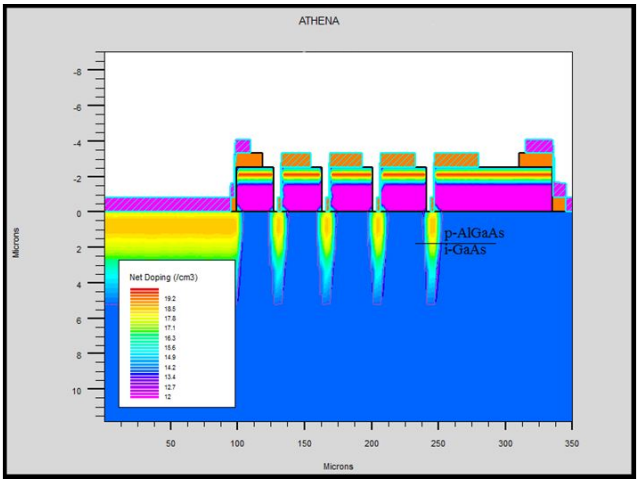

Figure 1. Proposed super junction MOSFET.

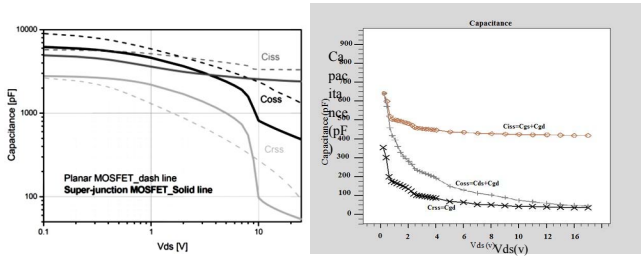

Figure 2. Comparison of capacitances between traditional super junction MOSFET[9] and this work.

This characteristic is an effective parameter in off and on process of MOSFET switches. Reducing the amount of capacitor switching losses can be done according to the following equation:

$$\int_0^{V_{DS}(on)} CV_{DS}\, dV_{DS} \qquad (1)$$

Which V_{DS} is drain-source voltage and $V_{DS\,(on)}$ is drain-source turn on voltage. This stored energy losses in each switching cycle. By reducing the value of capacitance, $\frac{dv}{dt}$ and $\frac{di}{dt}$ can vary much faster. So, the switching speed can increase with lower dissipations. However, this effect can increase the EMI noise. Switching control must omit it. To show the turn on speed of new structure, the channel voltage in turning on process is shown in following Figure. To demonstrate the new structure performance in switching, the turning speed of traditional one is shown. The applied circuit to test this characteristic is in[9].

Channel resistive calculated by following equation[18]:

$$R = AqN_s\left[\mu_1 - (\mu_1 - \mu_2)R - F(\mu_1 - \mu_2)\frac{dR}{dF}\right] \qquad (2)$$

F is the electric field, A is the area of channel square, N_s are the impurity and μ_1 and μ_2 are the materials mobility. Wise choice of motilities can make the negative resistance. In the room temperature, GaAs mobility is about 800cm^2/V-s and that of AlGaAs is about 500cm^2/V-s. These materials are suitable to form an electron gas region. In this region, electrons can move with high speed mobility, therefore, the Transient states run out faster.

According to Figure 3, transient time to turn off the traditional MOSFET is about 2.5ns, whereas, it is about 0.2ns for new structure. By considering the capacitor and channel resistance value, the decreasing in dissipations is desired.

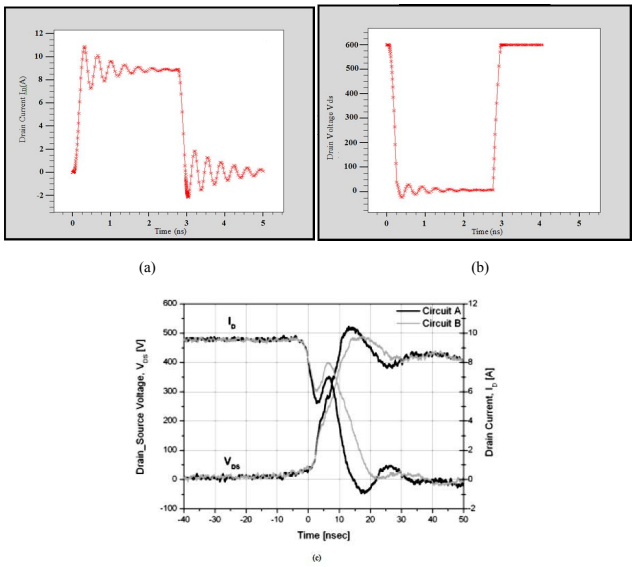

Figure 3. Transient current (a) and voltage (b) of proposed MOSFET for turning off in comparison with[9].

As seen in Figure 4, the power dissipation in turning on and off is decreased. Explanation that can be offered for turning off is that due to the high mobility of GaAs/AlGaAs, the charge stored in the channel is reduced. So, the stored charge in channel is reduced and causes decreasing the dissipation because of parasitic capacitor. In turning on, the MOSFET in this phenomenon causes the channel to be formed quickly and uniform field across the channel is established.

So with these observations, we can say that this new MOSFET is designed for superior performance and speed than SiC MOSFETs. In following, to show the new MOSFET performance in applications, it is applied in an inverter.

3. Application

High switching speed is an essential factor in the inverters. Fast switching causes increase in the output sinusoidal

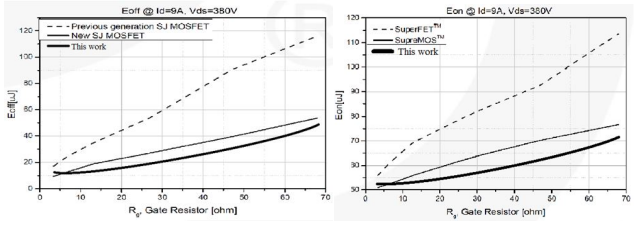

Figure 4. Losses energy in proposed MOSFET in comparison with traditional one[9] in the same conditions.

signal quality. So, it is needed in fast switches. The more switching speed, the less Total Harmonic Distortion (THD). In this work, a 3–phase inverter as shows is applied.

The traditional and new MOSFET structures are applied in the inverter. Table 1 shows the inverter parameters. Modulation index is swiped from about 0 to 0.9. The new MOSFET make a possible faster switching speed. So, as shows in Figure 6, THD is decreased.

As can be seen, the THD value has a warranted value by the new structure. The new MOSFET due to low channel resistance, low parasitic capacitance of the output, and in conclusion reduction in the $R_{DS} \times Q_S$ will give us the possibility of high switching frequency application. It is lowered to less salt obtained. Output sinusoidal voltage is the final result which presents the new structure sufficiency.

Because of low RDS resistance the drop voltage is very low. This new MOSFET structure can be used to control the speed of induction fast motors. Future of this work is applied this structure in a fast PWM frequency inverter in the induction motors.

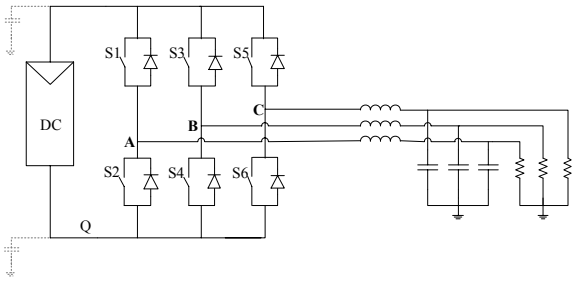

Figure 5. Applied typical inverter to test the new MOSFET structure.

Table 1. Inverter parameters

Circuit element	Value	Description
V_{DC}	600V	PV array voltage
C_{DC}	300µf	DC capacitor
C_P	120nf	Parasitic capacitor between PV array and ground
L_f	2.2mH	Inductance of three phase filter
C_f	3µf	Capacitor of three phase filter
R_{Load}	8Ω	Grid load
F_{sw}	8kHz	Switching frequency

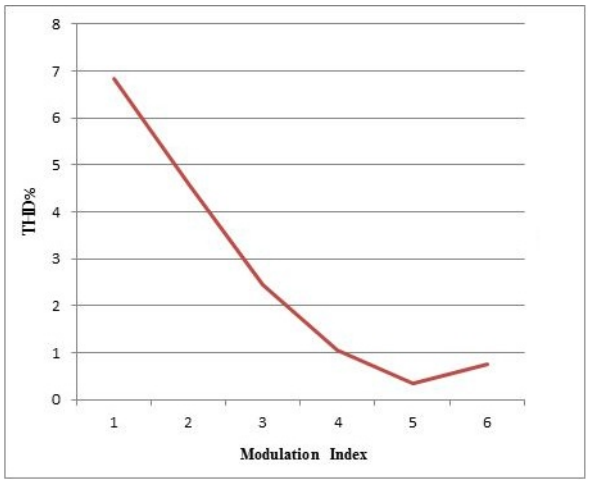

Figure 6. THD in the 3-phase inverter in permissive range.

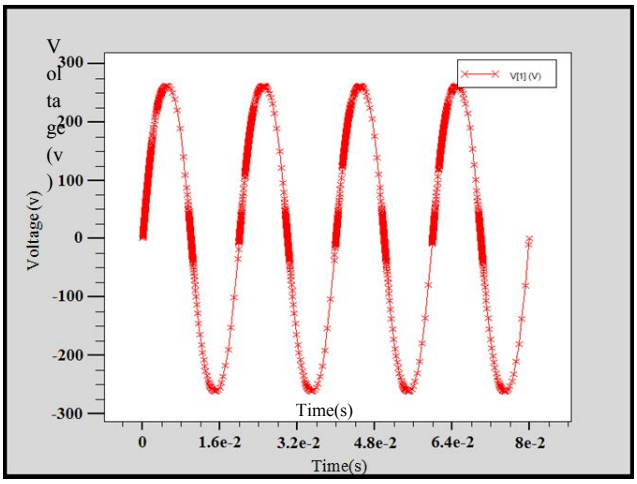

Figure 7. Output voltage of inverter that applied the proposed MOSFET.

4. Conclusion

Super junction MOSFETs have been known as the fastest switching MOSFETs. Lower dissipations have made valuable this type of switch. MOSFET presented in this work, in terms of on-state resistance and charge stored in the channel, showed more superior than the traditional one. The response of the GaAs/AlGaAs hetero structure MOSFET is much faster than that of Si MOSFETs, due to the electron gas formation at the interface of GaAs/AlGaAs and also higher electron mobility of GaAs. The results presented the very good performance for new MOSFET. Only inevitable option is the cost of fabrication of the new MOSFET compared with traditional

super junction MOSFET. Both of them fabricate by MBE system. However, special considerations must be made to allow for the fabrication of the new transistor with silicon and GaAs/AlGaAs together.

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