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Analysis and Design of SDF Architecture for MIMO Application

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Abstract

Background/Objectives: Fast Fourier transforms (FFT) has become ubiquitous in many engineering applications. FFT is one of the most employed blocks in many communications and signal processing systems. This paper aims in designing SDF architecture for efficient FFT algorithms.**Methods/Statistical analysis**: Efficient algorithms are being designed to improve the architecture of FFT.Higher Radix FFT algorithms have the traditional advantage of using less numbers of computational elements and are more suitable for calculating FFT of long data sequence.**Findings:**In designing SDF architecture for efficient FFT algorithms like Radix 2, Radix 4 and Radix 2^2,thedesigns are compared by performing simulations using VERILOG HDL and power analysis. The comparison includes the number of logic gates used by every architectures and their power dissipation using various devices. Trade-off between accuracy, speed, hardware complexity and power consumption should be made so as to choose the best fit architectures for the given application.**Improvements/Applications:**From the comparison results, best fit architecture is chosen and is implemented at the software level for the desired device for the Multiple Input Multiple Output (MIMO) application using Orthogonal Frequency Division Multiplexing (OFDM) employed in 4G technologies.

Keywords: Fast Fourier Transform (FFT), Multiple Input Multiple Output (MIMO), Pipelined FFT, Power Analysis

1. Introduction

Digital Signal Processing (DSP) is the mathematical calculation of an information signal to vary or enhance it in some way. It is categorized by discrete time, discrete frequency, or other discrete domain signal.

Modern signal and image processing would be impossible without DFT. It is a transform in which every time domain signal is converted into a frequency domain signal. This transformation helps user in performing various required operations over the input signal with less error. After completing the desired process, it can be converted back to its original time domain form by using Inverse Discrete Fourier Transform (IDFT). DFT pair is given by,

$$X(k)=\sum_{n=0}^{N-1} x(n) e^{\frac{-j2\pi kn}{N}}$$

$$x(n)=\frac{1}{N}\sum_{K=0}^{N-1} X(k) W_N^{-nk}$$

Equation 1. DFT pair

where, = twiddle factor = $e^{-j2\pi/N}$.

Direct computation of DFT for a given input signal requires large amounts of computational speed and time. It is also quite complex if the number of inputs is more. To have speedy computation and to perform complex multiplication effectively, the twiddle factors of DFT sequence are decomposed as a matrix and it is used. This

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technique of transformation is referred to as FFT. Major properties employed in FFT are symmetrical and periodicity property. Various FFT applications are image processing, speech processing, spectrum analysis and OFDM applications.

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2. Proposed Work

In this paper, we design various FFT architectures using DIF algorithm. In this algorithm, the input sequence is taken in the normal order and is then converted into a frequency domain sequence using the butterfly diagram. The obtained frequency domain signal is in bit reversed order[1].

The most commonly used algorithm is DIF algorithm as the architectural design may be made simpler as it does not require any circuit that re-orders the given input sequence, also reordering at output side will not increase complexity to design in a larger extent[2].

2.1 RADIX 2 FFT

Radix 2 algorithm is the most common algorithm that follows Cooley-Tukey FFT[3]. In this algorithm the length of the sequence is expressed only as powers of 2[4]. If N represents the length of the sequence, then for the Radix 2 algorithm, it should be of the form N= Where m represents the number of stages[5]. The butterfly unit of Radix 2 is as follows (Figure 1).

2.2 RADIX 4 FFT

In this algorithm, the length of the sequence is represented in powers of 4. If N is the number of input signals, then it can be expressed as $N=4^m$ where m refers to the number of stages and the butterfly unit is as follows (Figure 2).

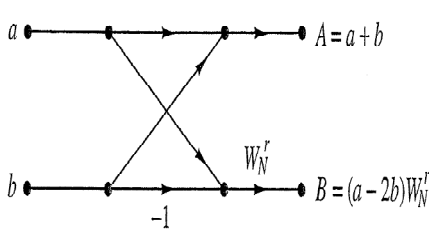

Figure 1. Radix 2 Butterfly unit.

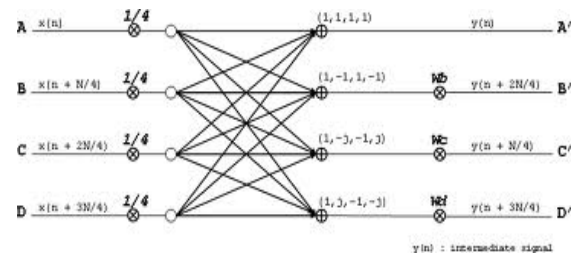

Figure 2. Radix 4 Butterfly unit.

2.3 RADIX 2^2 FFT

This algorithm computes Radix 4 a more simplified manner using the butterfly unit of Radix 3 algorithm. we generate Radix 4 using Radix 2 butterfly unit by using this algorithm. This reduces the complexity of the design[6]. This algorithm has its butterfly unit as follows (Figure 3).

3. Pipelined FFT Architectures

It is a kind of architecture which uses the feedback and delays in their design there by computing the FFT. In such a case the size of memory required is reduced to a greater extent. The common Pipelined architectures are listed below.

- Single Path Delay Feedback Architecture
- Single Path Delay Commutator Architecture
- Multiple Path Delay Commutator Architecture

This paper deals with Single Path Delay Feedback (SDF) Architecture for various algorithms mentioned above. SDF uses the registers more efficiently for storing the butterfly output as feedback shift registers. Its memory requirement is minimal. The general schematic representation of SDF architecture as follows (Figure 4). In this SDF, Single input is fed into the butterfly unit leaving one output and remaining outputs are fed back into the butterfly unit through the feedback shift register. This operation continues until all the inputs are processed.

3.1 R2SDF

A single data stream goes through the multiplier at every stage. Architecture of R2SDF is as follows (Figure 5). In R2SDF, a single input is given to butterfly unit and one output obtained is delayed and given as feedback to this butterfly unit, thus computes the DIF output sequence. A sequence of butterfly unit with a delay feedback is designed

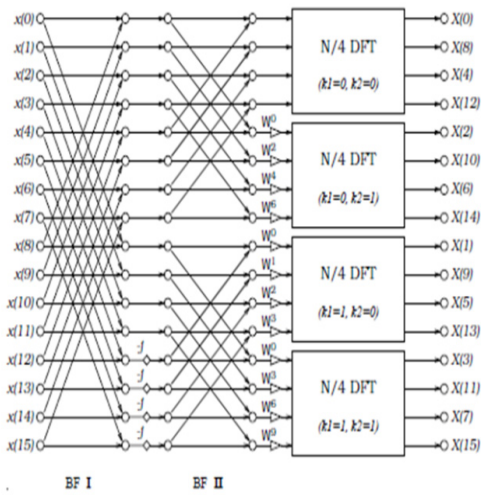

Figure 3. Radix 2^2 Butterfly unit.

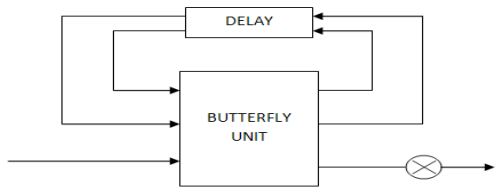

Figure 4. Schematic of SDF.

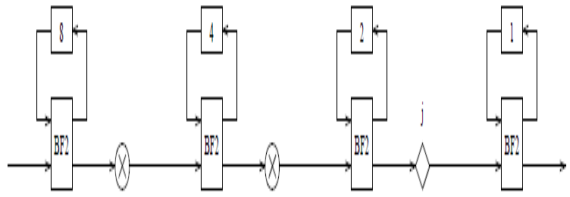

Figure 5. R2SDF architecture.

until the required number of stages is reached. This FFT output can be obtained through this architecture.

3.2 R4SDF

R4SDF was proposed as a Radix 4 version of R2SDF, employ as CORDIC iterations. It is very similar to the R2SDF architecture[7]. Its architecture is enumerated as follows (Figure 6). In R4SDF, a single input is given to butterfly unit. Three outputs obtained are delayed and given as feedback to this butterfly unit, thus computes the DIF output sequence. A sequence of butterfly unit with a delay

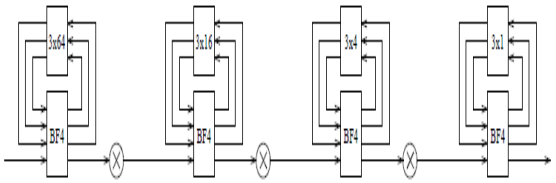

Figure 6. R4SDF architecture.

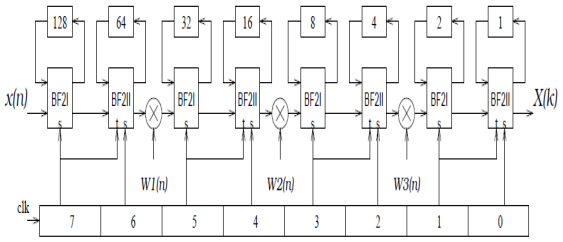

Figure 7. $R2^2SDF$ architecture.

feedback is designed until the required number of stages is reached. This FFT output can be obtained through this architecture.

3.3 $R2^2SDF$

$R2^2SDF$ architecture is designed with the help of a butterfly unit of Radix[8].In $R2^2SDF$, a single input is given to the butterfly unit 1. Output similar to Radix 2is obtained and it is delayed and given as feedback to this butterfly unit 1. This is then given to the next butterfly unit 2 and some delay is used according to the requirements and this computes the DIF output sequence. A sequence of butterfly unit with a delay feedback is designed bythe architecture of $R2^2SDF$ is as follows (Figure 7).

4. Application

From the comparison table 1, it is clear that $R2^2SDF$ has the best efficiency result than the other two architectures. Thus, this architecture considers the best fit architecture and is used in the implementation of MIMO applications[9]. MIMO means Multiple Input Multiple Output; it enhances the data rate and link reliability[10]. The communication performance is improved by the use of multiple antennas at both transmitter and receiver. MIMO architecture is as follows (Figure 8).

MIMO is classified into three main phases, namely coding, spatial multiplexing and diversity coding[11]. The

MIMO architecture composed of two butterfly units as follows (Figures 9 and 10).

In BFI structure, the muxes and demuxes at both input and output of the BF_RAMs are controlled by the control signals, i.e., c1 and c2 where the control signals are supplied by BFI controller. While the computation unit is controlled by c1 control signals.

WiMAX supports 1Rx and 2Rx, LTE supports 1Rx, 2Rx and 4Rx. Based on the requirement extra buffers can be extended to the existing BF structure[12].

In BFII structure, the multiplication –1, +j and –j is controlled by two control signals c1 and c2 (basic computation unit). The muxes and the demuxes are controlled by another pair of control signals, i.e., c3 and c4. The product with –j term is implemented by exchanging the real and imaginary parts considering the sign of the sample used[13].

5. Results

Waveforms of R2²SDF and MIMO using R2²SDF Architecture are shown in the Figures11 and 12. These Waveforms are obtained from the ModelSim Simulator by simulating Verilog HDL codes of respective Architectures.

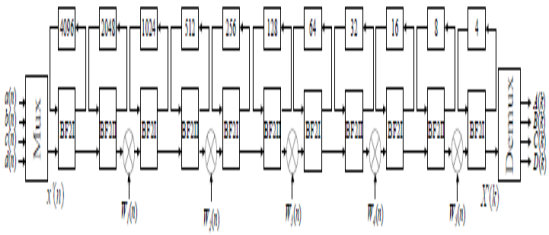

Figure 8. MIMO Architecture.

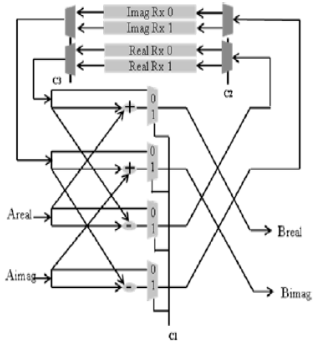

Figure 9. Internal structure of BFI.

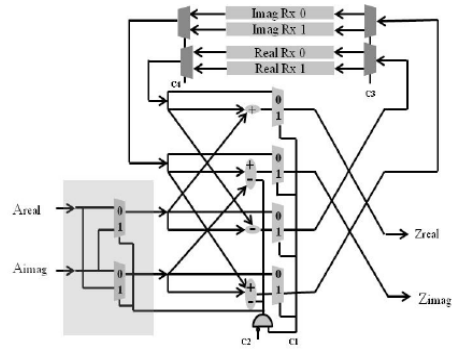

Figure 10. Internal structure of BFII.

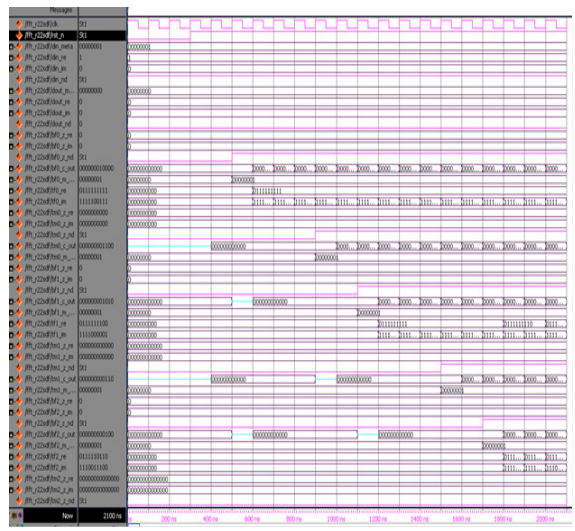

Figure 11. R2²SDF output wave.

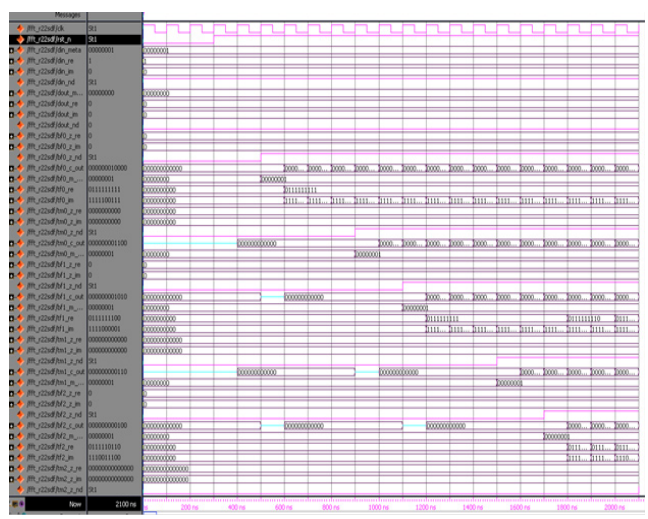

Figure 12. MIMO using R2²SDF Architecture.

Table 1. Power Analysis

Parameters	R2SDF	R4SDF	$R2^2SDF$
Io Thermal Power Dissipation	24.09mW	20.44mW	18.78mW
Average Fan Out	2.21	2.11	2.28

Table 2. Power Analysis for Different Devices

Device	R2SDF (mW)	R4SDF (mW)	$R2^2SDF$ (mW)
Cyclone II	54.76	39.86	42.19
Cyclone III	64.98	63.28	63.36
Startix II	360.67	339.48	344.10
Stratix II GX	545.37	519.55	528.12
Stratix III	408.32	404.63	405.66

Power Analysis of different architecture is compared and shown in the Table 1. Power is also obtained from various devices shown in Table 2.

6. Conclusion

In this paper, various architectures of FFT are designed and simulated using VERILOG HDL. The power dissipation and fan out conditions are computed under various devices using QUARTUS tool. From the comparison, the best fit architecture is employed in MIMO application used for 4G technologies.

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