A Systematic Approach to CMOS Low Noise Amplifier Design for Low Power Transmission

Twinkle Sinha^{*}, P. Saisharan, K. Mugesh Kumar and T. Deepa

Department of Telecommunication, SRM University, Kattankulathur - 603203, Tamil Nadu, India; twinklesinha511878@gmail.com, saisharan.p@gmail.com, blackpearlson@gmail.com, deepa.t@ktr.srmuniv.ac.in

Abstract

Recent interest in 60 GHz band for high-density and short range wireless links has led to significant progress in milli-metre (mm) wave radio systems. The Low Noise Amplifier (LNA) serves as the first component in the Radio Frequency (RF) transceiver system. The performance of LNA determines the sensitivity and selectivity of the system. In order to maximize performance gain, Noise Figure (NF) and input matching of LNA need to be optimized. A LNA for 60 GHz is designed. The main topology used in our design is cascode with a middle inductor and a Common Source (CS) configuration. The design is laid out on 130 nm CMOS standard technology. LNA is designed using classical noise matching techniques. Simulated results shows a very low noise figure of 1.3 dB with a gain of 9.8 dB and the reflection coefficientis-11.5 dB. The proposed LNA can be very well used in biomedical applications in research areas like neurology and other short range applications.

Keywords: CMOS, Cascode Topology, CS Configuration, 60 GHz, LNA

1. Introduction

Recent interest in the 60-GHz band for high-density, short-range wireless links haveled to significant progress in the development of integrated circuits for low-cost mm-wave radio systems^{1,2}. 57-64 GHz is an unlicensed frequency band^{3,4}. It can be used for short range gigabit wireless communication systems⁵. The main function of an LNA is to amplify extremely low signals and is used at both the transmitter and the receiver side without adding noise, thus preserving and maintaining the required Signal to Noise Ratio (SNR) of the system and operates at extremely low power levels. Also for large signal levels the LNA eliminates channel interference by amplifying thereceived signal without introducing any distortions⁶. Obtaining high gain with considerable noise figure along

with proper input and output matching is a challenging work while designing an LNA.

Class A amplifier has bias point more or less at the centre of maximum voltage and current capability of the device used. So basically the LNA always operates in the same region as that of the class an amplifier mostly at 15-20% of its maximum useful current⁷.

Carefully selecting the transistor and having proper understanding about various parameters and their respective trade-offs can help us meet most conditions met without using feedback arrangements. Proper Transistor selection is the first and most important step in an LNA design.

Millimetre wave radio frequency transistors have traditionally been the domain of III-V compounded semiconductors such as GaAs and InP, an increasing

^{*} Author for correspondence

number of 60-GHz blocks and systems have been recently reported in advanced SiGeBi-CMOS and CMOS technologies to meet the cost, size and power consumption needs of the consumer^{8,9}. The transistor needs to exhibit proper S parameters and have a low noise figure and good performance with lowest possible current consumption and preserving the matching of the design at the same time along with proper linearity. The cascode topology have been implemented which provides better isolation, improved bandwidth, higher gain even at millimetre wave frequencies.

In this paper, we design a LNA for 60 GHz which is based on cascade topology with a middle inductor. The remaining paper is organized as follows: Section 2 focuses on the CMOS LNA topology that has been used in this paper. The design methodology for the mm-wave CMOS LNA is presented in Section 3. Section 4 shows the schematic of the LNA and Section 5 showing the simulation results.

2. CMOS LNA Topology

CMOS technology has low current drive and power dissipation when compared to BJTs, HEMTs and any other semiconductor group technologies. Using of BJT is one of the most famous ways of designing an LNA; HEMTs came into the role for high frequency systems or block design. Here we are using CMOS in our design. Common-Gate and cascode amplifier is the two common ways of designing an LNA for CMOS technology. The Common-Gate stage provides a wide-band input matching and also has ahigh noise figure^{10,11}.

The main topology used in our design is cascode with a middle inductor. This is also called as source degenerative cascoded topology.

The cascode topology shown in Figure 1 provides better isolation, improved band width and higher gain even at millimetre wave frequencies. For the tuning out of the middle pole of cascode a series inductor is always placed between the common source and common drain. For any LNA design we prefer to have higher value of f_t , so an optimal value of the middle inductor has to be chosen by simulating f_t and noise figure for the whole cascode with inductive broad banding, as a function of L_M .

Although the cascode topology has higher gain, larger output impedance and flat I_{ds} -V_{ds} characteristic,

the single-transistor CS configuration is advantageous in terms of the lower supply voltage required, leading to higher efficiency and good linearity².

Here in the given design of the LNA consists of both cascode topology and the single-transistor CS configuration techniques. This leads to the better performance of the system.

3. Design Procedure

Using the above mentioned topology and techniques, a three stage LNA is designed with CMOS transistors. Firstly a paper pencil design is made using the transistor considerations and then simulating using ADS. The design steps are follows:

Step 1: Consider a bias current for the required application. For the present system design $I_{bias} = 5$ mA.

Step 2: The trans-conductance of the system should be selected in such a way that it prevents the inversion of the transistor¹³. The transistor inversion plays an important role at high frequencies like 60 GHz. The relationship between I_{bias} and trans-conductance (g_m) can be established as follows $g_m = K^*I_{bias}$ where K is an integer. This conditions help in maintaining the weak inversion where 'K' can range from 10 to 25.

Step 3: The saturation voltage of the transistor is determined by the width and length of the transistor along with the transconductance parameter. The saturation voltage of the transistor plays the critical role in maintaining the linearity. This voltage varies according to the frequency of operation. The width and length of transistor can be calculated by

$$\frac{W}{L} = \sqrt{\frac{2 \,\mathrm{x} \,\mathrm{I}_{\mathrm{bias}}}{\mathrm{K'} \,\mathrm{x} \,\mathrm{V}_{\mathrm{ext}}^2}} \tag{1}$$

$$V_{sat} = \sqrt{\frac{2 \text{ x } I_{\text{bias}}}{K' \text{ x} \left(\frac{W}{L}\right)}}$$
(2)

Step 4: A bypass capacitor should be placed between the gate and source which helps in matching of the input.

The capacitor can be selected with the help of oxide density of the transistor. This helps in better performance of the transistor and its matching with external component.

$$C = \frac{2}{3}$$
 x Oxide density x W x L

Step 5: To provide matching at the input with 50 Ω input matching. An external inductor value is determined using the matching technique.

$$g_m = \frac{L_s}{C} = \text{matching impedance}$$
(5)

Step 6: To provide the matching at the output and L and C is tuned to the output matching impedance.

Step 7: Using the tuning technique for 60 GHz frequency the second and third stage is developed with common source configuration.

4. Circuit Design

The complete design of the 3stage LNA with source degenerative inductive and common source topologies is shown in Figure 2.

5. Simulation

The above circuit shown in Figure 2 is simulated using

ADS and the output of the circuit is measured using the parameters reflection coefficient, gain and minimum noise figure.

Figure 3 shows the obtained graph for S_{11} vs. frequency where the obtained S_{11} is -11.5 dB. Figure 4 which show the plot for Noise Figure vs. frequency where the Noise Figure obtained is 1.3 dB. Which is followed by Figure 5 shows the graph for gain vs. frequency where the obtained gain is 9.8 dB.



Figure 3. Illustrates S_{11} at 60 GHz.



Figure 2. Schematic of LNA design.



Figure 4. Illustrates noise figure at 60 GHz.



Figure 5. Illustrates gain at 60 GHz.

6. Conclusion

From the designed LNA we observe that a good tradeoff is maintained between noise figure and gain with minimum reflected signal at the input. Using CMOS sufficiently low noise figure and good linearity is maintained throughout the system and also sufficient gain is obtained by maintaining the low power. This work is expected to be continued in order to increase the gain with considerably low noise figure further. The reflection coefficient for the designed LNA is -11.5 dB with the gain of 9.8 dB and noise figure of 1.3 dB.

7. References

- Yao T, Gordon MQ, Keith KW, Tang K, Yau HK, Yang MT, Schvan P, Voinigescu SP. IEEE algorithmic design of CMOSLNAs and PAs for 60-GHz Radio. IEEE Journal of Solid-State Circuits. 2007 May; 42(5):1044-57.
- Alldred D, Cousins B, Voinigescu SP. A 1.2 V, 60 GHz radio receiver with on-chip transformers and inductors in 90 nm CMOS. Proceedings of IEEE Compound Semiconductor Integrated Circuits Symposium; 2006 Nov. p. 51–4.
- Kang K, Lin F, Pham DD, Brinkhoff J, Heng CH, Guo YX, Yuan X. A 60-GHz OOK receiver with an on-chip antenna in 90 nm CMOS. IEEE J Solid-State Circuits. 2010 Sep; 45(9):1720-31.
- 4. Nguyen TK, Kim CH, JuIhm G, Yang MS, Lee SG. CMOS low-noise amplifier design optimization techniques. IEEE Trans Mircrow Theory Tech. 2004 May; 52(5):1433-42.
- Wang C, Hao Y, Haiying Z, Kang K, Tang Z. A 60 GHz LNA with 4.7 dB NF and 18 dB gain using inter-stage impedance matching technique in 90 nm CMOS. IEEE International Conference on Microwave Technology and Computational Electromagnetics (ICMTCE); Beijing, P. R. China. 2011. p. 270-3.
- 6. Prabhakaran G, Kannan V. Design and analysis of high gain, low power and low voltage a-Si TFT based operational amplifier. Indian Journal of Science and Technology. 2015 Jul; 8(16). doi no:10.17485/ijst/2015/v8i16/59228
- Pasricha R, Sharma S. Linearization of volterra series model power amplifier for wideband WCDMA base stations. Indian Journal of Science and Technology. 2009 Mar; 2(3). doi no:10.17485/ijst/2009/v2i3/29409
- Doan CH, Emami S, Niknejad AM, Brodersen RW. Millimeter-wave CMOS design. IEEE J Solid-State Circuits. 2005 Jan; 40(1):144–55.
- Razavi B. A 60-GHz direct-conversion CMOS receiver. IEEE International Solid-State Circuits Conference (ISS-CC) Digest of Technical Papers; 2005 Feb. p. 400–1.
- Doan C, et al. Millimeter-wave CMOS design. IEEE JSSC. 2005 Jan; 40(1):144-55.
- 11. Razavi B. A 60-GHz direct-conversion CMOS receiver. Proceedings of IEEE ISSCC; 2005 Feb. p. 400-1.
- 12. Yao T, Gordon M, Yau K, Yang MT, Voinigescu SP. 60-GHz PA and LNA in 90-nm RF-CMOS. 2006 Jun 11-13.
- Sappal AS, Patterh MS, Sharma S. Mathematical modeling of power amplifier with memory effects. Indian Journal of Science and Technology. 2009 Mar; 2(3). doi no:10.17485/ ijst/2009/v2i3/2940