

Study and Analysis of CMOS Carry Look Ahead Adder with Leakage Power Reduction Approaches

Damarla Paradhasaradhi*, K. Satya Priya, K. Sabarish, P. Harish and G. V. Narasimharao

Department of Electronics and Communications Engineering, K L University, Guntur – 522502, Andhra Pradesh, India;
dparadhasaradhi@gmail.com, satyapriyamahi@gmail.com, sabarish417@gmail.com,
p.harish150794@gamil.com, venkatanarasimharao94@gmail.com

Abstract

Background/Objectives: This paper represents the implementation of carry look ahead adder using different leakage power reduction techniques like sleepy approach, stack approach, sleepy stack approach and sleepy keeper approach. Effecting the static power dissipation high, the threshold voltage (V_{th}) is reduced that has granted tremendously towards the growth in the sub threshold leakage power. Here conventional 4-bit carry look ahead adder is designed by adopting 1-bit full adders and carry look ahead blocks. **Methods/Statistical Analysis:** In this paper, an extensive study and analysis of different leakage power minimization approaches have been implemented. In the comparative analysis carry look ahead adder is designed using different leakage power reduction approaches like sleepy, stack, sleepy stack and sleepy keeper. The circuits are implemented on Tanner EDA tool at 250nm Technology and considered PMOS, NMOS as typical models. From this paper work that only an applicable selection of leakage power reduction approach for a particular function will be well borne by a Very Large Scale Integrated (VLSI) circuit design depend on progressive analytical method. **Findings:** The average power, delay and number of transistors are calculated in the tanner tool for carry look ahead adder using all the four approaches. **Applications/Improvements:** The analytical study is implemented in the real time applications while constructing adders.

Keywords: Conventional CMOS, Leakage Power, Power Dissipation, Reduction Technique, Sleepy Keeper

1. Introduction

In CMOS technology threshold voltage and feature size are reducing for many years to accomplish high performance and high density¹. Owing to this technology trend, transistor discharge power has exponentially increased. Short channel length lead to increase in sub threshold leakage current because of the feature size becomes smaller. As transistors could not be turned off fully low threshold voltage additionally leads to increase in sub threshold discharge current. Due of these reasons, Dissipation of leakage power have grown into a major part of total consumption of power for the existing and forthcoming silicon technologies^{2,3}. Various VLSI approaches are present in most of the circuits to diminish leakage power. Every single

method delivers an adequate approach for leakage power reduction.

In the VLSI systems, the full adder circuit is employed in arithmetic operations corresponding to multiplication and addition. It is used in many applications such as VLSI, microprocessors, image process and digital signal process. Majority of these systems are based on circuits performance, variety of transistors, area of the chip, circuit speed, leakage of threshold and therefore the most significant is power consumption⁴.

The *full adder* circuit performs the addition of three binary numbers and gives the output of two binary numbers i.e., a sum and a carry. Using basic full adder, carry look ahead adder is designed. In this adder carry generator gets the output carry and carry propagator propagates the carry

*Author for correspondence

to the following level⁵. Regardless of input carry is implemented in four completely different approaches such as sleepy technique, stack technique, sleepy stack technique and sleepy keeper technique⁶. Carry-look ahead adder decreases time consumption which is needed to estimate carry bits by improving the speed.

In this paper work is structured as: section 2 labels various leakage power reduction approaches, section 3 explains design of conventional (basic) CMOS based full adder and with different leakage power reduction techniques for CMOS based full adder, section 4 describes conventional CMOS based 4-bit carry look ahead adder and also implemented via different leakage power reduction techniques. The simulated results are evaluated in the section 5; conclusion is discussed in section 7.

2. Leakage Power Reduction Approaches

Different approaches are available for reduction of leakage power that depends on two operational modes of the system. They are Standby mode (idle mode) and Active mode. In these techniques power reduction is done by blocking the main power supply of the circuit in an idle operational mode⁷. In this paper four approaches are implemented for the analysis of both 1-bit full adder and Carry look ahead adders.

- 2.1. Sleepy Approach
- 2.2. Stack Approach
- 2.3. Sleepy Stack Approach
- 2.4. Sleepy Keeper Approach

2.1 Sleepy Approach

In sleepy approach extra PMOS based transistor is connected within the V_{DD} and the pull up structure, the structure presented in the Figure 1, also in the same method NMOS transistor also added within pull down network and GND. Together the NMOS and PMOS sleepy transistors are in OFF state if the circuit is in idle mode and is in ON state if the circuit is in active mode⁸. The sleepy transistors in the circuit disconnect the power supply during OFF state. NMOS sleep transistor will be considered to control GND and hence it is called as footer switch. PMOS sleep transistor will be considered to control V_{DD} and hence it is called as header switch.

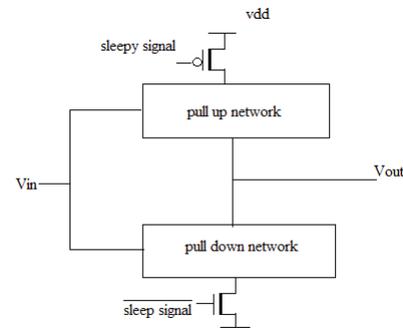


Figure 1. Sleepy approach.

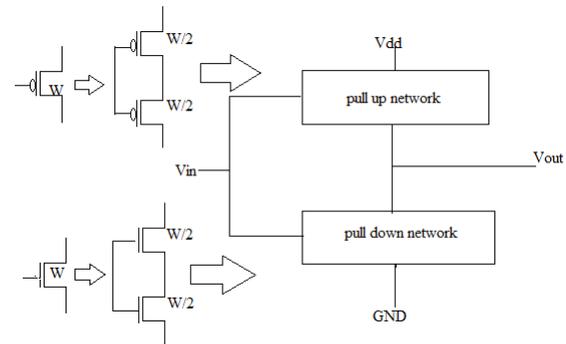


Figure 2. Stack approach.

2.2 Stack Approach

In this approach every single transistor of length (L) and the width (W) is divided into two equal transistors of having length (L) and width as ($W/2$) as shown in Figure 2. Stack approach is preferred in active mode for reduction of leakage currents⁹. Leakage current declines whenever two or more series transistors are in off state, and the reverse bias calculated between both the transistors which reduces sub-threshold leakage power⁴. This approach also called as a Forced Stacking tactic.

2.3 Sleepy Stack Approach

The basic concept in sleepy stack approach is to join the sleep transistor technique while in operative mode with that of the stack technique while in idle mode. This breaks down actual transistor into two equal sized transistors standard like in the stack approach, and then the sleep transistors s and s' are attached in equivalent to each of the branched transistors as presented in the Figure 3. Whenever the circuit is in standby (idle) mode the two transistors that connected in parallel become on, therefore the efficient resistance of the circuit is decreased and

this concludes in terms of less propagation delay¹⁰. If the circuit is in OFF mode, the sleepy transistor is idle mode and stack transistor decreases the leakage current.

2.4 Sleepy Keeper Approach

In the sleepy keeper approach an another circuit of both PMOS and NMOS laying similar to each other is added above and below pull up and pull down setups respectively. Normally PMOS transistor is good for '1' and NMOS transistor is good for '0'. Performance of PMOS transistor degrades while passing through ground and performance of NMOS transistor degrades while passing through V_{DD} . However, to preserve '1' in OFF state, given that the '1' value has already been calculated while the circuit is in sleep operation and NMOS transistor is attached to supply voltage V_{DD} to retain output significance as '1'. Similarly, the value of '0' has already been calculated that is PMOS transistor which is associated to GND to retain the output value as '0' while in off state to preserve '0' in sleep mode¹¹. When in sleep mode, sleep transistor becomes off state, and then the only PMOS transistor is acts as source for the GND. From Figure 4, there is a

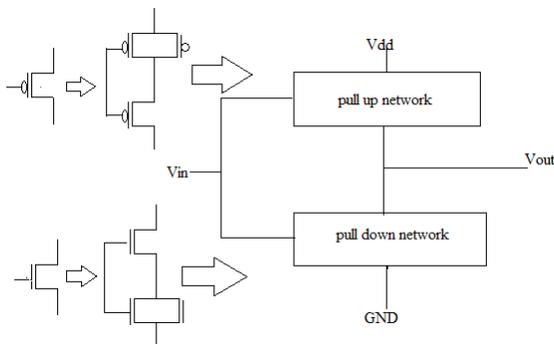


Figure 3. Sleepy stack approach.

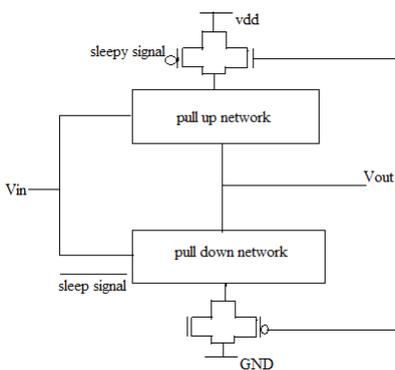


Figure 4. Sleepy keeper approach.

further only one NMOS transistor which is connecting power supply to the pull-up network. The only one source of V_{DD} in the sleep mode is NMOS transistor.

3. Implementation of CMOS based Full Adder

In this section CMOS based full adder is implemented by using four different leakage power reduction approaches as discussed above.

3.1 Conventional CMOS based Full adder

In general, full adder circuit comprises of three inputs are defined as A, B, C_{in} and the outputs are defined as Sum(S) and the Carry (C_{out})¹². The logical expressions for Sum and the Carry are given by.

$$\text{Sum} = A \oplus B \oplus C_{in} \text{ and } \text{Carry} = AB + BC_{in} + C_{in}A$$

To design both sum and carry using CMOS based conventional full adder 36 transistors are required as shown in Figure 5. This CMOS based full adder considered as conventional model for the implementation carry look ahead adder.

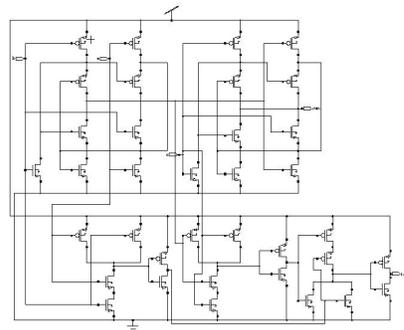


Figure 5. Conventional CMOS based full adder.

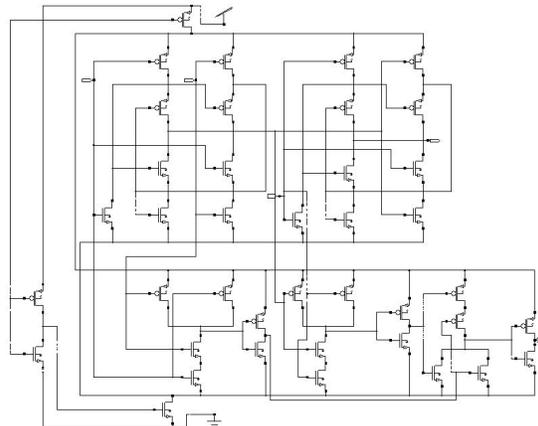


Figure 6. CMOS based full adder using sleepy approach.

3.1 CMOS based Full Adder using Sleepy Approach

As discussed in sleepy approach in the section II, two sleep transistors are required that is one PMOS transistor is placed at node 1 and another NMOS transistor is placed at node 2 as shown in Figure 6. The sleepy transistors S and S' becomes ON if the circuit is in idle condition and it changed to OFF when the circuit will be in standby condition. These sleep transistors are benefit for leakage power minimization.

3.2 CMOS based Full Adder using Stack Approach

In stack approach each transistor width sized 'W' is substituted with two equal length of transistors of width sized 'W/2' as presented in Figure 5, each transistor width is given by 'W'=2.50u and according to stack approach it is divided into two equal length transistors of equal width sized 'W/2'=1.25u is presented in the Figure 7. By increasing the transistor count that are connected in stack model, more leakage power minimization can be achieved.

3.3 CMOS based Full Adder using Sleepy Stack Approach

The Sleepy stack technique motto is the grouping of sleepy approach and the stack approach. The structure of the CMOS based Full adder using sleepy stack approach is shown in Figure 8. Each transistor have been divided

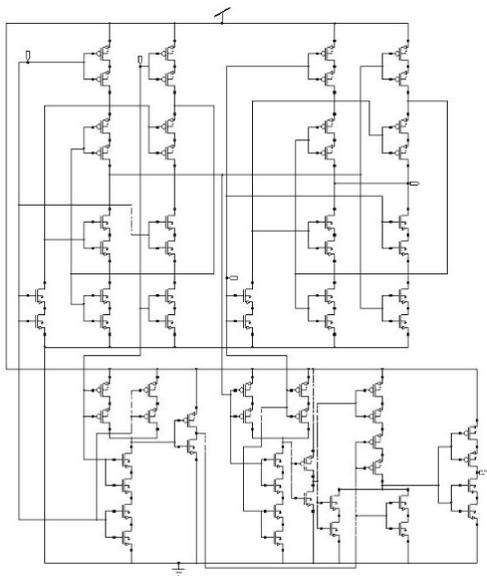


Figure 7. CMOS based full adder using stack approach.

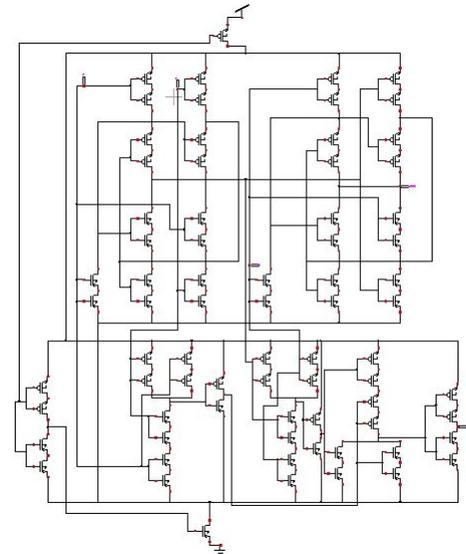


Figure 8. CMOS based full adder using sleepy stack approach.

into half and sleep transistors that are PMOS, NMOS can be placed above the pull up system and below the pull down system respectively by maintaining equivalent input capacitance³.

3.4 CMOS based Full Adder using Sleepy Keeper Approach

In sleepy keeper approach NMOS transistors are arranged parallel to the sleepy transistor of pull up network to give power supply in sleep mode when the other PMOS is in off. Similarly a PMOS transistor is connected similar to the pull down sleepy transistor to maintain output value as "0". The structure of CMOS based full adder using sleepy keeper approach is presented in the Figure 9.

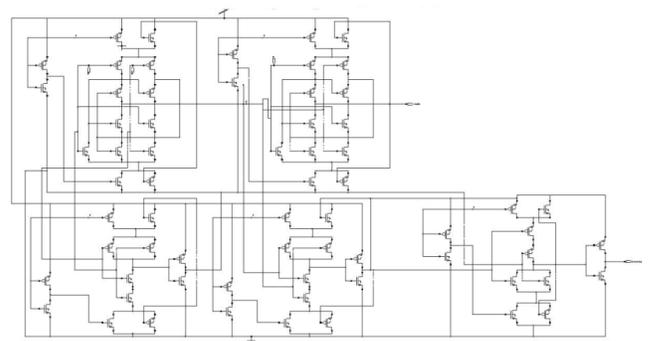


Figure 9. CMOS based full adder using sleepy keeper approach.

4. Implementation OF CMOS based Carry Look Ahead Adder

In general, conventional Carry-Look Ahead adder (CLA) decreases the percentage of time essential to define carry bits by improving speed. This adder estimates one or more number of carry bits previously the sum, it decreases the time that take to analyze the outcome bits are larger in number^{8,11}. The Carry look ahead adder has two signals known as Carry Propagator represented as ‘P’ and the Carry Generator represented as ‘G’. The carry generator block is used to generate the output carry whereas the carry propagator is used to propagate the carry to following level irrespective of input carry⁸. The functioning of conventional (basic) CLA can be tacit by handling the Boolean expressions dealing with the full adder. The term Propagate ‘P_i’ is given by $P_i = A_i \text{ XOR } B_i$ and the term generate ‘G_i’ is given by $G_i = A_i \text{ AND } B_i$. The novel equations for the output variables Sum, C_{out} are mentioned as:

$$\text{Sum} = S_i = P_i \wedge C_{i-1}; \quad C_{\text{out}} = C_{i+1} = G_i \parallel (P_i \& C_i)$$

4.1 Conventional CMOS based Carry Look Ahead Adder

To implement CMOS based carry look ahead adder consists of four bits there are four full adders and a carry look ahead blocks are required. Each full adder blocks using 36 transistors as shown in Figure 5. Carry look ahead block internally consists of four carry generator using 8 transistors. Suppose A, B, C_{in} are given as inputs to the first full adder then the propagate and generator blocks are obtained from first full adder and are fed as inputs to the first carry generator in carry look ahead adder. Along with propagator and generator C₀ is also fed as input to carry generator and C_i obtained by the first carry generator and fed as input to the second full adder this process will go on up to final sum and carry as shown in Figure 10.

4.2 CMOS based Carry Look Ahead Adder using Sleepy Approach

As discussed in sleepy approach shown in Figure 1, two sleep transistors are required. To generate sleep transistors S and S’ another inverter block is used. The CMOS based carry look ahead adder having 4-bits using sleepy approach is shown in the Figure 11.

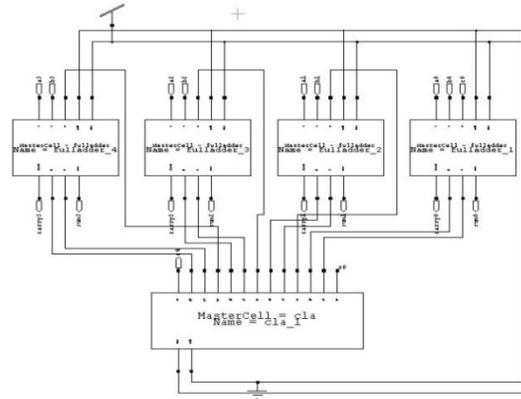


Figure 10. Conventional CMOS based carry look ahead adder.

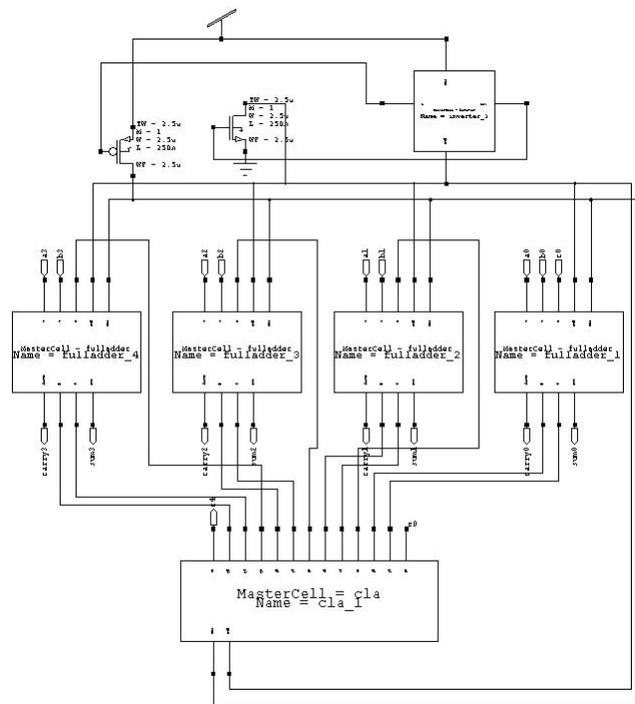


Figure 11. CMOS based carry look ahead adder using sleepy approach.

4.3 CMOS based Carry Look Ahead Adder using Stack Approach

To design CMOS based carry look ahead adder consisting of 4-bits using stack approach, each transistor width ‘W’ is divided into half as ‘W/2’. So each full adder block in the conventional carry look ahead adder having 4-bits is presented in the Figure 10. is

replace by the structure of CMOS based carry full adder using stack approach explained in Figure 7. In the carry look ahead block also each transistor width is divided into half.

4.4 CMOS based Carry Look Ahead Adder using Sleepy Stack Approach

To implement CMOS based CLA using sleepy stack approach, both the stack approach and sleepy approaches are combined and the block diagram of CLA using sleepy stack approach is looks like Figure 11. But internally each and every transistor width is stacked into half and sleep transistors are place above and below the pull up system and the pull down systems correspondingly.

4.5 CMOS based Carry Look Ahead Adder using Sleepy Keeper Approach

To implement CLA using sleepy keeper approach, NMOS as well as PMOS transistors are placed similar to both pull up and pull down transistors respectively as shown in Figure 11. To generate sleepy transistors S and S' additional inverter block is placed in the design.

5. Results and Discussion

The 1-bit Conventional CMOS based full adder is simulated with the help of various leakage power reduction approaches sleepy, stack, sleepy stack and sleepy keeper. This full adder is considered and implemented the 4-bit CMOS based carry look ahead adders with the sleepy, sleepy keeper, stack and finally sleepy stack. When exploring the results in the table of delay, Utilized power (average power consumed) and the Power Delay Product (PDP), the sleep keeper approach is producing comparatively better results. The simulations are performed using Tanner EDA tools at 250nm technology. The circuit's schematics are designed on S-Edit and the final spice netlist are generated using T-Spice. The circuits were simulated at a temperature of 25°C and typical models of NMOS and PMOS are considered. The both 1-bit full adder and 4-bit carry look ahead adders using leakage power reduction approaches of transient analysis is performed and the results are shown in Figure 12. Table I explain the simulated results in the form of average power, delay and PDP for 1-bit conventional full adder and the full adder using sleepy, sleepy stack, sleepy keeper and stack approaches. Table II explains the simulated

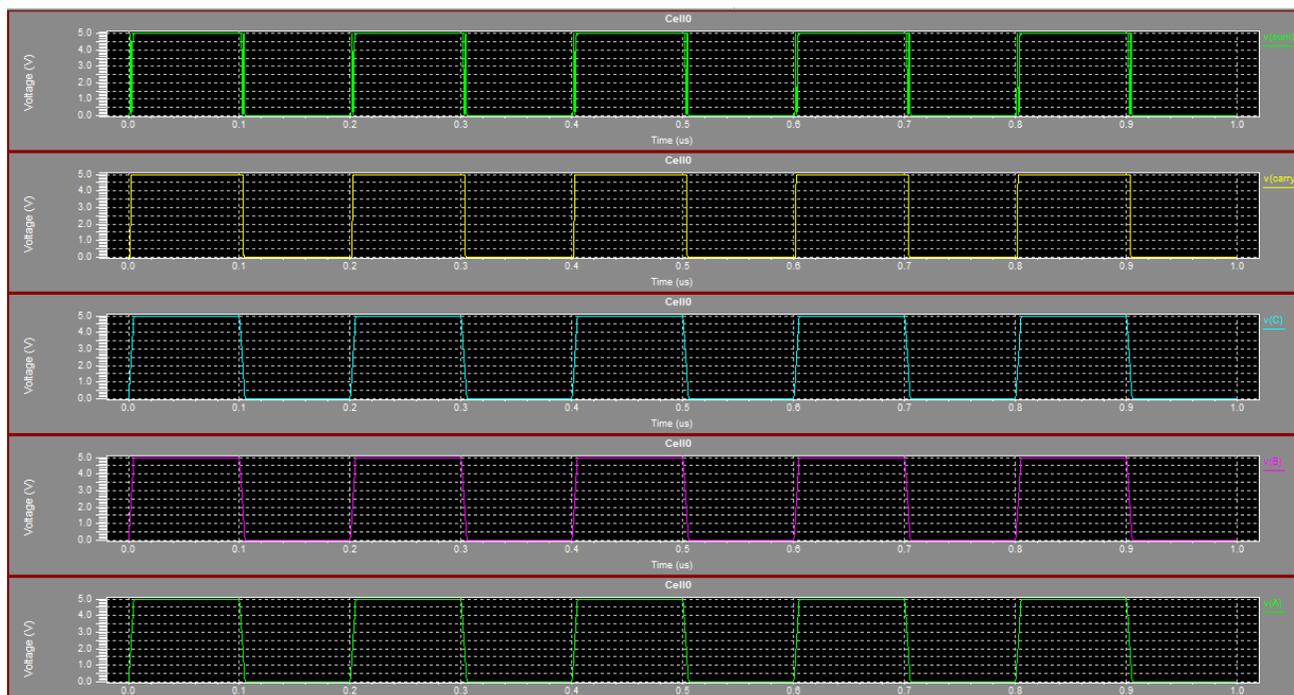


Figure 12. Transient Analysis of conventional carry look ahead adder.

Table 1. Average Power, Delay and number of transistors for 4-bit CMOS based Full adder

| Technique | Average Power(Watts) | Delay (s) | No. of transistors |
|-------------------------|----------------------|--------------|--------------------|
| Conventional full adder | 5.179507 e-012 | 2.3687 e-010 | 36 |
| sleepy | 5.193814 e-012 | 2.4252 e-010 | 40 |
| stack | 3.007335 e-012 | 4.2801 e-010 | 72 |
| Sleepy stack | 3.016228 e-012 | 5.4100 e-010 | 76 |
| Sleepy keeper | 2.757978 e-012 | 2.6397 e-010 | 66 |

Table 2. Average Power, Delay and number of transistors for 4-bit CMOS based carry look ahead adder

| Technique | Average power(Watts) | Delay (s) | No. of transistors |
|-------------------------------------|----------------------|--------------|--------------------|
| Conventional carry look ahead adder | 1.767278 e-011 | 3.9488 e-010 | 176 |
| sleepy | 1.766216 e-011 | 6.8462 e-010 | 180 |
| stack | 5.664637 e-012 | 8.4659 e-010 | 352 |
| Sleepy stack | 5.665998 e-012 | 8.4449 e-010 | 358 |
| Sleepy keeper | 1.066254 e-013 | 5.2528 e-010 | 320 |

results in the form of average power, delay and PDP for 4-bit conventional CMOS based carry look ahead adder as well as the CMOS based carry look ahead adder using sleepy, stack, sleepy stack and sleepy keeper approaches. From Table I and Table II, it is clear that the sleepy keeper approach yield more percentage of reduction in standby power compared to other approaches.

6. Conclusion

CMOS technology feature size and threshold voltage are being minimized to achieve high performance. So this gradually increases the leakage power dissipation. This paperwork delivers an applicable option for leakage

power reduction approaches for the particular application by sequential analytical approach. Here four bit carry look ahead adder with different leakage power reduction approaches is implemented. For ultra-low static power consumption the sleepy keeper approach is best option to choose and it will save the state also. Moreover, this sleepy keeper approach can be operated over multiple and single threshold voltages. While considering the benefit of dual V_{th} , the sleepy keeper is one of the utmost effective technique to minimize the leakage current along through the increased area and delay while consecutively maintaining particular logic state in sleep operation mode. While considering the area parameter, the sleepy keeper technique is probable to be the most eminent for complicated logic circuits, when compared to simple logic designs the percentage of enlarged area of the requisite transistors is less for compound logic circuits.

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