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# Hybrid Integration in 3D NoC with Efficient Path Establishment Mechanism in Circuit Switching

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## Abstract

On chip communication is now an upcoming technology; whereOn-chip interconnections are becoming tedious as they need to assure reliability, power, speed and scalability issues. Systems on chips, (SoCs), are so intricate that they oblige new interconnection techniques. Networks on Chip (NoCs) have paved way to resolve these problems. As application is becoming complex they require good design for greater bandwidth and performance which lead to 3D NoC. 3D NoC provide best solutions to connect as many functional elements on-chip over 2D NoC. Data flow NoCs can be categorized into: packet switched and circuit switched NoCs. The paper focus on simultaneous circuit and packet switching to benefit from two methods which ensures low latency and more resource utilization. Here in this paper, the circuit switched NoC is much concentrated where we implement our ideas in area like circuit setup method. Here we bring in a new method for guaranteed Quality of Service (QoS) known an efficient path establishment mechanism in circuit switching in 3D Torus topology. Torus topology aims to produce less latency of other topologies, where the path is estimated based on to the destination node layers and position. This paper is more advantageous where it can get switched between to different layers and position in which destination is placed. As of 3D NoC with increased number of nodes it ensureslow power, low latency, increase hardware integration, improved throughput and enables multi core processing and also resolves scalability crisis. It can operate on both packet and circuit switching which reduces both cost and operational expenses. Analysis on latency, power and throughput is made for 3D hybrid integration which provides better solutions. Optic Communication can be extended for future progress for improved speed and accuracy.

**Keywords:** Circuit Switching, 3D NoC, SoC, Packet Switching, Torus, Quality of Service

## 1. Introduction

By magnifying the size of die, transistors size has been compacted by the semiconductor expertise so that on a single chip more components and Intellectual Property (IP) cores can be incorporated. But the lessening of transistor size will lead to the enhancement of wiring delay and crosstalk. Moreover, to the increase in number of devices, the required communication bandwidth is more. Therefore, to conquer the restrictions on wire delay and B.W. novel communicating designs are necessary. This lead to the emerging of Network-on-Chip (NoC)[1]. NoC is anticipated to surpass the constraint on the communication bandwidth, wiring delay problem and believed to be a communication way out[2]. As the name implies NoC, put up a communication system on chip. Therefore, NoC can be considered as a prototype change in VLSI from dedicated wires to shared network[3].

According to Moore's theory the package bulkiness keep on increasing for each and every single chip. The 2D NoC thereby results in scalability issues due to continuous increase in processing cores. Distributing the clock, power leak and dissipation and reliability[4] are inflexible in 2D NoC. It led to an upcoming and promising technology. Future NoC is 3D integration to pile up manifold dies on distinct chip[5]. It works well for any complex SoCs with

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elevated performance, energy and design. Cutting-Edge expertise by incorporating NoC scheme in 3D manner is 3D NoC. On contrast to 2D NoC, 3D NoC considerablydiminish the diameter and distance of network thereby upgrading the performance and limiting the consumed power andmake use of vertical interconnect to increase scaling[6].

In packet switching, the router undergoes Buffer-Write (BW), Routing-Computation (RC), Virtual channel-Allocation (VA), Switch-Allocation (SA) and Switch-Traversal (ST) stage. This stages leads to high latency and power ratio. By comparing packet switching with that of circuit switching, it results in low latency and power as it includes only switch traversal stage as the path is established beforehand. If many data contend for a same link, circuits have to be established thereby resulting in time consuming setup phase[7]. This leads to overall decline in performance of NoC. To tackle the troubles of packet and circuit switching, a blended scheme that combines packet and circuit switching is proposed. By not only improves flexibility it will also provide optimization for latency. But none has taken this to 3D integration. The main idea of paper focus on providing equivalent or low power and latency and improved throughput in 3D NoC with respect to 2D NoC for hybrid scheme[8].

## 2. Router Architecture

### 2.1 The 2d Router Architecture

A standard NoC router design is shown in Figure 1. The router has X key in and X key out channels or ports. Thereby the crossbar is 5x5. The packets to be traversed are broken into flits. The Routing-Computation (RC); drive on the header flit of an arriving packet and by the packet target states the corresponding port or Physical-Channel (PC), or Virtual-Channel (VC). The Virtual channel-Allocation (VA) makes decision among all packets contend for admittance to a like output VC. The Switch- Allocation (SA) judges amid all VCs asking for a way in to the crossbar. The chosen flits are now allowed to pass through the crossbar and assigned to output[9].

### 2.2 The 3D Router Architecture

For 3D NoC, each router includes 2 ports to connect a top and bottom layer which includes buffer, arbitration and crossbar. This results in 7X7 crossbar as in Figure 2.

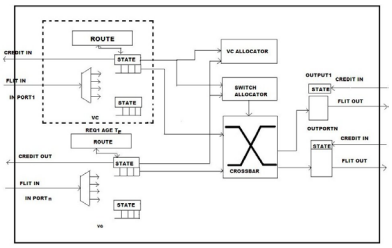


**Figure 1.** 2D router design.

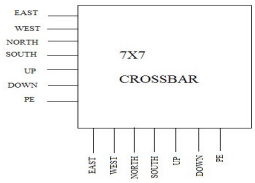


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**Figure 2.** 3D crossbar switch.

## 3. Topology

### 3.1 Mesh Topology

Most convenient design in 2D NoC is mesh as in Figure 3a. It consists of nxm switches which connect cores within. Resulting 3D design can be obtained from this formation. The extension of this arrangement is the 3D Mesh[10]. It makes use of seven switches: one to the PE, one for connecting top and bottom layers and each one for each direction (n,e,s,w) as demonstrated in Figure 3b.

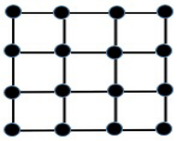

**Figure 3a.** 2D mesh.

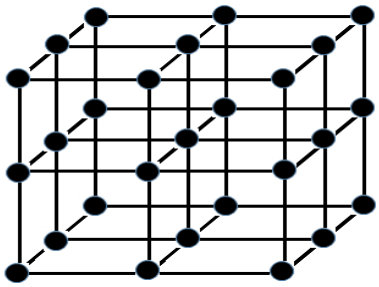

**Figure 3b.** 3D mesh.

On comparing to 2D NoC, mesh topology in 3D NoC has two drawbacks within it:

- It will not utilize the advantageous trait of a small interwafer distance.
- Addition of two ports to communicate up and down results in more power consumption than 2D.

### 3.2 Torus Topology

Two dimensional torus is illustrated in Figure 4a. Nodes in Torus topology are connected using short cable to adjacent nodes. Switches are not necessary as the signals are directly routed from one node to other node. Nodes communication takes place in six directions as illustrated in Figure 4b. Each node can be connected to other 6 nodes resulting in 3D shown in Figure 4c. Such arrangement permits addition of nodes without shrinking the performance. No additional cable or switch is required as node is combined as addition to grid. This addition of nodes in any complex system can be made with little trouble. The latency in links is comparatively low as the communication is made with short and direct interconnects.

Advantage of Torus over Mesh:

- Speed is high
- Low latency
- Consumes less energy and
- Avoids scalable problems

On basis of performance, latency and energy analysis the blended scheme of circuit and packet switching is implemented using torus topology in 3D[11].

## 4. Switching in Noc

Switching in NoC design is of two types: packet and circuit switching NoC.

In a packet switching, a data flow is broken and sealed into a block of a definite size, known as packets. A packet has a header and a pay_load. The header includes the collective information wanted by the routers to forward the packet to the target. The pay_load has the information a base node wants to send. For each packet resources like buffers and channels are assigned within routers. As soon as a packet reaches to a router, resources are owed. While the packet, moves out from the router the owed resources are reclaimed. The flow control in packet switching is between each two hops. This is known as hop_by_hop flow control[12].

Links in a packet switching NoC is never idle if there are packets to transfer. Packets of dissimilar data flows will move in turns to use a shared link. An arbiter selects the order. The packet is placed in buffered until its turn.

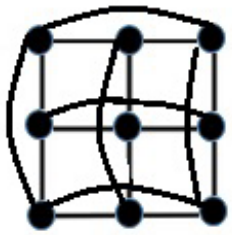

**Figure 4a.** 2D torus.

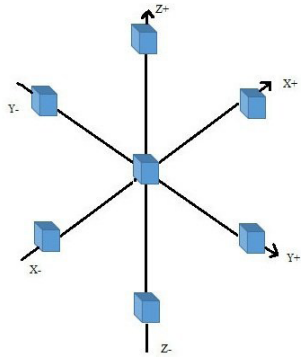


**Figure 4b.** Connection type.

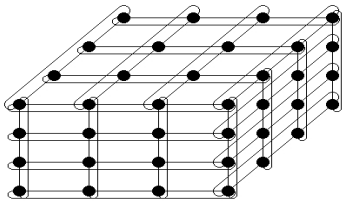

**Figure 4c.** 3D torus.

The main variation between circuit switching Noc and packet switching NoC is a circuit switching NoC will allocate a path before hand for a data flow before. In circuit switching NoC, no contention occurs and no need for header for forwarding packets as the resources are assigned and thus there is no requirement for arbitration during the data delivery. The flow includes path setup, data transfer and path release phase as shown in Figure 5.

In circuit switching NoC, links are shared between various data flows via TDM. Each connection can merely utilize a link only for a determined portion of time. The flow control in circuit switching is between source and target. This is known as end_to_end flow control[13].

Packet switching NoCs have been analyzed more carefully and intensively. However, Circuit switching NoC

has some attractive virtues and could be preferred under certain scenarios. On Comparing with packet switching NoC, even though circuit switching NoC has circuit setup over_head time, it can afford assured through-put and latency. Further, it can also provide lesser hardware complication and more energy efficiency, and operate at a elevated clock frequency. Here we bring in a flow based priority for adaptive circuit switching in 3D NoC for obtaining low latency and power.

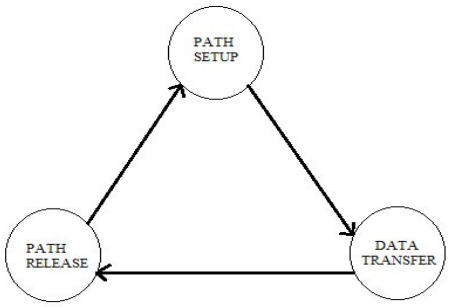


**Figure 5.** Circuit switching flow.

## 5. Proposed Technique

### 5.1 Efficient Path Setup Mechanism

In our proposed scheme, an efficient path establishment mechanism is implemented for low latency and power in 3D Noc. Path is estimated based on the destination node given by its layers and position. For any increase in number of nodes path laid are switched among different layers and fast enough for low latency. This method allows high hardware integration also enables parallel processing thereby increasing the overall performance.

We implement a Torus topology in 3D which includes 48 nodes. Bottom layer has 0-15 nodes, middle has17-31 nodes and topmost has 32-48 nodes. The source node and destination node is defined. The source and destination contains 8 bit data. The layer at which target resides is identified using layer select function which is defined by the node number. To set the priority to destination path, selection control signals is used. At a time only one condition is active to set the path for destination placement. Once the target is identified in particular layer the target position (n,e,w,s) is considered and activated with respect to selection signal. The layer write function is defined for the control bit which is high for the reserved path. The resources in the defined path remains held up until the next reset occurs for new source and destination. Circuit switching data is precedence over packet switching flits. For efficient Qos, effective path mechanism for path setup in circuit switching is implemented which provides guaranteed service and best effort as reserved path is used. Once the flits arrive the source router, if the source and the target router vary, the adjacent router becomes neighboring routers. Neighbor router are estimated and priorityis given to router based on where the destination router lies i.e. layer in which destination node resides and next w.r.t. the position (n,e,w,s) of destination router. Once the priority is given circuit switching takes place. Here as there is no need for acknowledgement for path setup the communication is fast enough resulting in reduced latency. At the same time when any flit request for same link, it is routed by packet switching. The proposed flow is shown in Figure 6.

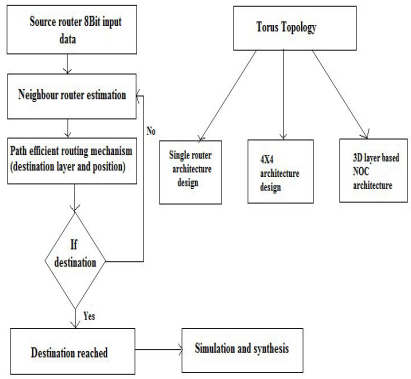


**Figure 6.** Proposed flow.

The sequence occurs to set up/release an adaptive CS connection

- The master PE receives a source data.
- Priority is assigned based on layer of destination.
- After layer is found the position in which the destination is placed is considered.
- The PE evaluates if it is realistic to set up the connection among the pair.
- If there is an accessible path among the pair, a message is sent to the set up path.
- Now it avails a link with the target. A connection is laid between a source and target pair and the resources in the pathway stay assigned until the next reset occurs.
- Control packet is passed in PS manner to the adjacent nodes, allocating resources in the path.

- In this approach, if a pathway is found, the link establishment is sanctioned and the successful setup is guaranteed.
- All data packets are traversed through the established pathway, without latency. The connection provides QoS, contributing a maximum throughput, since the communication is in a reserved manner.

# 6. Experimental Results

The proposed methods have been evaluated and syntheses report is generated using Xilinx software. Important parameters of Latency, Power and Throughput are given much importance and results are displayed.

The simulation result displayed in Figure 7 explains the adaptive circuit switching where destination resides in node 44 i.e. on layer 3, where it first communicates with node 32 adaptively and traverse the data to target.


**Figure 7.** Adaptive circuit switching.

## 6.1 Power

Power utilization is given based on the overall capacitances and signal behavior of the switch andeach division of the interconnect wire. A power simulator of 7 series XPE is used to analyze power, Figure 8 shows the power utilized. The dynamic power obtained is 21 mW.

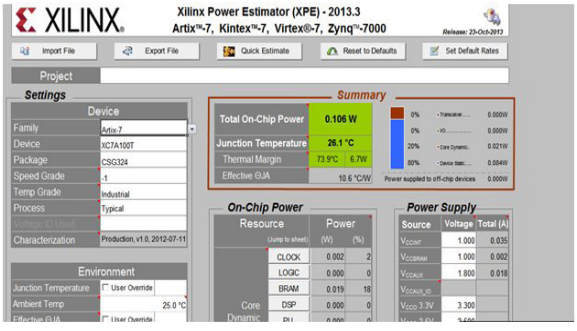


**Figure 8.** Power utilization.

## 6.2 Latency

Latency is defined as the time intrusion among the incidence of header flit in source node of network and the corresponding response of tail flit at the target node[14]. The timing window in Figure 9 shows the timing details of the proposed work.

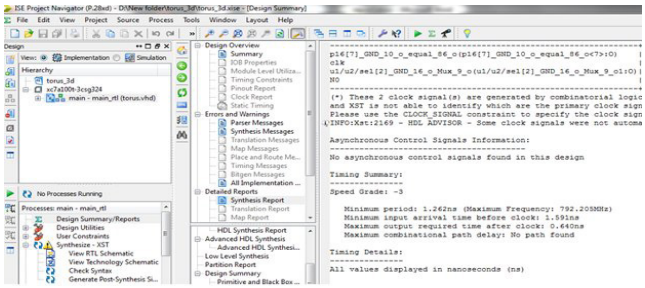

**Figure 9.** Timing report.

## 6.3 Throughput

Throughput can be defined as the data bits per clock cycle

$$\text{Throughput} = {}^{Data\ Bits}/_{Clock\ Cycle}$$

It can be seen from Figure 9 that Maximum frequency obtained is 792.2 MHz from which throughput can be calculated. The obtained throughput by $\{\{(8 * 792.2 * 10\hat{}6)/8\}/1024\}/1024$ is 755.500 MBps.

**Table 1.** Complete overview

| Power | 21 mW |
|---|---|
| Latency | 0.640 ns-1.591 ns |
| Throughput | 755.500 MBps |

The above mentioned Table 1 displays the complete overview of the analyzed parameters. The latency of 0.640-1.591 ns, power of 21 mW and throughput of 755.500 MBps is obtained which provides better solution for increased number of nodes in 3D NoC.

# 7. Conclusion

3D-NoC is a likely expansion of the 2D-NoC design formerly developed. The techniques that implemented can achieve a proficient solution. However, the adaptive scheme helps us to communicate with any layers. The adaptableness of this effort is utterly different from other

strategies, since it considers destination layer and position information to define the circuit switching mode. The results present an evaluation in power utilization, latency and throughput. We conclude this paper, thereby proving low power and latency for increased number of nodes for hybrid integration in 3D torus based NoC by introducing adaptive priority based circuit switching. Guaranteed QoS is obtained by focusing on destination based on layers and position.

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