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Differential Voltage Current Conveyor Based One-Shot Pulse Generator Circuit Implementation

Amit Bhattacharyya*

Department of Electronics and Communication Engineering Haldia Institute of Technology, Haldia – 721657, West Bengal, India; amit_elec06@yahoo.com

Abstract

Background/ Objectives: To design and analysis of One-shot pulse Generator Circuit, which is composed of only one Differential voltage current conveyor (DVCC) as the active element. **Methods/ Statistical Analysis:** Two application circuits utilizing the DVCC are introduced and implemented. The first one is a general one-shot pulse generating circuit. The second design can reduce the recovery time after applying triggered signals. Is-Spice is the simulation software to simulate every model. Commercially available ICs AD844AN and passive elements are required for circuit implementation. **Findings:** The effectivity of the projected circuits is examined as programme and experimental outputs satisfy theoretical results. Simulated and measured waveforms of Vtrg, Vo, and VC for two projected models with T = 1 ms are shown and it is clearly observed, that even the design parameters are same; the second proposed circuit is able to reduce the recovery time. The measurements show that recovery time T_r is 281 µs for the first proposed model, and T_r is 21.3 µs for the second proposed model. Applications/**Improvements:** The projected models provide new applications for the DVCC based systems. They have wide applications in the instrumentation, measurement, and communication systems and phase-locked loop circuits.

Keywords: Differential Voltage Current Conveyor, One-Shot Pulse Generator, Parasitic Effects, Positive-Edge Trigger, Recovery Time

1. Introduction

One-shot pulse generators are widely used in instrumentation, communication, phase-locked loop circuits, power conversion control circuits and signal processing applications[1]. Generally, One-shot pulse generator circuit consists of operational amplifier basically in voltage comparator mode, one capacitor and three resistors[2] as shown in Figure 1. Perhaps traditional structure requires several resistors and capacitors. Initially mostly operational amplifiers were used, later in place of voltage-mode; current-mode concept is used in analog system for larger width of the band, greater exactness, higher active range, and ease of fabrication[3-6] over traditional operational amplifiers. The idea of DVCC device is first came in[7]. Linear applications of DVCC in various fields such as active filters, impedance converters and sinusoidal oscillators, are well known. This paper presents a novel One-shot pulse Generator Circuit composed of only one DVCC as active element. The application circuits utilizing the DVCC are introduced and implemented. Each given circuit is implemented by only one DVCC with passive components. Each circuit is able to provide a pulse shaped response having changeable width via a positive-edge triggered signal. The first one is a general one-shot pulse generating circuit. The second design can shortens the recovery time for triggering signals. Due to wide popularity of DVCC-based application circuits in the present era, the presented One-shot pulse generator circuit is more applicable than the traditional designs to DVCC-based circuit systems. The proposed model has a

*Author for correspondence

number of advantages over the traditional design as given in Table 1.

Aspects of the projected models are as follows:

(1) Number of active devices used in the model are Less or same.
(2) Most of the passive components are grounded rather than floating structure to obtain the advantages of IC fabrication techniques and enhanced parasitic properties.
(3) Obtained operating frequency is higher than OPA based structure.
(4) The design can shortens the recovery time for triggering signals.
(5) Temperature sensitivity is less.
(6) Applicability in fully DVCC-based systems increases.

In Section 2, the basic concept and construction of DVCC is emphasized. Then working ideology of One-shot pulse Generator models is described and associated expressions are given. Also the non-ideality and parasitic properties on the planned model is analyzed in third Section .In fourth Section, a useful fabrication technique and parametric criteria is introduced. Later, laboratory examinations are performed on the fabricated models. The operation of the planned models is checked via simulation software and laboratory examination results. Programme and laboratory examined outputs match with hypothetical concepts. The last portion consists of conclusion.

2. Circuit Discussions and Working Ideology

2.1 Fundamental idea and construction of DVCC

The DVCC is useful for performing various superior presentations of continuous signal processed fields where voltage terminals require high input impedance and current terminals require high output impedance. Circuit symbol of DVCC having four terminals is given in Figure 2.

Table 1. Assessment of projected One-shot pulse Generator Circuit with other available models

Model Type	Used active and passive element numbers and types	Reducing ability of recovery time	Temperature sensitivity	Type of triggering	Least thickness of pulse
Operational amplifier based	1] Operational amplifier = 1 2] Resistor =3 (only one grounded) 3] Capacitor =1 (grounded) 4] Diode =1 (grounded)	No	Yes	Negative-edge triggered	Hundreds of μS
Operational transconductance amplifier based	1] Operational transconductance amplifier = 1 2] Resistor =2 (grounded) 3] Capacitor =1 (grounded) 4] Switch =1 (grounded)	No	No	Positive-edge triggered	Tens of μS
Operational transresistance amplifier based	1] Operational transresistance amplifier = 1 2] Resistor =3 (floating) 3] Capacitor =1 (floating) 4] Diode =3 (floating)	Yes	Yes	Positive or negative-edge triggered	Several μS
Standard 555 IC timer based	1] Operational amplifier = 2 2] Resistor =4 (only one grounded) 3] Capacitor =1 (grounded) 4] Switch =1 (grounded) 5] Flip-flop =1 (S-R type)	No	Yes	Negative-edge triggered	Tens of μS
Differential voltage current conveyor based (projected)	1] DVCC =1 2] Resistor =2 (only one floating) 3] Capacitor =1 (grounded) 4] Switch or diode=1 (grounded)	Yes	Yes	Positive-edge triggered	Several μS

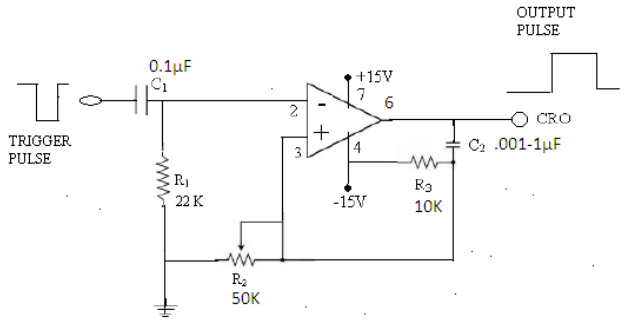


Figure 1. Traditional approach of One-shot pulse generator circuit.

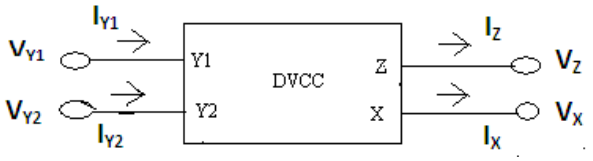


Figure 2. Circuit symbol of DVCC.

Voltage drop at X terminal (V_X) equals the difference of voltage between two Y terminals which areV_{Y1} and V_{Y2}, and current flowing through X terminal (I_X) is same as that of Z terminal (I_Z). DVCC has zero X terminal input impedance and infinite impedances at two Y terminals; hence I_{Y1} and I_{Y2} both are zero. Voltage drop at Z terminal is denoted as V_Z .From above characteristics, V-I relations of DVCC is articulated in equation (1).

$$\begin{pmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_Z \end{pmatrix} = \begin{pmatrix} 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_Z \end{pmatrix} \quad (1)$$

To check the effectivity of projected model, Figure 3 shows a realistic construction of DVCC using ICAD844AN which is easily accessible in the market.

The difference between AD844AN and OPAs is that it has a virtual short property between the inverting and non-inverting input terminals. Current flow through inverting terminal and current flow through T_Z terminal are same. Infinite resistances at two Y terminals are taken from non-inverting input terminals of the first two AD844ANs of DVCC structure; hence I_{Y1} and I_{Y2} both are zero. By connecting the Tz terminal of the first IC AD844AN to the non-inverting input terminal of the third through resistor R_b which is grounded , voltage drop at X terminal equals the difference of voltage between two Y terminals, and the current flowing through X terminal

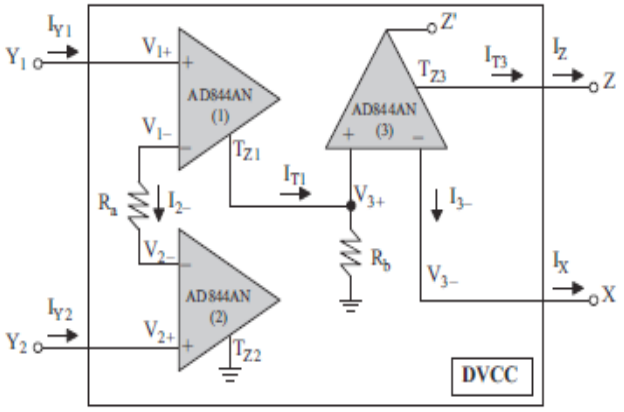


Figure 3. Implementation of DVCC using IC844AN.

is same as that of Z terminal, is obtained. From Figure 3 the following V-I characteristic equations can be written:

$$V_{Y1} = V_{1+} = V_{1-} \quad (2)$$

$$V_{Y2} = V_{2+} = V_{2-} \quad (3)$$

$$I_{Y1} = I_{Y2} = 0 \quad (4)$$

$$I_{TI} = I_{2-} = \frac{V_{1-} - V_{2-}}{R_a} = \frac{V_{Y1} - V_{Y2}}{R_a} \quad (5)$$

$$I_X = I_{3-} = I_{T3} = I_Z \quad (6)$$

$$V_X = V_{3-} = V_{3+} = I_{T1} R_b = \frac{R_b}{R_a}(V_{Y1} - V_{Y2}) \quad (7)$$

V_{3+} and V_{3-} are non-inverting and inverting voltage drop of third ICAD844AN, I_{T1} is current flowing through T_Z terminal of first ICAD844AN. Therefore, the V-I characteristic equations of ideal DVCC can be obtained by setting resistor R_a=R_b. Figure 3 shows a realistic construction of DVCC using IC844AN which is easily accessible in the market.

2.2 Proposed DVCC based Model Discussions

Figure 4 shows the models of the proposed DVCC-based One-shot pulse Generator. Figure 4(a) is a diode-clamping circuit. A modified model is shown in Figure 4(b) shorten the recovery time. Each proposed model is implemented by only one DVCC and several resistors and capacitors. An oscillator[8] provides rising-edged signal V_{trg} for triggering the circuits for producing pulse shaped waveform having fixed width. To form a regenerative-feedback[9] in two projected

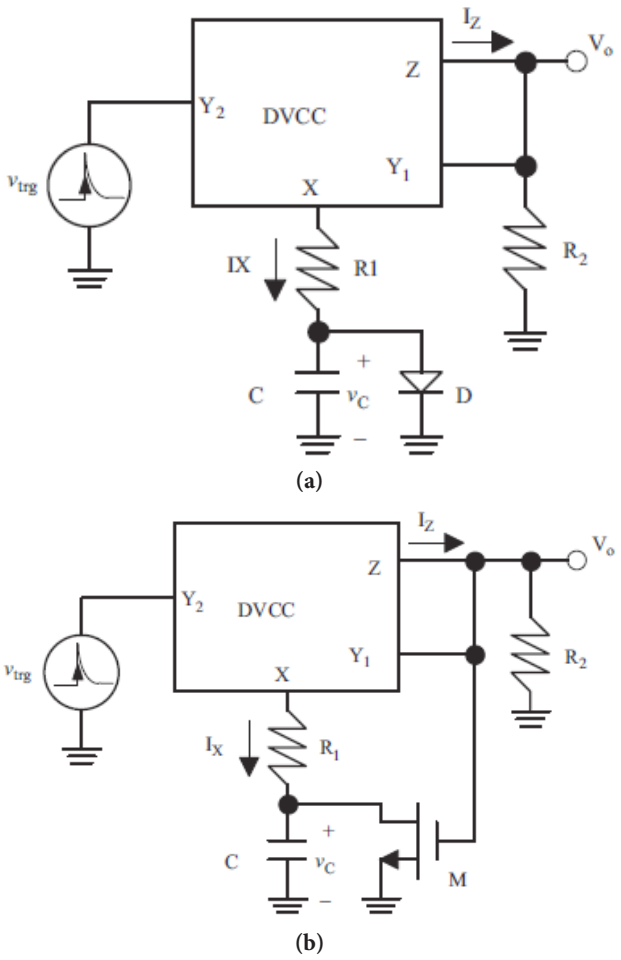


Figure 4. **(a)** First projected model and **(b)** Second projected model to reduce recovery.

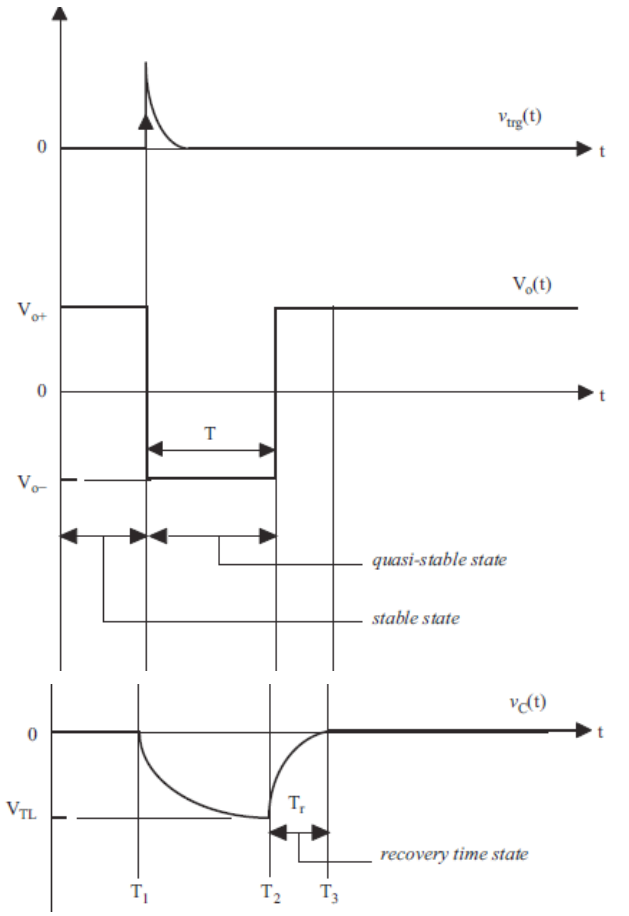


Figure 5. Generated waveforms of the proposed models.

models connects Y_1–Z together with the grounded resistor R_2. DVCC swings between two constant levels Vo_+ and Vo-. Figure 5 shows the related responses of the projected models in Figure 4. T represents the pulse width, and T_r is considered as the required time of recovery until later pulse is fired. The working ideology of every proposed model has three conditions: stable condition, quasi stable condition, and recovery time condition.

During stable condition, capacitor C is open-circuited and capacitor voltage VC drop is secured by the diode D, or the analog switch M. By adjusting R_2 greater than R_1 stable state operation is maintained, for which I_Z is less positive than I_X. Hence the output voltage V_O reaches upper constant level Vo_+. For the stable condition, the equations of I_x and I_z can be written as

$$I_X = \frac{V_O}{R_1} = \frac{V_{O+}}{R_1} \tag{8}$$

$$I_Z = \frac{V_O}{R_2} = \frac{V_{O+}}{R_2} \tag{9}$$

This state will continue up to t = T_1, where a trigger pulse is fired and then, the quasi stable condition will start. At present, Iz is greater than Ix and consequently the output voltage Vo jumps abruptly from Vo_+ to Vo-. Since Vo remains at Vo_-, C starts to discharge through R1 from t = T_1. In this state, the currents through X and Z terminals, i.e., Ix and Iz and the capacitor voltage $V_C(t)$ are expressed as

$$V_C(t) = V_{O-}(1 - e^{-\frac{(t-T_1)}{R_1 C}}) \tag{10}$$

$$I_X = \frac{V_O - V_C}{R_1} = \frac{V_{O-} - V_C}{R_1} \tag{11}$$

$$I_Z = \frac{V_O}{R_2} = \frac{V_{O-}}{R_2} \tag{12}$$

When t = T_2, capacitor voltage V_C reaches minimum voltage V_{TL}. By solving (11) and (12) the equation of minimum voltage V_{TL} is obtained for Ix=Iz:

$$V_{TL} = V_C(T_2) = (1 - \frac{R_1}{R_2})V_{O-} \quad (13)$$

Solving (10) & (13), size of the pulse, T, is obtained as given in equation (14). Equation (14) shows that the size of the pulse is changed for broad range of frequency by changing R_1 and C, and R_2 is used for accurate -tuning:

$$T = T_2 - T_1 = R_1 C \ln(1 - \frac{V_{TL}}{V_{O-}}) = R_1 C \ln(\frac{R_2}{R_1}) \quad (14)$$

Figure 6 shows the equivalent circuits of projected models at the ending of the quasi stable condition from where time of recovery T_r is obtained. In Figure 6, ideally infinite value R_{DR} considers as the turn off resistance of diode D, and ideally zero value R_{DS} as the turn on resistance of switch M.

3. Real and Parasitic Properties Explanations

Using IC AD844AN Second generation current conveyor in positive mode cascaded with buffering voltage having inbuilt parasitic impedances is obtained according to the datasheet. Several non-idealities, like parasitic impedances

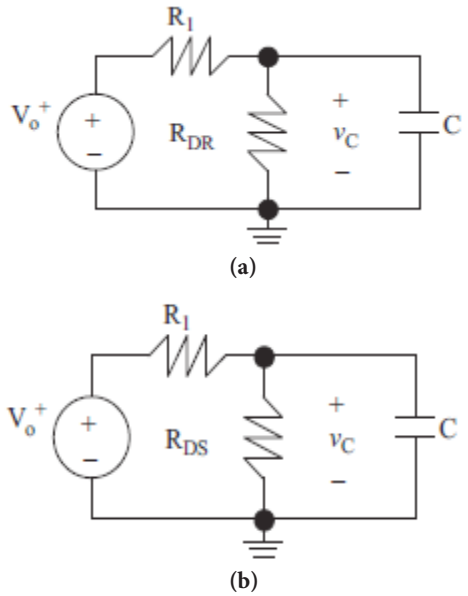


Figure 6. Equivalent circuits in the recovery time condition: **(a)** the first projected model and **(b)** the second projected model.

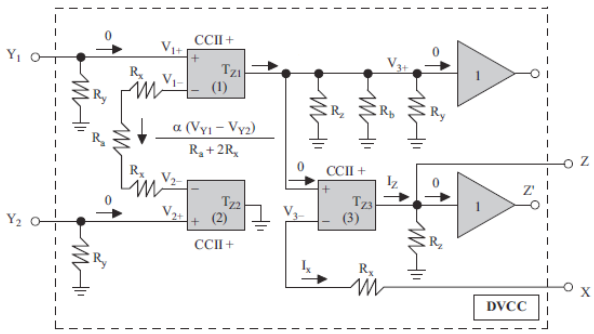


Figure 7. Real structure of used DVCC based circuit model.

and real gain concepts are emphasized here. A real structure of used DVCC based circuit model in Figure 7, is given where Rx, Ry, and Rz acting as terminal parasitic resistances. Parasitic resistance Rx is approximately several tens of ohms, but Ry and Rz are approximately several mega-ohms. α is considered as non-ideal voltage gain. According to the datasheet of AD844AN[10] the typical datas of α gain = 0.99, β gain = 0.98, Rx = 50Ω, Ry = 10 M Ω, and Rz = 3MΩ are considered.

4. Fabrication Criteria and Examined Outputs

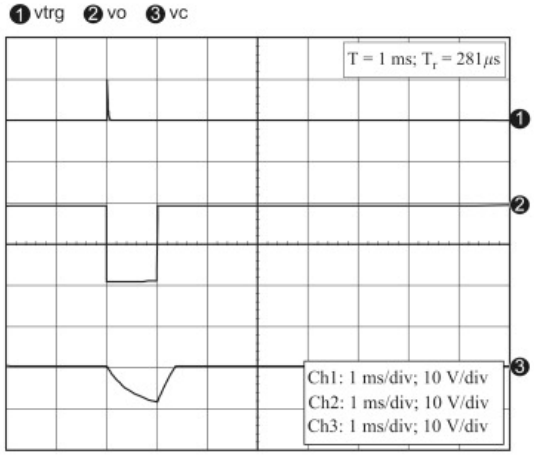
4.1 Fabrication Techniques and Parametric Criteria

Pulse width T is considered as the ratio R_2/R_1 and the capacitor C is arbitrarily determined. Minimization of the chance of parasitic and real gain effects on the proposed model, the criteria that Ra>>Rx, R_1>>Rx, R_b<< (Rz//Ry), R_2<< (Rz//Ry), and R_1>>R_{DS} must be maintained in the fabrication techniques. Parasitic resistance Rx is approximately several tens of ohms, but Ry and Rz are approximately several mega-ohm range.

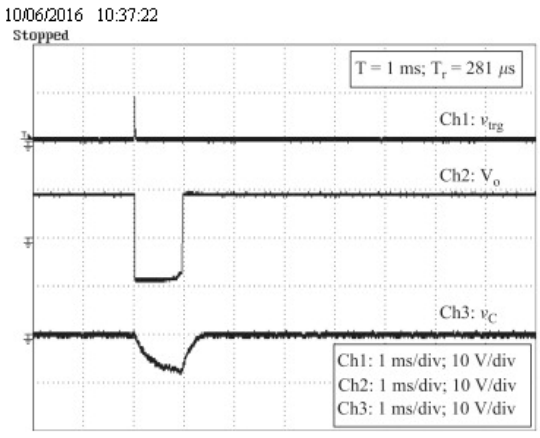
Thus the chosen values for resistors R_a, R_b, R_1, and R_2 range from few kilo-ohms to few hundreds of kilo-ohms. Fabrication criteria are such that R_1 must be smaller than R_2. From the integration point of view, the proposed One-shot pulse Generator models with grounded passive components is easier to fabricate in integrated circuits. Not only that, DVCC fabricated with easily accessible ICs is able to rise above the issue of loading effect even in the absence of voltage buffer. For implementation and checking purpose, easily accessible ICs AD844AN and passive elements are used to check viability of projected model.

4.2 Simulated and Examined Outputs

Laboratory examination is performed by using easily accessible AD844AN[11] ICs, analog switch CD4066, several resistors and capacitors to build projected model. Is-Spice is the simulation software to simulate real structure as given in Figure 7. The circuit simulations and experiments are maintained at supply voltages of ±10 V with saturation levels $Vo_+ = Vo_- = 9.4$ V. From an external function generator the triggering signal Vtrg is applied. According to the datasheet of AD844AN the typical datas of α gain = 0.99, β gain = 0.98, Rx = 50Ω, Ry = 10 M Ω, and Rz = 3MΩ are considered. For the proposed One-shot pulse Generator models, the width of the pulse is considered as T = 1ms, and impedance ratio of $R_2/R_1 = 10$ is adjusted. C is considered as 100 nF. Consider R_1 is much greater than Rx. Figure 8 and 9 shows the simulated and measured waveforms of

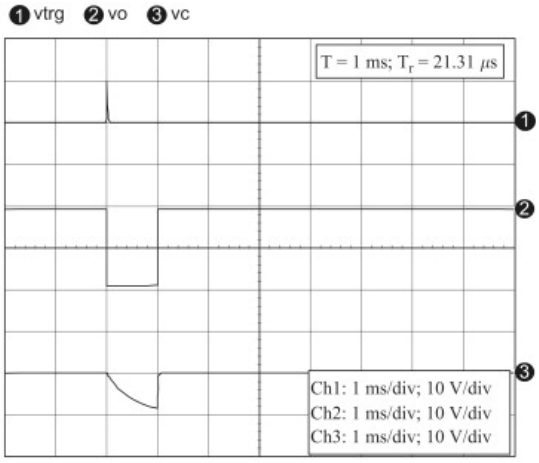


(a)

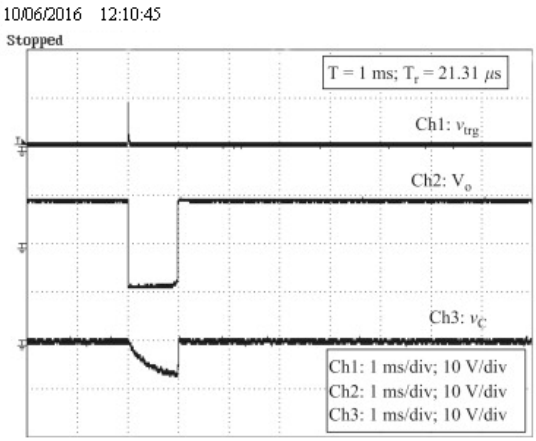


(b)

Figure 8. Simulated and Measured outputs of the corresponding waveforms with T = 1 ms for the first proposed model. **(a)** Simulated results. **(b)** Measured outputs



(a)



(b)

Figure 9. Simulated and Measured outputs of the corresponding waveforms with T = 1 ms for the second proposed model. **(a)** Simulated results **(b)** Measured outputs

Vtrg, Vo, and VC for two projected models with T = 1 ms and it is clearly observed, that even the design parameters are same, the second proposed circuit is able to reduce the recovery time. The measurements show that recovery time T_r is 281 μs for the first proposed model, and T_r is 21.3 μs for the second proposed model.

5. Conclusion

In this paper, the projected models consist of only one DVCC and several resistors and capacitors. An oscillator provides rising-edged signal Vtrg for triggering the circuits for producing pulse shaped waveform having fixed width. The second proposed model can shorten the recovery

time. The effectivity of the projected circuits are examined as programme and experimental outputs satisfy theoretical results. The projected models provide new applications for the DVCC based systems. They have wide applications in the field of measurement systems, signal processing field specially processing of electrocardiogram signal (ECG)[12-14], instrumentation, and communication systems.

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