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Reversible SSG Gate for Implementing Parity Checker Generator andMagnitude Comparator

S. S. Gayathri*, R. Dayana and P. Malarvezhi

Electronics and Communication Engineering department, SRM University, Chennai - 603203, Tamil Nadu, India; gayathrisu6@gmail.com,dayana.r@ktr.srmuniv.ac.in,malar83@gmail.com

Abstract

The objective is to design a new reversible logic gate for implementing parity checker and generator logic circuit and a magnitude comparator logic circuit with minimum computational time. Power dissipation seems to be a major drawback in all conventional irreversible logic circuits. As a solution to this, circuits can be constructed using reversible logic gates. According to the principle of reversible logic a new 3X3 gate named as SSG gate has been proposed. SSG gate has the ability to realize the following logic functions like XOR, NOR, OR, NOT, XNOR, AND and COPY. The proposed work can be implemented on a floating point subtractor and multiplier design. The proposed SSG gate is used to test the functionality of a even parity checker and generator circuit and it is compared with the circuit realized using existing Feynman gate. The comparative result shows that SSG parity checker and generator consumes 0.67 seconds less time compared with the existing gate. The comparative result of the 2-bit magnitude comparator designed using proposed SSG gate and with the existing reversible gate1 and Gate2 shows that the computation time for SSG gate comparator is reduced by 0.33 seconds with the existing reversible gate1 and gate2.

Keywords: Magnitude Comparator, Parity Checker, Parity Generator, Reversible Logic

1. Introduction

Reversible logic has attained more attention nowadays due to its low power consumption there by it offers high speed and higher densities. Reversible logic has wide application in the field of DNA computing, quantum computing, nanotechnology. According to R. Landauer research in 1960, loss of one bit leads to KTln2 Joules of energy dissipation, where K is Boltzmann constant and T is the absolute temperature[1]. As a solution to this, Bennett showed that KTln2 Joules of energy dissipation can be avoided if the computation is done in reversible way [2]. Thus to avoid the energy dissipation, circuits must be constructed using reversible logic. A reversible circuit should posses the following features[3],

Use minimum number of reversible gates
Use minimum number of garbage outputs
Use minimum number of constant inputs
The relation between input and output in a reversible logic is given by the formula[4]

Output = Input + Constant

Parity bit plays a vital role in the current digital communication world. Parity generator circuit generates the parity bit based on the data packets. Parity checker circuit is employed at the receiver side to check the accuracy of data received. Section 2 deals with the existing works done in this expertise Section 3 explains the commonly used reversible logic gates, Section 4 describes the functionality of the proposed gate, Section 5 explains the design of the reversible parity generator, checker and magnitude comparator circuit using the proposed reversible gate. Section 6 deals with the simulation results of the proposed work and its performance analysis. Section 7 gives the conclusion of the proposed work.

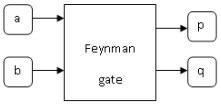
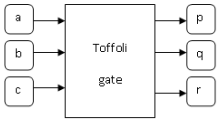
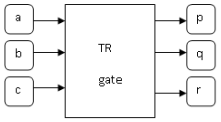
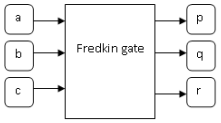
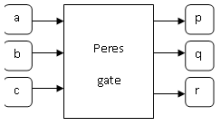
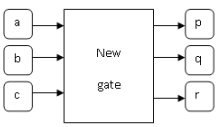
2. Previous Works

A new reversible gate NTG is proposed and it is tested

* *Author for correspondence*

on a booth multiplier architecture[5]. A new 4*4 universal parity preserving reversible logic gate has been proposed in which the parity of the input matches with the parity of the output. The proposed gate is used to implement any arbitrary Booleanfunction[6]. Three novel reversible gates has been proposed and it is tested to implement a novel half adder and full adder logic[7]. A fault tolerant reversible ALU using parity preserving reversible logic gates was designed and the designed ALU is capable of generating seven arithmetic and four logical operations[8]. A new parity preserving logic gate was proposed and it also presents two optimized design of a self-checking two rail checker circuit based on the proposed parity preserving logic gate [9]. An even and odd parity generator and checker circuit using Feynman gate[10]. An efficient low power multiplier was designed by constructing a Vedic multiplier using reversible logic gate and the results showed reduced garbage outputs, constant inputs and TRLIC factor[11]. A reversible 16 bit adder using Kogge stone adder was designed using Peres logic was found to be efficient than the conventional adder[12].

3. Reversible Logic

S. no	Name	Block diagram	Function
1	Feynman gate		p=a q=a ⊕ b
2	Toffoli gate		p=a q=b r=ab ⊕ c
3	TR gate		p=a q= a ⊕ b r= ab' ⊕ c
4	Fredkin gate		p=a q=a'b ⊕ ac' R= ab ⊕ a'c
5	Peres gate		p=a q= a ⊕ b r= ab ⊕ c
6	New gate		p=a q=ab ⊕ c r=a'c' ⊕ b'

Reversible logic gates are circuits in which number of inputs is equal to number of outputs and the outputs are unique i. e, there is a one to one correspondence between input and output. Some of the basic logic gates with its logical expression are shown below,

4. Proposed Work

In this work, a new 3*3 reversible SSG gate is proposed to realize even and odd parity generator and checker circuit. The proposed gate realizes some of the basic Boolean functions like XOR, NOR, OR, NOT, XNOR, AND and COPY functions. The logical block diagram of SSG gate is shown in the figure1.

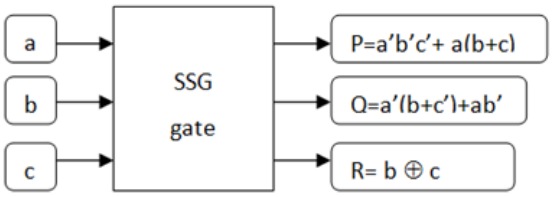


Figure 1. Logical Block Diagram of SSG gate.

Table 1. Truth Table of the Proposed SSG gate

INPUTS			OUTPUTS		
A	B	C	P	Q	R
0	0	0	1	1	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

From the truth table, it is inferred that there is a one-to-one correspondence between the input and output.

4.1 SSG Gate Output Expressions when A=0

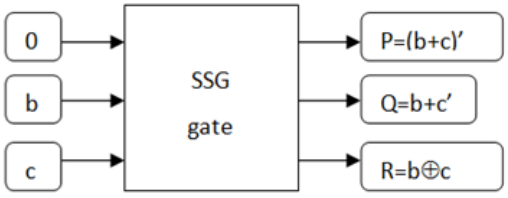


Figure 2. SSG gate when A is forced to '0'.

As seen from figure 2, when the input A is forced to logic '0', the proposed SSG gate can be used to realize one of the universal NOR functions at output P.

4.2 SSG Gate Output Expressions when A=1

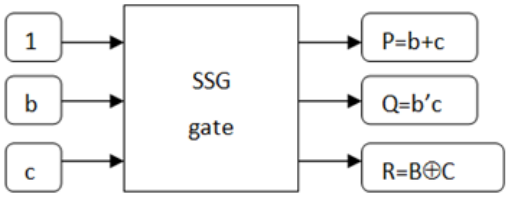


Figure 3. SSG gate when A is forced to '1'.

As seen from figure 3, when the input A is forced to logic '1', the proposed SSG gate can be used to realize OR function at output P.

4.3 SSG Gate Output Expressions when B=0

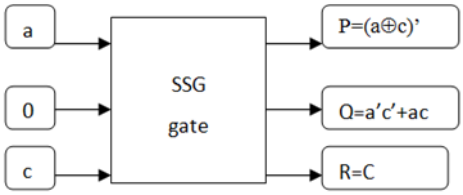


Figure 4. SSG gate when B is forced to '0'.

As seen from figure 4, when the input B is forced to logic '0', the SSG gate can be used to realize XNOR function at output P, Q and COPY function at R.

4.4 SSG Gate Output Expressions when B=1

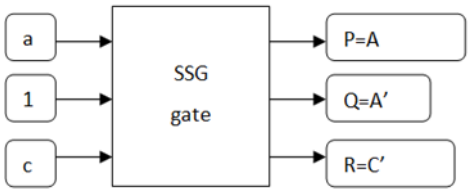


Figure 5. SSG gate when B is forced to '1'.

As seen from figure 5, when the input B is forced to logic '1', the SSG gate can be used to realize NOT function at output Q and R, COPY function at P.

4.5 SSG Gate Output Expressions when C=0

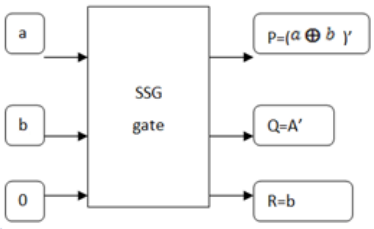


Figure 6. SSG gate when C is forced to '0'.

As seen from figure 6, when the input C is forced to logic '0', the proposed SSG gate can be used to realize XNOR function at output P, NOT function at Q and COPY function at R.

4.6 SSG Gate Output Expressions when C=1

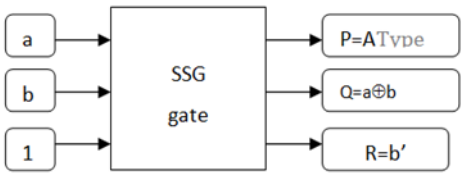


Figure 7. SSG gate when C is forced to '1'.

As seen from figure 7, when the input C is forced to logic '1', the proposed SSG gate can be used to realize a COPY function at P, Ex-Or function at Q and NOT function at R

All the above stated figures explains that SSG gate can be used to realize the basic Boolean functions like XOR, NOR, OR, NOT, XNOR, AND and COPY by controlling one of the inputs as a constant input.

5. Parity Generator and Checker Design using SSG Gate

This is a digital communication era where the information to be transmitted and received is in the form of binary bits. Parity bits are used to ensure the error free transmission and reception.

The output expression for odd parity generator is

Po=$(A \oplus B \oplus C)$

The output expression for even parity generator is

Po=$(A \oplus B \oplus C)$

Parity checker is employed at the receiver side. While checking the received bits if any discrepancies found with

the parity bits it implies that the information has some erroneous bits.

The output expression for even parity checker is,

Pe-out= $(A \oplus B \oplus C \oplus Pin)$

The output expression for odd parity checker is,

Po-out= $(A \oplus B \oplus C \oplus Pin)'$

5.1 Design of 3-bit even parity generator & checker using SSG gate

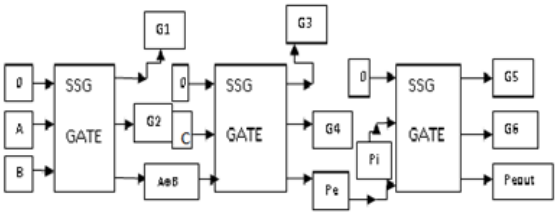


Figure 8. Logical block diagram of even parity checker and generator using SSG gate.

Figure 8 shows the design of 3-bit even parity generator and checker using the proposed SSG gate. The input bits are A, B, C & Pin. The parity generator output is given by the variable Pe and the even parity checker output is given by the variable Pe-out. The variables G1, G2, G3, G4, G5, and G6 are the garbage outputs.

5.2 Design of 3-bit odd parity generator and checker using SSG gate

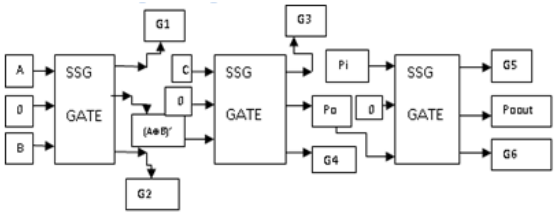


Figure 9. Logical block diagram of odd parity checker and generator using SSG gate.

Figure 9 shows the design of 3-bit odd parity generator and checker using the proposed SSG gate. The input bits are A, B, C & Pin. The parity generator output is given by the variable Po and the odd parity checker output is given by the variable Po-out. The variables G1, G2, G3, G4, G5, and G6 are the garbage outputs.

5.3 Design of one bit Magnitude Comparator using SSG gate

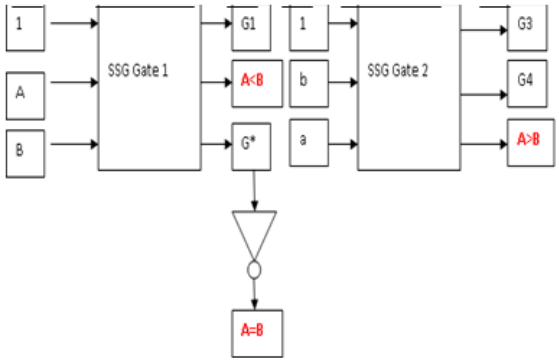


Figure 10. Logical block diagram of Magnitude comparator using SSG gate.

Figure 10 shows the logical block diagram of magnitude comparator which can compare the input of one bit length and produces three outputs A<B,A>B,A=B along with three garbage outputs G1,G2,G3.

6. Simulation Results

The proposed design is simulated using Modelsim and synthesized using Xilinx Virtex5.

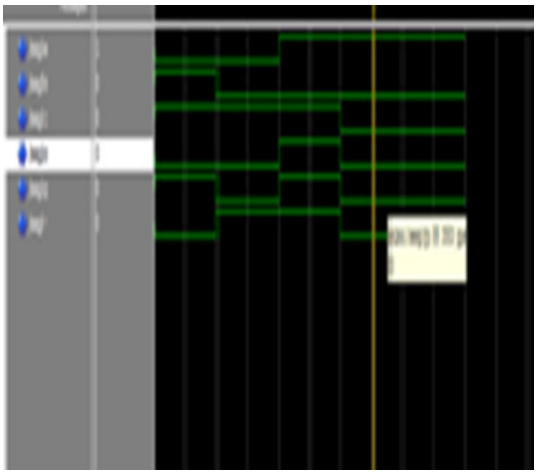


Figure 11. Simulation Result of SSG gate.

Figure 11 shows the simulation result of SSG gate. The variables a=1, b=1, c=0 indicates input and the variables p=0, q=0, r=0 indicates output.

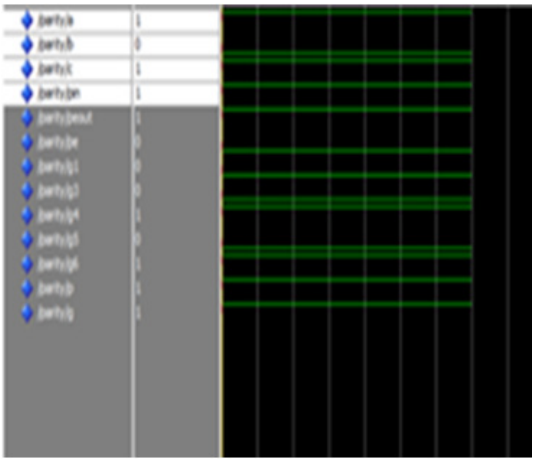


Figure 12. Simulation Result of even parity checker and generator using SSG gate.

Figure 12 shows the simulation Result of even parity checker and generator using SSG gate. a, b, c and pin are the input variables.pe is the parity generator output and peout is the parity checker output.

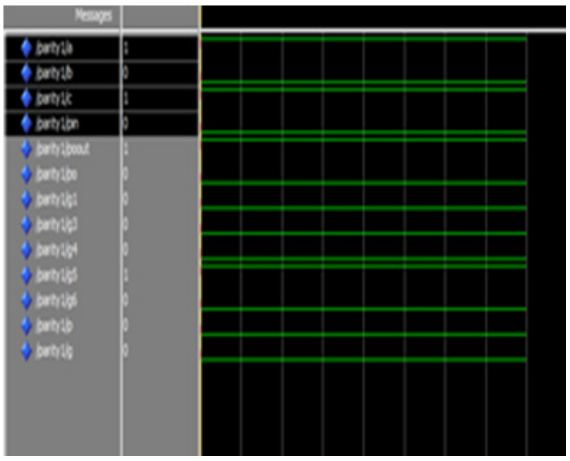


Figure 13. Simulation Result of odd parity checker and generator using SSG gate.

Figure 13 shows the simulation Result of odd parity checker and generator using SSG gate. a=1, b=0, c=1 and pin=0 are the input variables. Po=0 is the parity generator output and pout=1 is the parity checker output. Table 6 and 7shows the performance analysis of even parity generator and checker and odd parity generator and checker respectively.

Table 2. Comparison of Proposed reversible parity checker &generator with existing reversible parity checker &generator

Content	Garbage Outputs	Constant inputs	Computation time
SSG gate	6	3	4.96 Seconds
Comparator			
Feynman gate	3	-	5.63 Seconds
Comparator			

Table 2 shows Comparison of Proposed reversible parity checker & generator with existing reversible parity checker & generator. The analysis is done in terms of Garbage outputs, Constant inputs, Computation time. AV Anantha Lakshmi proposed two new3x3 reversible gates to realize a reversible 1-bit comparator[13].

The proposed reversible 1-bit comparator is compared with the above design and work is analyzed in terms of number of reversible gates, garbage outputs, constant inputs and quantum costs. Table 8 shows the comparison between the existing reversible magnitude comparator and proposed reversible magnitude comparator.

Table 3 shows the comparison of the proposed reversible magnitude comparator with the existing design made using reversible gate1 & reversible gate 2**.** As seen from the above table it's proved that proposed design utilizes fewer devices and also the computational time is less when compared with the proposed design.

Table 3. Comparison of Proposed reversible Magnitude comparator with existing reversible magnitude comparator

System	Device Utilization Summary	Garbage Outputs	Constant Inputs	Computation Time
Existing System	Number of Slices: 2 out of 256 0% Number of 4 input LUTs: 3 out of 512 0% Number of bonded IOBs: 6 out of 88 6%	2	2	3.51S
Proposed System	Number of Slices: 1 out of 256 0% Number of 4 input LUTs: 2 out of 512 0% Number of bonded IOBs: 5 out of 88 5%	3	2	3.18S

7. Conclusion

In this work, a new 3x3 reversible logic gate is proposed which can implement many logic functions. This paper also gives an idea of implementing the proposed reversible gate in applications like Parity checker, Parity generator and Magnitude comparator. It is shown that the proposed logic gate is an optimized gate for realizing several logic circuits.

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