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TG based 2T2M RRAM using Memristor as Memory Element

Chandramauleswar Roy* and Aminul Islam

Department of Electronics and Communication Engineering, Birla Institute of Technology (Deemed University), Mesra, Ranchi - 835215, Jharkhand, India; chandram@bitmesra.ac.in, aminulislam@bitmesra.ac.in

Abstract

Objective: This article presents a transmission gate based novel 2T2M RRAM using memristor as memory element. **Method/Analysis:** Simulation results of critical design metrics of proposed 2T2M RRAM cell and conventional SRAM cell are compared. **Findings:** The proposed 2T2M RRAM cell achieves 1.35 × lower read delays at the expense of 1.02 ×higher write delay than conventional 6T SRAM cell at nominal V_{dd}. Moreover, being non-volatile it is more power efficient and also saves at least 50% of area. **Novelty/Improvement:** It is more power efficient and saves 50% of area. Further, being differential in nature, proposed cell is more immune to PVT variation during read operation.

Keywords: Memristor, Nonvolatile, RRAM, Read Delay, Transmission Gate, Write Delay

1. Introduction

In the past decade, CMOS based SRAM memory was most dominant. It kept pace with Moore's law through continuous scaling. But today, when CMOS devices are being scaled beyond 22-nm technology node it becomes prone to PVT variations and many other quantum effects[1,2]. Moreover, with coming of devices like cellphone, wireless network element and other gadgets there is need of device with high integration and ultra-low power consumption (to increase the battery life), which traditional memory such as SRAM and Flash memory failed to accomplish[3].

Thus, there is need of emerging memory device with different characteristics such as a) higher reliability b) smaller dimension c) low power consumption d) shorter access time. In recent years, several memory technologies have emerged namely magneto-resistive RAM (MRAM), conductive-bridging memory (CBRAM), phase change memory (PCRAM), resistive memory RRAM)[4]. Among them, because of smaller dimension and shorter access time (comparable to SRAM), memristor is the most promising candidate among the emerging memory technologies.

Memristor is a two terminal device whose resistance can be changed by applying potential difference across the terminal. The term 'memristor' was first coined in as the fourth fundamental element after resistor (R), capacitor (C) and inductor (L)[5]. He predicted the existence of memristor on symmetry reasons. According to Chua, there can be six possible combination of relations from four fundamental circuit variable namely voltage (V), current (I), flux (Φ) and charge (Q). Flux and charge are integration of voltage and current with respect to time respectively. Other three relations are V=IR; Q=CV; and Φ=LI. Thus, missing sixth possible combination could be relation between charge (Q) and flux (Φ) i.e.

$$M = \partial \phi / \partial q$$

where, M represents memristor.

Although memristor had been discovered almost four decades ago, due to lack of fabrication it was mere a concept till 2008. In along with other researchers fabricated the first memristive device using TiO_2 at HP Lab[6]. Have proposed an imply logic through which memristor can also be used as logic element[7,8]. Because of its ultra-small size, memristor will be the key element for neuromorphic structure[9]. It is expected to achieve beyond Von-Neumann computation with the aid of memristive logics[10]. Because of its promising future, memristor has

* *Author for correspondence*

drawn significant attention of researchers all over the world[11,12].

In this paper, we have proposed a transmission gate based novel 2T2M RRAM using memristor as memory element. This structure uses differential scheme for read operation. Moreover, our proposed cell reduces the size of memory cell compared to 6T SRAM cell, as it uses only two memristors. Also the power consumption of our proposed cell is very less due to non-volatile characteristic of memristors. To verify the proposed design extensive simulation using 45-nm PTM (developed by Nan scale Integration and Modeling (NIMO) Group, Arizona State University (ASU)) and linear drift memristor model (HP Lab) has been carried out[13].

The rest of the paper is organized as follows: Section 2 provides brief overview of memristor. In section 3, proposed 2T2M RRAM is discussed. Simulation methodology and results have been explained in section 4 and finally the paper is concluded in section 5.

2. Memristor

Memristor is two-terminal device whose resistance changes when electric field is applied but remains unchanged when field is removed. In have proposed a physical model which consists of thin semiconductor film of TiO_2 sandwiched between two metal contacts Figure 1.

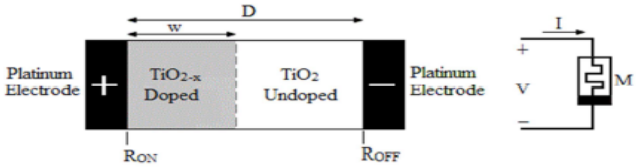

Figure 1. Memristor structure and its circuit symbol in which thick black line represents doped layer.

T_iO_2 layer has two parts: undoped and doped (with oxygen vacancies). The undoped part is highly resistive and the doped part is highly conductive. Oxygen vacant doped layer act as positive charged ion. When external electric field is applied across the terminal, positively charged oxygen vacancies in doped region get repelled. This results in change in width of doped and un-doped regions thereby changing overall resistance of the device. State variable 'W' is the width of doped region (T_iO_{2-x}). When doped region extends to the width of device (*i.e.* W=D), then resistance of device is R_{ON} (low resistance). Similarly, when undoped region extends to width of device (i.e., W=0), then resistance of device is R_{OFF} (high resistance). However, these oxygen vacancies do not move when electric field is removed which leads to non-volatile property of memristor.

A two-terminal linear memristor can be modeled by considering two resistances in series as shown in following equation:

$$R(W) = R_{ON} \times \frac{W}{D} + R_{OFF}\left(1 - \frac{W}{D}\right) \quad (1)$$

$$M(Q) = R_{OFF}\left(1 - \frac{\mu_V R_{ON}}{D^2} Q(t)\right) \quad (2)$$

where, $M(Q)$ is memristance of memristor,μ_V is the mobility of oxygen ions and 'D' is the device width. I-V relationship of memristor can be modeled as:

$$V(t) = \left(R_{ON} \times \frac{W(t)}{D} + R_{OFF}\left(1 - \frac{W(t)}{D}\right)\right) I(t) \quad (3)$$

where, $W(t)$ is given as

$$W(t) = \frac{\mu_V R_{ON}}{D} Q(t). \quad (4)$$

I-V characteristic of memristor is a hysteresis loop Figure 2 which is the fundamental characteristics of memristor. Since hysteresis curve cannot be obtained by any combination of R, L and C without using any active element, memristor is fourth fundamental element after resistor, capacitor and inductor.

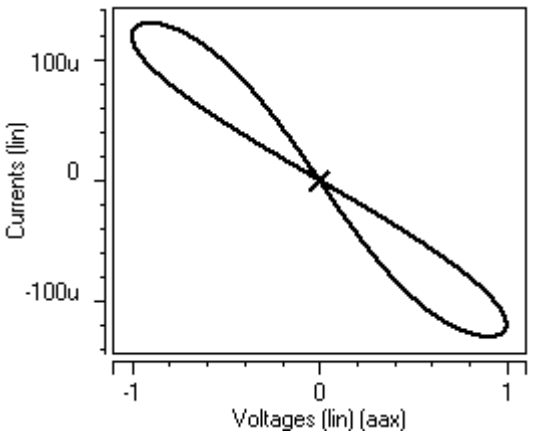

Figure 2. I-V characteristic of memristor in response to sinusoidal wave input voltage.

3. Proposed 2T2M RRAM

In this section, structure and operations of proposed 2T2M RRAM has been discussed. As shown in Figure 3 proposed cell consists of two memristor connected back to back. It has a transmission gate as access device to boost the write-1 operation as NMOS provides weak logic '1' (i.e., V_{DD}-V_t). Although other researchers have proposed single memristor based RRAM but single ended sensing is not reliable and more sensitive to process variation. It also needed additional reference voltage and there was lot of overhead associated with routing of reference voltage. Differential structure of proposed cell provides immunity to PVT variations. The differential structure also makes RAM cell more reliable during read operation through simple sense-amplifier with higher noise margin.

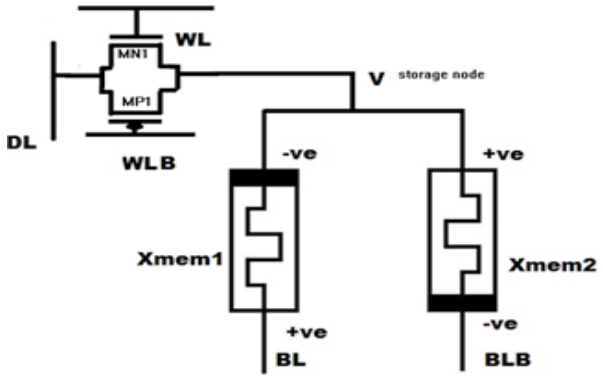

Figure 3. Proposed 2T2MRRAMdifferential structure.

3.1 Write Operation

Write operation is initiated by turning word line (WL) and word line bar (WLB) on and off respectively. To write, data is applied on data line (DL) and inverse of the data is applied to both bitline (BL) and bitline bar (BLB). As both memristor is connected to storage node (V) and BL/BLB in a complementary fashion, depending upon data one of them goes in to high resistance state (say logic '0') and other in to low resistance state (say logic '1').

For Illustration, let us assume that we have to write logic '1'. For this, the value to be written, i.e., '1' is loaded on DL and '0' is applied on BL and BLB. As a result of applied potential difference across memristor, doped layer in Xmem1 expands changing it to its low resistance state (logic '1'). Similarly, in Xmem2 doped layer shrinks resulting in high resistance state (logic '0'). Write delay is shown in Table 1, Levels of control signals during write operation are shown in Figure 4. Write-1 takes longer time than write-0 because current driving capability of PMOS is less than that of NMOS.

Table 1. Write Delay or Write Access Time (TwA)

V_{DD} (V)	Write -1(ns)	Write-0(ns)
0.9	0.86	0.79
0.95	0.83	0.73
1	0.78	0.68
1.05	0.72	0.64
1.1	0.63	0.53

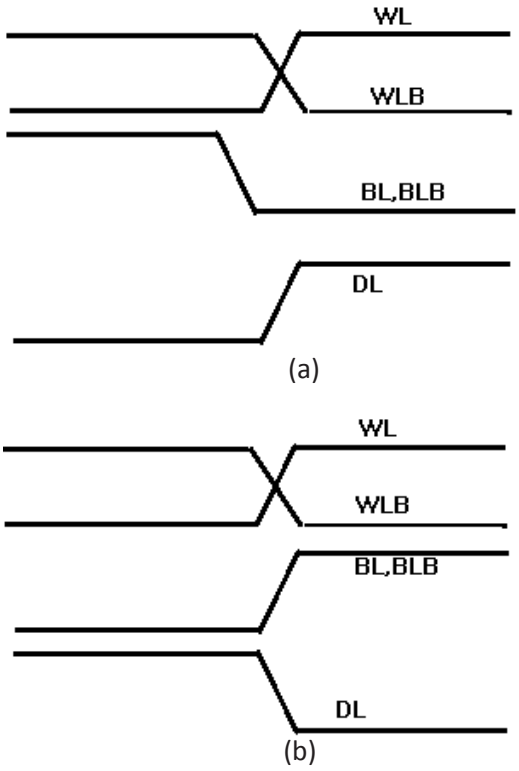

Figure 4 Control signal during write operation (a) write-1 (b) write-0.

3.2 Read Operation

Prior to read operation of device, BL and BLB are discharged. Read operation is initiated by raising WL high and lowering WLB to GND for a very brief period so that stored data is not destroyed. Once the transistors of transmission gate are ON, BL and BLB start charging with rate depending upon their resistance state.

For illustration, say Xmem1 is in low resistance state (logic '1') and Xmem2 is in high resistance state (logic '0') prior to read operation. In this case, BL will charge at

faster rate than BLB Figure 5. Sense amplifier will sense the data when difference between voltage level of BL and BLB become more than 50 mV and decipher the content of the memory cell. Table 2 shows the read delay. Because of symmetry read-0 and read-1 is same.

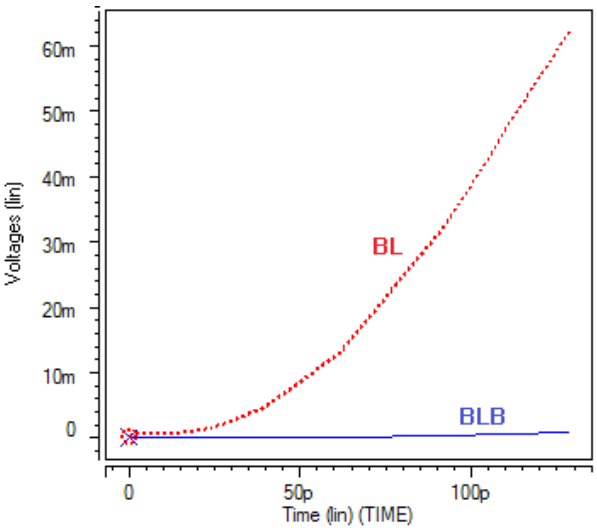

Figure 5. Read operation.

Table 2. Read Delay or Read Access time (TRA)

V_{DD} (V)	Read-1(ns)	Read -0(ns)
0.9	0.124	0.124
0.95	0.117	0.117
1	0.111	0.111
1.05	0.105	0.105
1.1	0.101	0.101

4. Simulation Results and Discussion

To simulate our proposed device, linear drift model of memristor proposed by HP Lab has been used. All the MOSFET has been simulated using 45-nm technology node. Important parameters used are listed in Table 3.

Proposed RRAM cell is also compared to conventional 6T SRAM cell in terms of read and write delay. Table 4 shows the comparison between 6T SRAM cell and proposed 2T2M RRAM cell. Write delay of memristor is calculated as average of delay during write-1 and write-0. Proposed 2T2M shows 1.35 times improvement in read delay. However, due to weak mobility of memristor, there is penalty of 1.02 times in write delay.

Table 3. Parameters of memristor used for simulation

Name	Description	Value
R_{ON}(ohm)	Memristor's minimum resistance	100 Ω
R_{OFF}(ohm)	Memristor's maximum resistance	200kΩ
D(m)	Physical width of memristor	3nm
UV(m^2/Vsec)	Linear ion mobility	10e-14
Initial state (W/D)	Initial state of state variable	0.5

Table 4. Comparison of 6T SRAM Cell with proposed 2T2M @ VDD = 1V

Operation	6T SRAM cell(ns)	Proposed 2T2M(ns)
Read	0.15	0.111

5. Conclusion

This paper presented a new TG base 2T2MRRAM cell using memristor as memory element. Write delay is reduced using transmission gate as access transistor. Since read operation is differential, the proposed cell is more immune to PVT variations. Also it is more power efficient compared to conventional SRAM cell and saves area. Moreover, results obtained from simulation show that read and write delays are comparable to conventional SRAM cell. Therefore, proposed RRAM cell is the most suitable candidate for future memory applications.

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