Indian Journal of Science and Technology, *Vol 9(42), DOI: 10.17485/ijst/2016/v9i42/99482,* November 2016
ISSN (Print) : 0974-6846
ISSN (Online) : 0974-5645

Study and Design Evaluation of RF CMOS Oscillators

M. Sumathi*, R. Narmadha and K. Sumathi

Sathyabama University, Chennai - 600119, Tamil Nadu, India; sumagopi206@gmail.com, narmadha1109@gmail.com, sumathi.ece@sairamit.edu.in

Abstract

Objectives: To design and analyze the performance of CMOS RF Oscillator circuits at low supply voltage. Methods/Statistical Analysis: The Current Mode Logic (CML) based oscillator and LC oscillator is designed for 5GHz WLAN applications. The CML design adopts a DCO topology and the schematic layout is drawn using Microwind 2.7. The performance analysis is carried out using Intel Core2 Duo CPU E7400 @ 2.80 GHz processor. Advanced Design System 9.0 is used to implement schematics for analyzing the performances of proposed LC tank oscillator. Findings: The simulated results show that the tri-state inverter based DCO has 20 to 30% power reduction which is more than other conventional oscillator circuits. The CML inverter based DCO consumed more power than tri-state inverter because it used tail current transistor that provides always the static path from supply to ground. The theoretical phase noise is compared with simulated value of –95.19 dBc/Hz at same offset frequency. Application/Improvements: These designs produce a substantial improvement in performance and may be easily integrated with RF front-end blocks with minimal interface problems.

Keywords: Current Mode Logic, CMOS Technology, Oscillator, Radio Frequency Design

1. Introduction

Today there is an increased market demand for portable wireless communication devices and high speed computing devices. This is true because low cost and high integration have resulted in the commercial success in wireless communication integrated circuits. But these devices are operated by batteries which have only a limited lifetime. The battery technology has not improved in par with electronics technology. As the developments in battery technology have failed to keep up with increasing current consumption in wireless communication devices, innovative circuit design techniques are required in order to reduce the power consumption and to utilize the low voltage. Today the trend of RF CMOS design is technology scaling towards the deep submicron process to achieve improvement in power consumption, speed and chip area. Due to the growing demand for larger bandwidth and high speed communication high frequency wireless transceivers/multi-standard receivers require high performance Voltage Controlled Oscillators (VCO's) with excellent properties such as frequency tuning, phase noise, output power and oscillation amplitude[1]. In the case of direct conversion receivers, Local Oscillator (LO) signals are required to drive down-conversion mixers. Most of the modern communication systems use frequency or phase modulated signals which require mixing with In-phase (I) and Quadrature (Q) signals to avoid signal overlapping[2,3]. CMOS is one of the most popular technologies for the integrated circuit design and fabrication. Based on this technology, a Digitally Controlled Oscillator (DCO) or a VCO can be implemented by using either the ring topology or LC resonant structure. An oscillator generates a periodic time varying signal by the application of DC power. It provides an output at a specific frequency with no input signal being required. Figure 1 denotes the basic block diagram of an oscillator. It consists of an amplifier and a feedback network constructed by the resonator. The principle of operation is as follows. When dc power is first applied to the circuit, initially noise is amplified by the amplifier and then fed to the input through the feedback network or frequency selector that is a resonant circuit with filter function. The feedback network allows the signal frequency and equals the resonant frequency

*Author for correspondence

to pass and rejecting other frequencies. The feedback signal is amplified and fed back again. If the feedback signal is in phase with the input signal and voltage gain is enough, therefore the oscillation begins at the output[4,5]. In this research, the realized CMOS oscillator designs use negative feedback circuits which require a phase shift of 180°. In order to analyses the fundamental properties, an oscillator is referred as VCO, it means that an oscillation frequency can be varied by control voltage or the control voltage has been set to centre the VCO at particular frequency. For the ideal VCO, the output frequency is a linear function of the V_{TUNE} in time domain and it is given in Equation (1).

$$V_{OUT} = V_P \cos(2\pi ft + \psi) \quad (1)$$

Manuscripts where V_p is the amplitude of the VCO, f and Ψ are phase parameters and f is based on the V_{TUNE} . In frequency domain, the expression for VCO output is provided in Equation (2),

$$\omega_{OUT} = \omega_0 + K_{VCO} V_{TUNE} \quad (2)$$

Must where ω_{OUT} is the output frequency, ω_0 is the fundamental frequency without any gain and K_{VCO} is the frequency tuning gain. That is, the output frequency of the VCO can continually be changed in the frequency tuning band based on the change of the tuning signal. Oscillators generally produce fairly sinusoidal signals, but the noise inside the oscillator leads to variations in the generated signal. In the time domain, it leads to "jitter" at the fundamental frequency, i.e., the period of the signal varies very slightly from one time to another. In the frequency domain, it is called as "phase noise" which leads to a rapidly decreasing power around the desired frequency[6,7]. The phase noise representation is shown in Figure 2.

Now the non ideal VCO can be described as,

$$V_{OUT} = V_P A(t) \cos(2\pi ft + \psi) \quad (3)$$

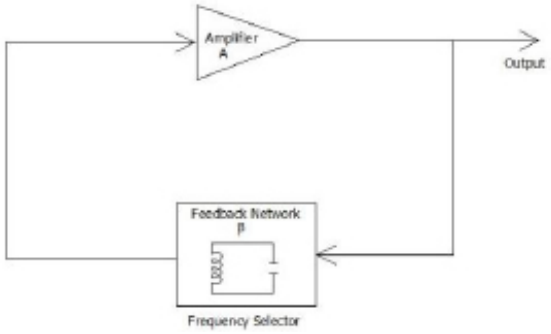

Figure 1. Block diagram of an oscillator.

Where, $A(t)$ represents the other frequency fluctuations, including random signals. In the frequency domain, the non-ideal frequency fluctuations would give the symmetrical distribution sidebands closed to as shown in Figure 3. In general, phase noise is characterized in terms of the single sideband power ($P_{sideband}$) and signal carrier power at oscillation frequency ($P_{carrier}$). Phase noise has units of decibels below the carrier per Hertz (dBc / Hz) and is defined in Equation (4),

$$L_{total}(f, \Delta f) = 10\log_{10}\left[\frac{P_{sideband}(f + \Delta f, 1Hz)}{P_{carrier}}\right] \quad (4)$$

Where, $P_{sideband}(f+\Delta f, 1Hz)$ denotes the signal sideband power at the oscillation frequency plus offset frequency Δf with a measurement bandwidth of 1Hz.

If the $P_{carrier}$ is greater than $P_{sideband}$, then the reduction in phase noise will be improved[8]. There are two major types of implementation in CMOS oscillators, first one is ring oscillator and the second one is LC oscillator. In this paper, circuit designs for Local Oscillator (LO) signal generation is prescribed. The work is organized as follows; Section 2 highlights the design of CML oscillator in DCO topology and LC Oscillator. The simulated results and conclusion are given in Section 3 and 4.

In GHz frequency applications, ring topology is usually preferred because it's improved noise performance and lower power consumption. It avoids the use of spiral inductors which are employed in LC tank oscillators. But these oscillators need to be realized by using digitally controlled logics with efficient delay elements for high

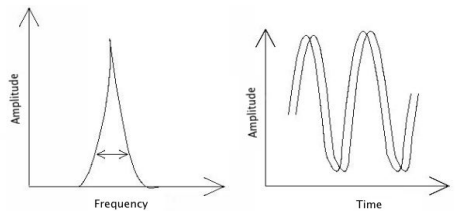

Figure 2. Phase noise.

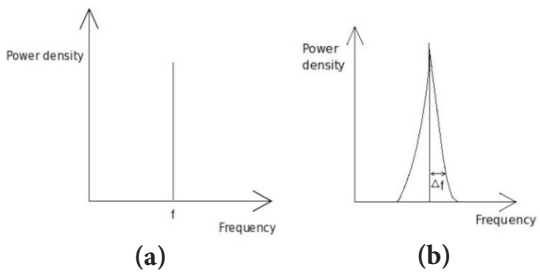

Figure 3. Power density of VCO. (**a**) Ideal. (**b**) Non ideal.

frequency generation. Few designs are observed from literatures, which are used to describe an implementation of a voltage-controlled oscillator using 1P8M 0.13–μm CMOS process[9,10]. The mixer structure composed of transconductance and switching stage nMOS transistors. It has an input 1dB compression point of -3.89 dBm and conversion gain of –0.96 dB. The designed VCO uses cross coupled nMOS transistors with LC feedback elements. The oscillation frequency of VCO is 5 GHz and has a phase noise value of -109 dBc/Hz at 1 MHz offset. In this design, the output buffers and bias network are added for performance improvement. The frequency divider is additionally used to improve the 6 dB oscillator phase noise. This paper presents a simple architecture for 1.1GHz, 8-bit Digitally Controlled Oscillator (DCO) on a 3-stage ring topology in TSMC 0.35–μm CMOS technology. A tri-state inverter is used as the delay element. The proposed oscillator design has been simulated and yields a phase noise of -106 dBc/Hz at 1 MHz. It provides a large tuning range from 333 MHz to 1472 MHz. The consumed power is 63.4 mW from 3 V power supply[11,12]. By providing proper delay and optimized width of the transistors, the design performance can be improved even under low supply voltage.

Another work is highlighted that comparison of phase noise models on a class of differential saturated ring oscillator. A 3-stage 1 GHz differential pair ring oscillator has been designed. The ring oscillator delay cells used are differential inverters whose outputs reach the power supply within the period of oscillation. The delay cell structure involves load resistors, nMOS differential pair, and two nMOS tail current transistors are serially connected with ground[13,14].

Two parameters, single stage jitter or variance and phase noise have been considered for performance comparison. The simulation results presented show that the proposed model can improve accuracy to 7–10 dBc/Hz. It is observed that a static path always exists between supply voltages and ground in delay cell if tail current source used[15,16]. Therefore, power consumption will be more in this design and moreover load resistors occupy large area in silicon. The surveyed literatures helped us to get a detailed idea in design and performance aspects of front-end circuits. It motivated to find an alternative structure of RF CMOS oscillators. The design of Current Mode Logic (CML) delay inverter and D-type latch whose performance analysis was done with conventional CMOS inverter and latch using Microwind software in our initial stage of research work[17] that is published in IEEE international symposium on "Microwave, Antenna, Propagation and EMC Technologies'2007. The proposed delay cell is utilized in the design of 5 GHz DCO, which is one of the design stages of this work. Reported LC oscillator designs provided changes only to the elements in tuned circuitry and analyzed the performance. It is clearly understood that the performance of oscillators can be improved either by increasing the supply voltage or by providing additional stages at the output. The above mentioned problem motivated to introduce an efficient oscillator designs under low operating voltage for 5GHz wireless applications.

2. Proposed Designs

The goal of the proposed work is to design a novel structure of oscillators in order to achieve higher performance. High frequency oscillators are also designed in ring topology and LC tank topology for LO signal generation. An improved structure of CML inverter and a tri-state inverter are used as delay elements in ring oscillators. In the LC oscillator design, a novel cross–coupling topology is used at the amplifier stage and a high Q inductor is used for betterment of low phase noise. A conventional ring oscillator which is shown in Figure 4 is a closed–loop chain of equal gates such as inverters. Each inverter in the ring oscillator is used as delay cell.

The frequency of oscillation of the ring oscillator is determined by Equation (5),

$$f_{OSC} = \frac{I_d}{2nC_L\Delta V} \tag{5}$$

where n is the number of delay cells or inverters used and C_L is the load capacitance, ΔV is the output voltage swing and I_d is the driving current to the load. From Equation (5), it is of interest that the frequency of oscillation can also be varied by changing the load capacitance. The designed ring oscillators are realized in digitally controlled logics and are suitable for generating the 5 GHz LO signal frequency. The first DCO uses Current-Mode Logic (CML) inverter and the second one uses tri-state inverter.

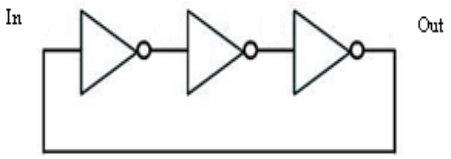

Figure 4. Block diagram of ring oscillator.

Using μ-Wind software, the design and performance of DCO's are analysed in simulation phase at layout level.

2.1 CML Inverter based DCO

Figure 5 shows the CML delay cell structure which has an nMOS differential pair of transistors (M1, M2) and tail current source transistor (M5). The gate input terminals of transistors are represented as D, DBAR. Two grounded pMOS transistors (M3, M4) are used as the load. CML logic structure works for smaller signal amplitude and faster than the CMOS logic and the power consumption is nearly independent of the operation frequency. The evaluated designs by making use of CML is more suitable for high frequency applications. The normal and complementary inputs are connected by an inverter to apply clock input. Only normal output signal is processed by an inverter delay cell. The complementary output signal is not used for the process. A single CML inverter layout is also shown in Figure 6. The layout window features a grid scaled in lambda units. The lambda unit is fixed to half of the technology scale. For 0.18-μm technology, the lambda (λ) is 0.09–μm.

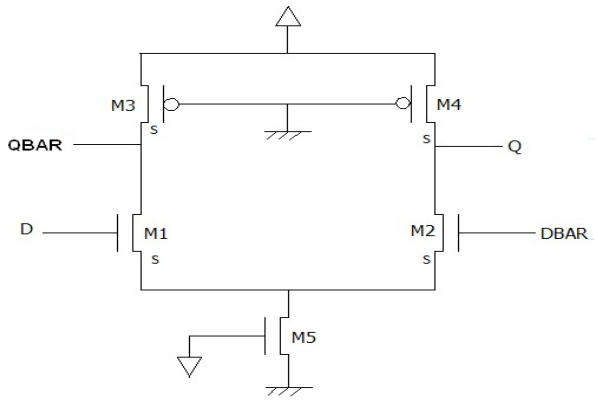

Figure 5. CML delay cell structure.

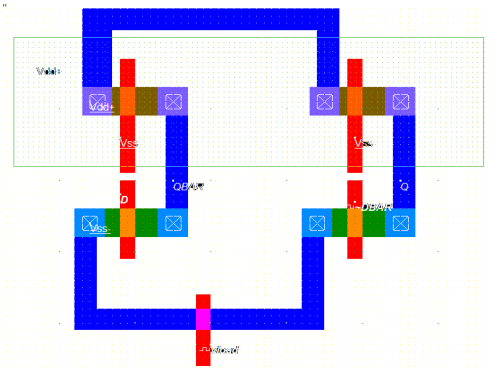

Figure 6. Layout of single CML delay cell.

The designed 3–stage CML inverter based DCO schematic is shown in Figure 7. It is developed for 8 control bits. All the stages in the schematic are identical and make a ring for an individual bit. Each ring is made with identical stages to provide equal delay. Each ring has three CML inverters. There are totally 8 rings used and arranged in parallel. It is developed for 8 control bits. All the stages in the schematic are identical and make a ring for an individual bit. Each ring is made with identical stages to provide equal delay. Each ring has three CML inverters. There are totally 8 rings used and arranged in parallel. The output frequency of the oscillator depends on the value of control bits, which is equal to HIGH. Layout is drawn for 8 ring CML structure and is optimized to reduce circuit parasitics.

2.2 Tri State inverter based DCO

In the conventional topology of tri-state inverter, structure is in cascade connection of transmission gate and an inverter. In this work, the inverter shown in Figure 8 is composed of direct signaling transmission gate transistors M1, M2 and CMOS inverter (M3, M4).

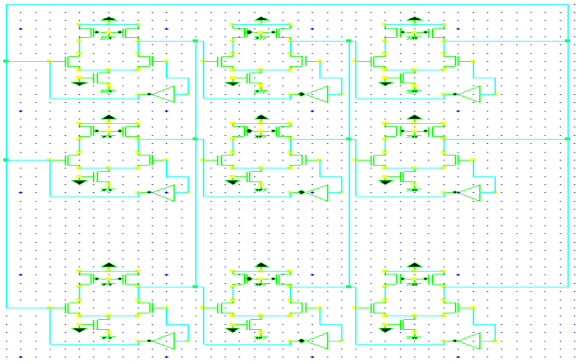

Figure 7. CML inverter based DCO topology.

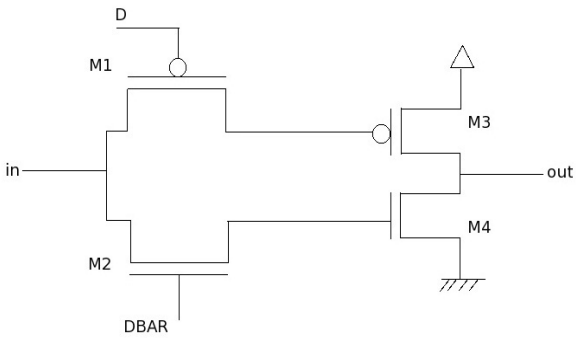

Figure 8. Tri-state inverter delay cell.

D and DBAR are the control inputs of the tri-state inverter. Only when DBAR is equal to 1, the signal propagation takes place from input to output. The propagation delay of tri-state inverter is sum of the delays of transmission gate and CMOS inverter. The size (W/L ratio) of the transistors is decided with respect to size ratio of the CMOS inverter. The W/L ratio of the delay cell is evaluated with the help of associated factors of propagation delay, supply voltage, load capacitance and impedances of transistors. The size of the single delay cell transistors is given in Table 1. These values are applied to an entire DCO structure and simulation processing steps are carried out.

The designed 3-stage tri-state inverter based DCO schematic is shown in Figure 9. The inverter symbol is used to process the normal and complementary control inputs. The output of each inverter delay cell is connected with the input of the other inverter delay cell and forms a ring topology. The performance of ring oscillators is analysed using Microwind software incorporated with a desk top system Intel core 2 duo CPU E7400 working at 2.80 GHz. The simulated results are provided in the next section. Another type of 3 GHz oscillator is designed in VCO LC topology and its performance is validated through ADS simulation.

2.3 LC Oscillators

LC oscillators are of the most common type used in the RF IC design. It can be designed for a fixed frequency or variable frequency. In general, the tuned and amplifier parts of oscillator are responsible for frequency of oscillation. The performance of the oscillator is determined by the quality factor of the LC resonator. There are two design possibilities to realize a VCO such that, either the oscillation frequency can be varied by control voltage or the control voltage has been set to center the VCO at a particular frequency. The conventional LC VCO is shown in Figure 10.

It consists of a cross-coupled transistor pair (M1, M2) and an LC tank used to set the desired frequency of oscillation. The cross-coupled transistors generate the negative resistance that starts the oscillation and compensates the losses of the tank. The tail current source at the bottom of the circuit can be applied to control the current flowing in the oscillator, and hence the power consumption and phase noise. A tail capacitor is generally connected in parallel with it in order to eliminate the effect of the tail transistor noise on the oscillator. This type of oscillator is also named as "negative-g_m oscillator because the input resistance of the conventional design is inversely proportional to the negative transconductance (g_m) of oscillator. Many reported designs[18–20] have concentrated only on providing changes of elements in tuned circuitry and analyzed the performance.

Table 1. Size of the transistors in tri-state inverter

Delay cell transistors	M1	M2	M3	M4
W/L ratio	3.0	1.0	3.0	1.0

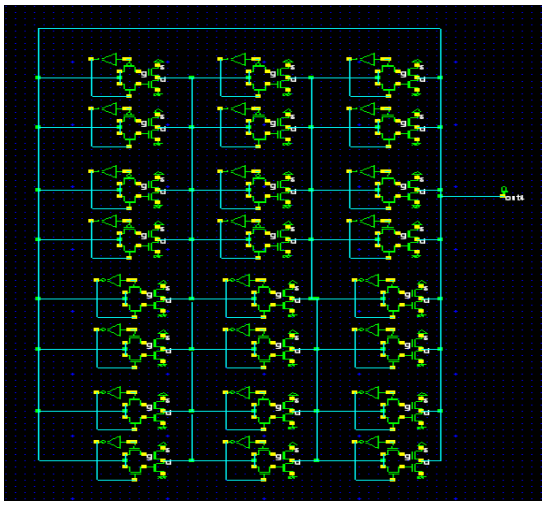

Figure 9. Tri-state inverter based DCO topology.

2.4 Dual Cross-Coupled LC Oscillator

The cross–coupling VCO structure with revised amplifier circuitry is used in this LC oscillator design. The basic difference between this proposed design and the conventional design is that four nMOS transistors are used in cross-coupling structure on against the two used in the previous design for betterment of oscillation and phase noise. It is titled as "Dual cross-coupled LC oscillator. Figure 11 represents the proposed LC oscillator. It consists of cross coupled pair of nMOS transistors (M1, 2 –M3, 4) and two pMOS transistors (M5-M6) with tail current

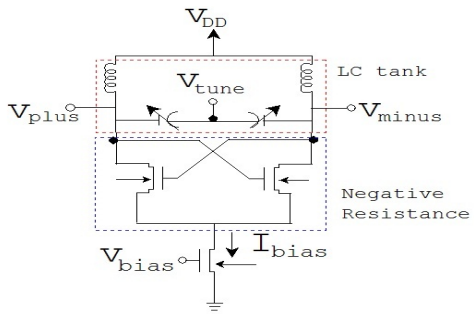

Figure 10. Conventional LC Oscillator.

source. The high Q off-chip inductor is used as a feedback element which is placed with series connection of capacitors. The proposed active part of circuitry compensates the losses in LC tank and provides stable oscillation. The Q of the resonator depends on the Q's of the inductor and variable capacitor. The values of Q are 5 and 40 respectively. The W/L ratio of active devices is calculated from this design Equation (6),

$$\frac{W}{L} = \frac{g_m^{\,2}}{2(K_n I_D)} \tag{6}$$

where K_n is the process dependent term and I_D is the drain current. The proper value of g_m and inductor L decides the entire performance of the VCO. The minimum value of g_m to be greater than 8 mS for better oscillation and I_D is assumed to be 5 mA. The design formula for process dependent term of nMOS transistor (K_n) is expressed in terms of mobility of charge carriers and oxide thickness of the transistor. It is shown in Equation (7).

$$K_n = \frac{\mu_n \varepsilon_o \varepsilon_s}{t_{ox}} \tag{7}$$

One of the performance factors of the oscillator is the phase noise and the most popular Leeson's phase noise model equation is used in this design study. The value of phase noise is theoretically estimated by using Equation (8),

$$L(\Delta f) = 10\log_{10}\left(\frac{kTR_{eff}(1+A)\left[\frac{f}{\Delta f}\right]^2}{\left[\frac{V_p^2}{2}\right]}\right) \tag{8}$$

Where, R_{eff} is the effective series resistance of the LC-tank and A is the start-up safety factor. f is the oscillation frequency with value of 3.25 GHz, Δf is the frequency offset with value of 1MHz, T is the absolute temperature of 293° Kelvin, V_p is the peak amplitude of the output with value of 1.5 V. k is the Boltzmann constant. By substituting these values, at 1 MHz frequency offset, the value of phase noise is nearly equal to -109.26 dBc/Hz. From this design study, it is understood that low phase noise performance of oscillator is achieved only by high Q bond-wire inductors in off-chip. Low Q on chip inductors is to be avoided in LC oscillator design.

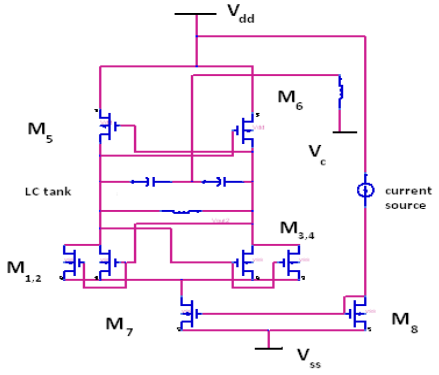

Figure 11. Dual cross-coupled LC oscillator.

3. Results and Discussions

The performance analysis of oscillators is carried out using the Microwind 2.7 version software. It is a CMOS circuit editor and simulation tool, for logic and layout-level design, running on Microsoft Windows. Microwind's layout library (MOS generators and Cell compiler from Verilog-HDL description) is used progressively to ease the layout design phase. This software is used to design and simulate an oscillator at physical description level. The single bit tri-state inverter and CML inverter based ring oscillator layout are shown in Figure 12 and Figure 13. The layout simulation of an 8-bit tri-state inverter based DCO, voltage versus

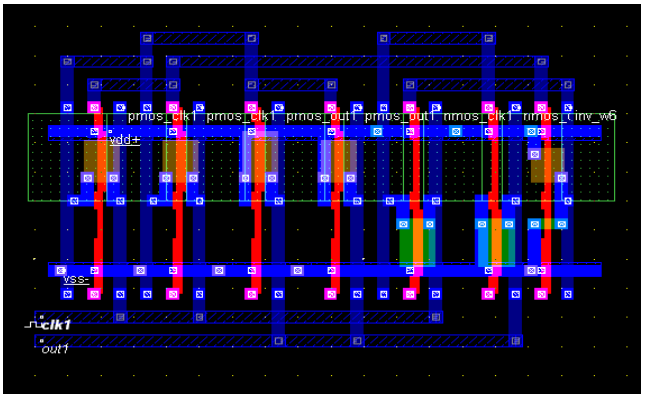

Figure 12. Layout of single bit tri-state inverter based oscillator.

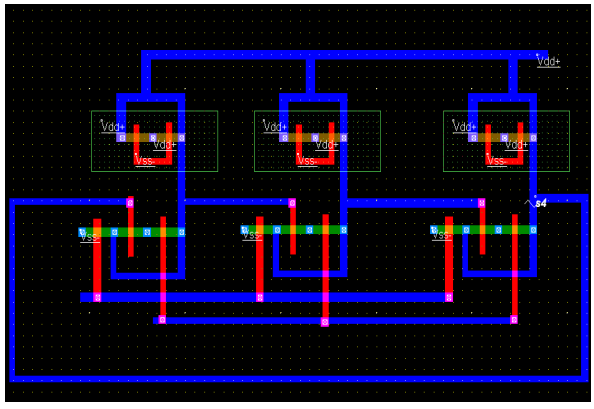

Figure 13. Layout of single bit CML inverter based oscillator.

time are shown in Figures 14 and 15 respectively. Both oscillators are capable of generating signal frequency of 5 GHz. The simulated results show that the tri-state inverter based DCO has 20 to 30 % power reduction which is more than other conventional oscillator circuits. The CML inverter based DCO consumed more power than tri-state inverter because it used tail current transistor that provides always the static path from supply to ground.

The software does not support analog design to the required extent. The phase noise of ring oscillators is not discussed in this thesis. Further, the research is extended with the design of LC oscillators and the value of phase noise is estimated with respect to theory and practical concepts. The performance of LC oscillator is analysed for the control voltage of 2.5 V. It is used to center the VCO at particular frequency. The performance metrics are output frequency, phase noise and output power respectively. Figure 16 shows the 3.25 GHz measured oscillation frequency in a 0 to 600 picoseconds span. The frequency of oscillation is determined from the reciprocal of the time period of one complete cycle.

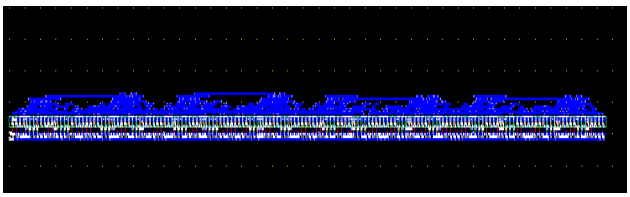

Figure 14. Layout of 8-bit tri-state inverter based DCO.

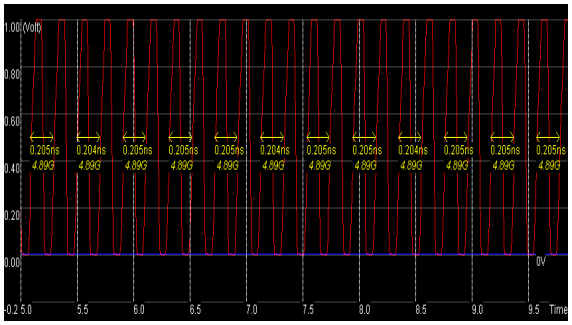

Figure 15. Output waveform of 8-bit tri-state inverter based DCO.

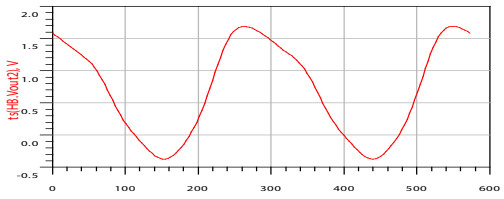

Figure 16. Output waveform LC oscillator.

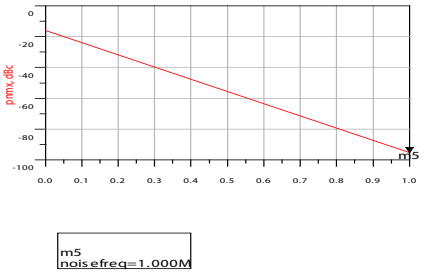

Figure 17. Phase noise of LC oscillator.

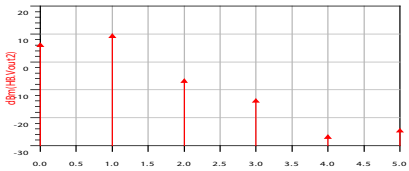

Figure 18. Harmonic spectrum of LC oscillator.

The theory of LC oscillator is validated by simulations using ADS software. Harmonic balance test set up is used to predict output frequency, output power and phase noise performance. The theoretical phase noise of -109.26 dBc/Hz is calculated with respect to V_p at 1 MHz offset. V_p is the peak amplitude of the output. The theoretical performance of oscillator is validated by the simulation result. A simulated phase noise of -95.19 dBc/Hz is measured at same offset frequency. Figure 17 shows the measured phase noise between 100 KHz and 1 MHz offset of the 3.25 GHz carrier frequency.

The predicted output power is 10 dBm that is observed from the graph of harmonic spectrum as shown in Figure 18. The harmonic content is quite high and therefore a buffer stage with a tuned output is required to improve further the phase noise.

4. Conclusion

The design and simulation process have been carried out in a standard TSMC 0.18-μm CMOS process technology. The performances of oscillator circuits are analyzed by using Intel Core2 Duo CPU E7400@2.80 GHz processor with Agilent's Advanced Design System (ADS) 2009 version and Microwind 2.7 version software. TSMC 0.18 micron CMOS logic process is the widely used for various electronic systems such as microprocessors, microcontrollers and high speed processors. It provides the device models under the operating voltage of 1.8 V. Therefore, this technology scale is utilized for realizing

oscillator designs. TSMC 0.18-µm RF CMOS models used in this work and the performance analysis of oscillators is carried out in layout level design using Microwind software. Further, the theoretical performance of LC oscillator is validated by simulation using ADS.

5. Acknowledgment

The author would like to thank RF and Microwave lab members for helpful discussions and encouragement.

6. References

1. Soltanian B, Peter R, Kinget K. Tail current-shaping to improve phase noise in LC voltage- controlled oscillators. IEEE Journal of Solid-State Circuits. 2006; 41(8):1792–802.
2. Liu HQ, Goh WL. Design and frequency/phase analysis of 10GHz CMOS ring oscillator with fine frequency tuning. Springer Science Journal. Analog Integr Circ Sig Process. 2006; 48(2):85–94.
3. Lee SY,Chen CY. Analysis and design of a wide-tuning range VCO with quadrature outputs. IEEE Transactions on Circuits and Systems. 2008; 55(12):1209–12.
4. Rahimi M. Design and simulation of a 2.4 GHz VCO with high Q MEMS inductor. International Journal of Computer and Electrical Engineering. 2009; 1(3):251–7.
5. Leung B. Comparison of phase-noise models on a class of ring oscillators using low voltage swing fully differential delay cells. Analog Integr Circ Sig Process, Springer Science Journal. 2009; 61(2):129–47.
6. Lee L, Thomas H. The design of CMOS radio frequency circuits. Cambridge, United Kingdom: Cambridge University Press; 1999. p. 309–13.
7. Behzad R. RF microelectronics. Upper Saddle River. NJ: Prentice Hall; 1998. p. 38–4.
8. Leung B. VLSI for wireless communication. Prentice Hall; 2002.
9. Cornetta G, David J, Santos S. 130 nm CMOS mixer and VCO for 2.4 GHz low-power wireless personal area networks. International Journal of Electronics, Circuits and Systems. 2008; 2(4):194–9.
10. Naimi HM, Ghonoodi H. Analysis of phase accuracy in CMOS quadrature LC oscillators. Springer science, Analog Integrated Circuits and Signal processing. 2011; 67(2):110–9.
11. Ho SSK, Carlos E, Saavedra S. A low-noise self-oscillating mixer using a balanced VCO load. IEEE Transactions on Circuits and Systems-I. 2011; 58(8):1705–12.
12. May A, Tomar T, Pokharel RK. Design of 1.1 GHz DCO ring oscillator. IEEE International Workshop on RFIT; 2007. p. 82–6.
13. John P, Uyemura U. Chip design for submicron VLSI: CMOS layout and simulation. 1st ed. Cengage Learning Ltd; 2006.
14. Sicard E , Bendhia SD. Basics of CMOS cell design. 1st ed. Tata McGraw Hill Ltd; 2007.
15. Ramaiah H. Design of low phase noise, low power ring oscillator for OC-48 application. IETE Journal of Research. 2012; 58(5):425–8.
16. Das B, Abdullah MFL, Shahida MSHN, Bakhsh Q. Current mode logic based semiconductor laser driver design for optical communication system. Indian Journal of Science and Technology. 2016 Mar; 9(10):1–6.
17. Sumathi M, Karthik Y. Performance analysis of CML logic gates and latches. IEEE International Symposium on Microwave, Antenna, Propagation and EMC Technologies for Wireless Comunications. IEEE Digital Library. 2007; 1(5):1428–32.
18. Manzoor M, Verma S, Singh T, Manzoor M. Various techniques to overcome noise in dynamic CMOS logic. Indian Journal of Science and Technology. 2016 Jun; 9(22):1–7.
19. Bhat S, Choudhary S, Selvakumar J. Design of low voltage CMOS OTA using bulk-driven technique. Indian Journal of Science and Technology. 2016 May; 9(19):1–6.
20. Harada Y, Fujimoto K, Eguchi K, Fukuhara M, Yoshida M. Design of a wide range hamming distance search circuit using neuron CMOS inverters. Indian Journal of Science and Technology. 2016 Jul; 9(28):1–5.