Indian Journal of Science and Technology, Vol 9(42), DOI: 10.17485/ijst/2016/v9i42/101849, November 2016
ISSN (Print) : 0974-6846
ISSN (Online) : 0974-5645

Implementation of 5 Phase 3 Level NPC Inverter using Space Vector Modulation

R. Palanisamy*, K. Vijayakumar, K. Selvakumar, D. Karthikeyan and G. Santhoshkumar

Department of EEE, SRM University, Chennai - 603203, Tamil Nadu, India; krspalani@gmail.com, selvakse@gmail.com, karthipencil@gmail.com, santhoshkumar.g@ktr.srmuniv.ac.in, kvijay_srm@rediffmail.com

Abstract

Objectives: The implementation of five phase three level Neutral Point Clamped (NPC) inverter is illustrated using space vector modulation technique based on the optimized five vectors switching strategy. **Methods/Analysis:** In 5 phases 3 levels NPC inverter consists of 243 switching state vectors, which can be reduced to 113 states by optimized Space Vector Modulation (SVM) switching strategy. The system has 11 sectors, which is converted into 6 sectors in that sub regions can be identified by optimised technique in d-q voltage vector. Simulation results of the five phase three level neutral point clamped inverter using SVM verified using Matlab/Simulink. **Findings:** SVM utilities switching states among the available various redundant states to reduce the common mode voltage and capacitor balancing problem. Dwell time calculations for this proposed does not need of any lockup table and park transformation. It's applicable for high power medium voltage, remote sensing and industrial applications. **Novelty/Improvement:** The 3level 5phase NPC inverter has improved power density of the machine, enhanced dissection of power source among the inverter legs, abridged amplitude and augmented frequency of the torque pulsation than the traditional inverters.

Keywords: Neutral Point Clamped Inverter (NPCI), Optimised Space Vector Modulation (OSVM), Pulse Width Modulation Method (PWM), Switching States

1. Introduction

In recent years the multilevel inverters used for high power medium voltage, remote sensing and industrial applications. The multilevel impression has been initiated from 1975. The phrase multilevel began with the three level inverter and its goes up to n level[1]. Consequently, many topologies of multilevel inverter are initiated. Conversely, the uncomplicated perception of a multilevel inverter to accomplish the high power is to make use power switches connected in series with many low voltage dc sources to execute the power adaptation by amalgamate a staircase output voltage level waveform[2]. Multiple dc sources like as fuel cells, batteries, renewable energy sources, capacitors and other devices[3]. The augmented admiration of multilevel inverter is owing to the precincts of the conservative 2 level output inverters in management for high power adaptation. The multilevel inverters reduce the total harmonic level and also when the number of level increases, the ripple content commences to diminish. To generate stepped waveform the multilevel inverter includes an array power semiconductor switch, capacitors, voltage sources and clamping diodes[5]. The recompenses of multilevel inverter are the dv/dt anxiety on the each switching state devices are abridged due to the diminutive growth in output voltage steps and minimised electromagnetic compatibility[6]. When activated at high voltage smaller rating of output voltage in expression of less ripple content, lower harmonics contents and lower switching losses[7]. Additionally, the multifaceted phase changing transformers that are compulsory in the multi pulse inverters at higher level are not unavoidable obligatory, thus helps in minimizing the expenditure of the system[8].

*Author for correspondence

One of the multilevel structures that has added much notice and broadly used is the NPC-MLI or also known as DC-MLI. This arrangement was first anticipated by Nabae[9]. The multilevel inverter scheme not only accomplishes with high power rating content, but as well facilitates the use of the renewable energy sources[10,11]. The renewable energy sources like as PV array, wind energy, battery cells and the fuel cells are effortlessly linked with multilevel inverter scheme for high power medium voltage application. The NPC inverter applications includes the distinctive functions are IPFC, SSSC, power quality issues, power conditioners for removing sag and swells, real and reactive power compensators and grid connected PV systems[12,13].

In the proposed system with 5 phase 3 levels NPC inverter implementation by using the Optimised Space Vector Modulation (OSVM), which is used to diminish the common mode voltage, total harmonic distortion and capacitor balancing. And it's executed by selecting the switching states among the various redundant switching states by optimized five vectors selection process.

2. Three Level 5 Phase NPC Inverter Scheme

The NPC multilevel inverter scheme amalgamates the very diminutive step of staircase output voltage from numerous levels of the DC capacitor voltage variations. A k level NPC-MLI inverter contains of (k-1) capacitors on DC bus link, 2(k-1) power switching vector devices per phase and 2(k-2) variable clamping diodes per phase. The capacitors used in 3 level inverter are C1 and C2, which divides the DC bus voltage split into 3 level[14]. Each capacitor divides voltage as $V_{dc}/2$ volts and voltage pressure will be inadequate to one capacitor level throughout clamping diodes. The Figure 1 demonstrates the 5 phase 3 levels NPC inverter scheme[15].

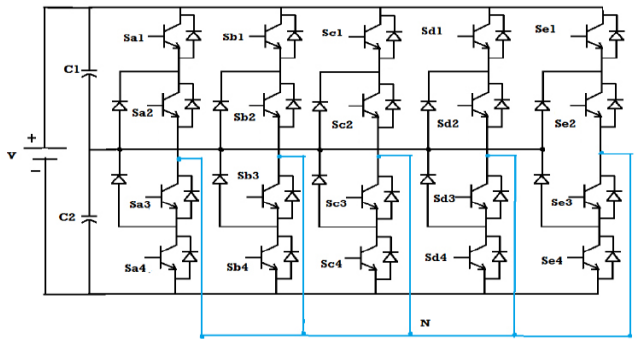

Figure 1. 3 level 5 phase NPC- inverter.

In this proposed system, which consists of 5 phases (5 legs) and each phase contains 4 switches[16]. From the Figure, each leg can be operated in 3 switching states like +Vdc/2, 0, -Vdc/2. In multiphase system have more advantages compare to three phase system like,

- Concentrated peak value and improved switching frequency.
- System with enhanced power density.
- Abridged total harmonic distortion.
- Power division between the inverter legs are enhanced.
- Reduced current harmonics and capacitor balancing.

The switching states of NPC inverters depends on n^m, where n- no. of levels and m- no. of phases[17]. In 3 level 5 phase NPC inverters, this contains totally 35 = 243 switching states. And it has two dc link capacitors connected in the inverter switches. The modes of operations shown in Figure 2.

3. Optimized Space Vector Modulation (OSVM)

In a complex plane, the switching vectors are identified by control variables given by the control system[18]. SVM is a Digital PWM scheme used to generate switching for power switches placed in the NPC-MLI[19]. So to Control the selected switch state duty cycle is easy and maximum

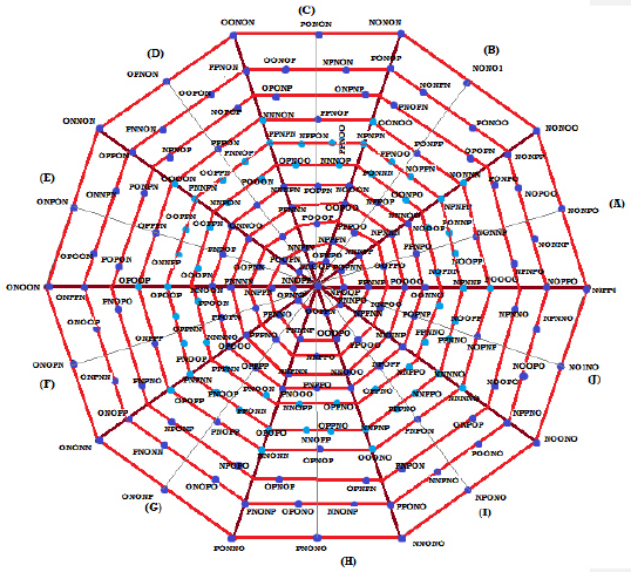

Figure 2. Structure of SVM for 3level 5phase inverter (d-q).

utilization of DC Link voltage[20]. SVM concept can be viewed as weighted average using of the output voltage to obtain maximum fundamental value with minimum harmonic content[21]. OSVM extravagance the sinusoidal voltage as a stable amplitude switching vector rotating at fixed frequency and control variable.

$$V_{sa1} = \frac{2}{5(V_{as} + a_n V_{bs} + a_n^2 V_{cs} + a_n^3 V_{ds} + a_n^4 V_{es})} \quad (1)$$

$$V_{sa3} = \frac{2}{5(V_{as} + a_n V_{cs} + a_n^2 V_{es} + a_n^3 V_{bs} + a_n^4 V_{ds})} \quad (2)$$

$$a_n = e^{\frac{j2\pi}{5}} \quad (3)$$

The Equations (1)-(3) show the voltage across the switches S_{a1} and S_{a3} of the 5phase 3 level NPC inverter. In this 5 phase 3 level system contains 10 sectors and each sector has 11 sub regions, which totally consists of 243 switching states shown in the Figure 3 (d-q).

It is recognized that the vectors on the outer most regions and the middle sub-regions can be used to realized the required output reference and so as to permutation of zero vectors. Generally the system will cause distortion and increase the switching loss of the system, when the vectors on the inner most vector sub-regions. So the total switching states for the sector 2 shown in the Figure 4. The each sector is divided into 2 regions are vertex and non-vertex regions based on that it classified into number of sub regions. For improving the output voltage, better current control and for reducing total harmonic distortion the inner most states in the sub regions are isolated. Only the medium and large vectors mostly used for reducing the common mode voltage and capacitor balancing.

A technique to eradicate gratuitous vectors is attractive to diminish the numeral of voltage switching vectors (from 243) consequently condense the intricacy of judgment apposite switching progression to devise the required output voltage orientation. The transformation linking decoupled position frame and the phase voltage reference frame equation can be represented as,

$$\begin{bmatrix} Vas \\ Vbs \\ Vcs \\ Vds \\ Ves \end{bmatrix} = \begin{bmatrix} 1 & \cos\alpha & \cos\cos 2\alpha & \cos 3\alpha & \cos 4\alpha \\ 0 & \sin\alpha & \sin 2\alpha & \sin 3\alpha & \sin 4\alpha \\ 1 & \cos 3\alpha & \cos 6\alpha & \cos 9\alpha & \cos 12\alpha \\ 0 & \sin 3\alpha & \sin 6\alpha & \sin 9\alpha & \sin 12\alpha \\ & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad (4)$$

Where,$\alpha = 2\pi/5$,

So each switching states are represented by its voltage values. For example [NNPPO] – which represents [$-V_{dc}/2$, $-V_{dc}/2$, $+V_{dc}/2$, $+V_{dc}/2$, 0] voltage levels. Based on these voltage level pole voltage relationships between phases are identified shown in Table 1. For producing better output voltage, current control and reduce THD value, reduced switching states space vector strategy implemented which is shown in Figure 5(d1-q1).

This reduces from 243 to 113 states. Then the amount stress in the each switches reduces, di/di value become

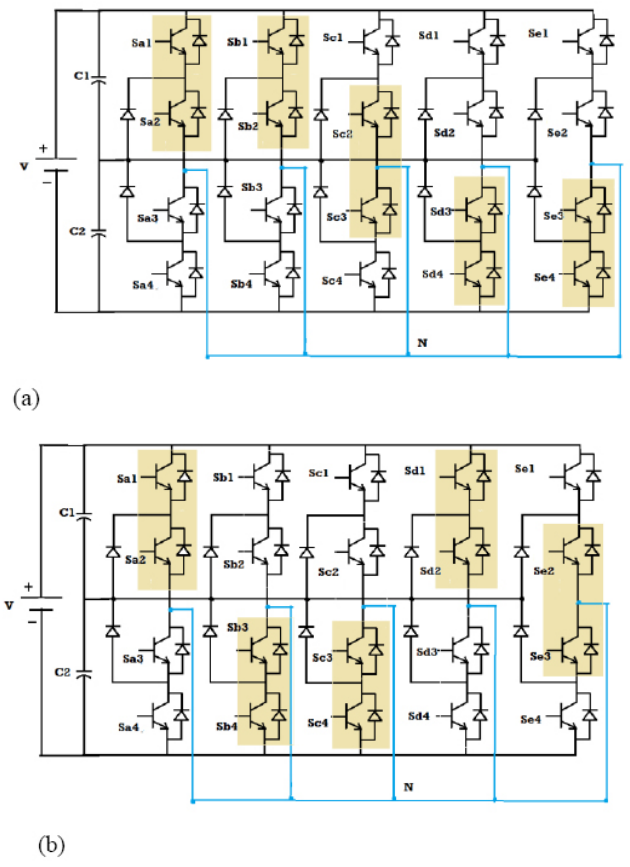

Figure 3. Modes of operation (a) PPONN (b) PNNPO.

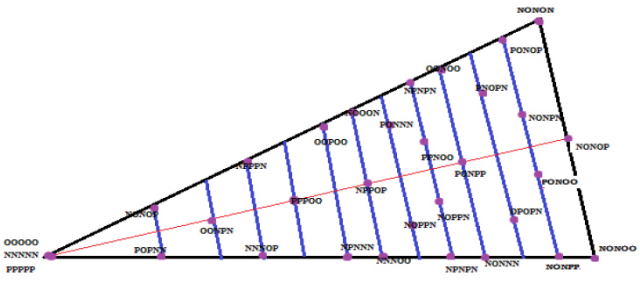

Figure 4. NPC inverter state in sector 2.

Table 1. Pole voltage between phases of various switching states

Switching States	Pole voltage relationship between phases
[NPNOP]	Vb0>=Ve0>=Vd0>=Vao>=Vc0
[NPNNP]	Vb0>=Veo>=Va0>=Vc0>=Vd0
[OOPNN]	Vc0>=Va0>=Vb0>=Vd0>=Ve0
[NPPPPP]	Vb0>=Vc0>=Vd0>=Ve0>=Va0
[ONNPP]	Vd0>=Ve0>=Va0>=Vb0>=Vc0
[PNPON]	Va0>=Vc0>=Vd0>=Vb0>=Ve0

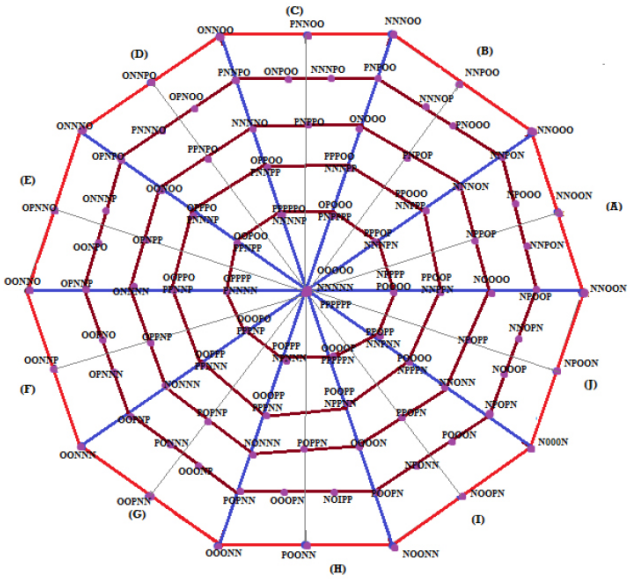

Figure 5. Reduced switching states for NPC-inverter based OSVM (d1-q1).

low. The regulations for the improvement of five phase three level SVM approach are as tracks,

- The switching space vectors are exploit to devise the required vector in the d-q vector space plane should be certain in a method that the amalgamation of the vectors in the d_1/q_1 vector space plane could affect in annulment in excess of the switching cycle.
- To diminish the switching defeat through the succession the inverter can only make one progress during each switching episode.
- Assortment of superfluous space vectors are preferable so that the neutral point capacitor voltage swells can be unprejudiced by altering the dwell time of the redundant switching voltage vectors. In the sector 2, after reducing the switching states are NPNNN, POPPN, NNOPN, OONNP, PPPPN, POPON, NONOP, PPNNO, OPOPN, and NPNPP by properly utilising these states the NPC inverter can operate in better conditions.

4. Dwell Time Calculations for Proposed System

In three phase two level systems, the output switching voltage reference value is engendered using the two vertex vectors of each vector of inner most the hexagon and a zero voltage vector. The region sheltered by these three state vectors is the regions; where the output voltage reference can be amalgamate. Conversely, the multi-phase scheme is dissimilar from the three phase arrangement as it is compulsory to abandon d_1-q_1 vector space plane constituent using suitable dwell time values. Bargain NPC inverter state in sector 2 is exposed in Figure 6.

This grades in a reachable section that the entrant switching vector progression can create being slighter than the region covered by the vectors used in the succession. The contender switching sequences are additional difficult than the five phase two level inverter scheme and the inflection approach engaged by three level three phase inverter scheme cannot be employed by the three level five phase inverter scheme. It is imperative to describe the reachable section of every of the ten switching succession in each sector. The following equation shows switching time estimation of 3 level 5 phase NPC inverter scheme.

$$\begin{bmatrix} T0 \\ T1 \\ T2 \\ T3 \\ T4 \\ \end{bmatrix} = \begin{bmatrix} Vd10 & Vd11 & Vd12 & Vd13 & Vd14 \\ Vq10 & Vq11 & Vq12 & Vq13 & Vq14 \\ Vd30 & Vd31 & Vd32 & Vd33 & Vd34 \\ Vq30 & Vq31 & Vq32 & Vq33 & Vq34 \\ 1 & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}^{-1} \begin{bmatrix} Vd1 \\ Vd2 \\ Vd3 \\ Vd4 \\ Ts \end{bmatrix} \quad (5)$$

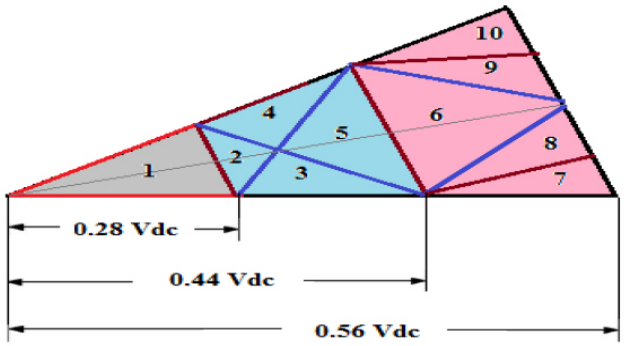

Figure 6. Reduced NPC inverter state in sector 2.

Here dwell times for switching states are T0, T1, T2, T3, T4 and voltage levels are varying from Vd1, Vd2, Vd3, Vd4. So the total switching time is,

$$T_s = T_0 + T_1 + T_2 + T_3 + T_4 \quad (6)$$

- Generally only one level can be transformed in switching states of each phase previously altering output state, which is used to avoid the output voltage from fabricating high di/dt.
- To decline switching loss, the number of distorted states in each phase of the system is not more than two in each control period of OSVM.
- Consider that each reference switching voltage vector has consequence on dc link neutral point voltage value; the particular vector should create neutral point voltage equilibrium.

5. Simulation Results and Discussions

The effort accessible at this point mostly spotlight on recuperating the power quality inserted to the grid scheme. It is imitation using Matlab/Simulink R2013a. The simulation of the proposed system has switching frequency of 10 kHz. In Figure 7 shows the output voltage of NPC-MLI, which is 200.5 V.

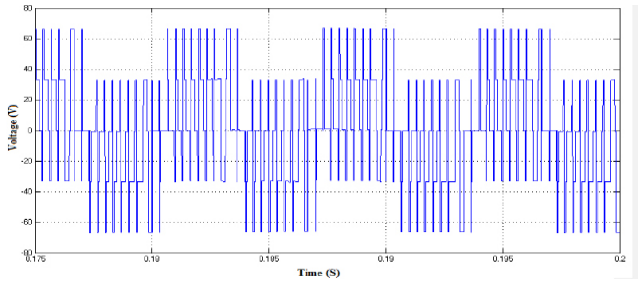

Figure 7. Common mode voltage level of NPC-MLI.

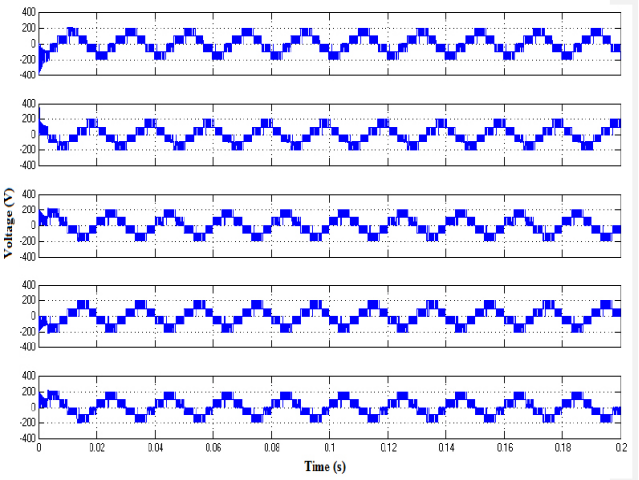

Figure 8. Line to line voltage of NPC-MLI

Common mode voltage levels of 5 phase 3-level NPC-MLI exposed in Figure 8. And the capacitor balanced voltage is exposed in Figure 9. The switching pulses of projected scheme and harmonic analysis of output voltage shown in Figure 10 and Figure 11 respectively.

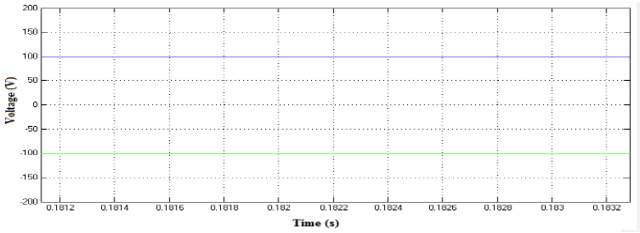

Figure 9. Capacitor balancing voltage.

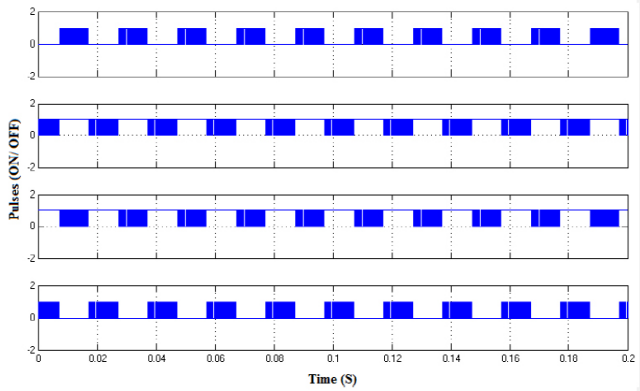

Figure 10. Switching pulses of leg 1.

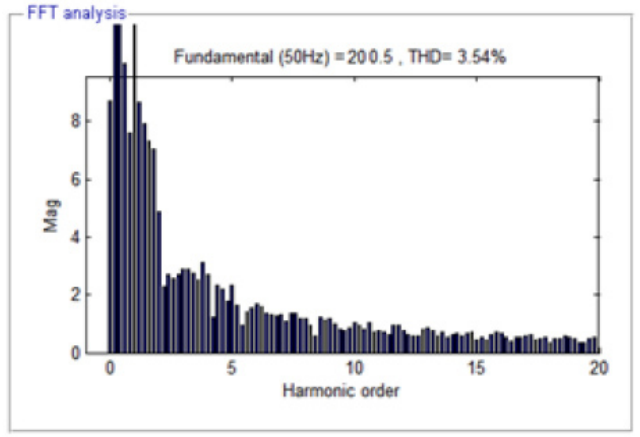

Figure 11. Harmonic analysis- NPC inverter output voltage.

6. Conclusion

The proposed system 3 level 5 phase NPC inverter was implemented and simulated in MATLAB environment, and it was observed that it reduces the voltage stress, reduces the THD, partial elimination common mode voltage and capacitor balancing voltage. The 3level 5 phase NPC inverter has improved power density of the machine, enhanced separation of power source between the various inverter legs, concentrated amplitude and enlarged switching frequency of torque pulsation than the traditional type inverters. The proposed system eliminates the losses and improves its reliability.

- From the proposed system the THD of output voltage is 3.54%.
- In future, by using 3D-SVM control strategy the THD level of this proposed can be reducing less than 1%.

7. References

1. Divan D, Johal H. A smarter grid for improving system reliability and asset utilization. Proceeding IEEE 5th International Power Electron, Motion Control Conference; 2006 Aug. p. 1–7.
2. Sankar AB, Seyezhai R. Development of active neutral point clamped multilevel inverter BLDC drive employing FPGA. Indian Journal of Science and Technology. 2015 Feb; 8(4):392-9.
3. Subhashini M, Latha P, Bhagyaveni MT. Comparative analysis for harmonic distortion of a solar PV fed cascaded h-bridge multilevel inverter controlled FPGA and diode clamped inverter. Indian Journal of Science and Technology. 2015 Jul; 8(16):1-8.
4. Antony ASM. Cascaded multilevel inverter of 11 levels for RL load with reduced distortion. Indian Journal of Science and Technology. 2015 Aug; 8(19):1-3.
5. Houy JMG, Rackliffe G. Advances in wind energy technologies for the context of smart grid. Proceeding IEEE. 2011 Jun; 99(6):1083–97.
6. Patel BK, Smith HS, Hewes TS, Marsh WJ. Application of phase shifting transformers for Daniel-McKnight 500 kV interconnection. IEEE Transaction on Power Delivery. 1986 Jul; 1(3):167–73.
7. Pandian G, Reddy SR. Simulation and analysis for multilevel inverter fed induction motor drive. Indian Journal of Science and Technology. 2009 Feb; 2(2):1-3.
8. Gyugyi L, Schauder CD. Static synchronous series compensator and solid-state approach to the series compensation of transmission lines. IEEE Transactions Power Delivery.1997 Apr; 12(2):406–17.
9. Gyugyi L. Unified power-flow control concept for flexible AC transmission systems. IEE Proceeding C- Generation Transmission Distributed. 1992 Jul; 139(4):323–31.
10. Gyugyi L, Schauder CD, Williams SL, Edris A. The unified power flow controller: A new approach to power transmission control. IEEE Transaction on Power Delivery. 1995 Apr; 10(2):1085–97.
11. Ghahnavieh AR, Feuillet R, Firuzabad F. UPFC for enhancing power system reliability. IEEE Transaction on Power Delivery. 2012 Oct; 25(4):2881–90.
12. Noroozian M, Angquist L, Ghandhari M, Andersson G. Use of UPFC for optimal power flow control. IEEE Transaction on Power Delivery. 1997 Oct; 12(4):1629–34.
13. Yamini K, Vasudha B, Ponnambalam P. Implementation of fuzzy logic controller for cascaded multilevel inverter with reduced number of components. Indian Journal of Science and Technology. 2015 Jan; 8(S2):240-56.
14. Sankar AB, Seyezhai R. Development of active neutral point clamped multilevel inverter fed BLDC drive employing FPGA. Indian Journal of Science and Technology. 2015 Feb; 8(4):392-9.
15. Babu AR. Comparative analysis of cascadeded multilevel inverter for phase disposition and phase shift carrier PWM for different load. Indian Journal of Science and Technology. 2015 Apr; 8(S7):251-62.
16. Sano K, Takasaki M. A transformer less D-STATCOM based on a multivoltage cascade converter requiring no DC sources. IEEE Transaction on Power Electronics. 2012 Jun; 27(6):2783–95.
17. Renz BA, Keri A, Mehraban AS, Schauder C, Stacey E, Kovalsky L, Gyugyi L, Edris A. AEP unified power flow controller performance. IEEE Transaction on Power Delivery. 1999 Oct; 14(4):1374–81.
18. Monteiro J, Silva JF, Pinto SF, Palma J. Matrix converter based unified power-flow controllers: Advanced direct power control method. IEEE Transaction on Power Delivery. 2011 Jan; 26(1):420–30.
19. Hemachandu P, Reddy VCV, Kusuma N, Reddy DM. Influence of advanced multi-carrier modulation scheme for 15-level multilevel inverter using ANFIS controller. Indian Journal of Science and Technology. 2016 Mar; 9(11):1-8.
20. Akagi H, Inoue S, Yoshii T. Control and performance of a transformer less cascade PWM STATCOM with star configuration. IEEE Transaction on Industry Applications. 2007 July-Aug; 43(4):1041–9.
21. Gultekin B, Gercek CO, Atalik T, Deniz M, Bicer N, Ermis M, Kose K N, Ermis C, Koc E, Cadirci I, Acik A, Akkaya Y, Toygar H, Bideci S. Design and implementation of a 154-kV 50-Mvar transmission STATCOM based on 21-Level cascaded multilevel converter. IEEE Transaction on Industry Applications. 2012 May-Jun; 48(3):1030–45.