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A New Model for Sample and Hold Unit of ADCs based on CC with High Bandwidth and Low Power Consumption (for Medical Applications)

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Abstract

Objectives: To present a new design based on CCII to improve ADC parameters. **Methods/Analysis:** ADCs play a vital role in implementation of electronic circuits. These circuits have different parts for which optimization can reduce power and voltage consumption and increase ADC bandwidth. **Findings:** The results showed that the suggested circuit could be implemented for certain application, such as medicine. ADC bandwidth reached an optimal level compared to other suggested designs; in the current model, ADC bandwidth was able to improve significantly. Moreover, <1mW power was used; therefore this ADC is suggested for medical applications. **Applications/Improvement:** Comparing the speed of the suggested design before and after implementation of CCII, the circuit speed was higher at current mode.

Keywords: ADC, Accuracy, Bandwidth, Current Conveyor, Power Consumption

1. Introduction

Advances in electronic components and circuits, as well as new applications required by industries have led to an increasing demand for systems with certain applications including medical applications. In the early 1980s, analog circuits were predicted to lose their effectiveness because of their advanced digital counterparts. In addition, digital signal processing algorithms became stronger continuously, while the integrated circuit(IC) technology allowed the implementation and application of these algorithms in silicon. Most goals and structures realized by analog technology were now implemented easily digitally. By increasing IC capabilities, signal processing seemed to be done digitally[1-4].

Although most signal processing technologies are digitalized, analog circuits are required for many complex, important and functional systems including natural signal processing systems such as sensors and optical cell of a video camera. Mixed-signal ICs (both analog and digital) involving tens of thousands of devices are now widely used in different applications. One of the most important applications of these circuits is medicine which requires high accuracy for survival and treatment of patients. Medical application may require various frequencies, which makes the design more difficult[4-7].

The tendency to produce smaller and lighter electronic products highlights low voltage techniques. On the other hand, the increasing growth of high frequency systems requires less expensive and smaller circuits with higher frequency. Moreover, the improved efficiency at light load is critical for extending battery life in portable applications. Currently, Analog-to-Digital Converters (ADCs) as a bridge between real-world analog quantities and digital processing world plays a key role in many electronic, communications and control systems. By increasingly high speed and accuracy of digital processors as well as the growth of portable systems which mainly operate by battery and require low-power components, the design of fast low-power converters is an important topic in the field of Ics[7-11].

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The purpose of this study is to design Sample and Hold unit of a four-bit ADC using second generation of current conveyors (CCIIs) to increase accuracy and bandwidth and reduce power. The used CCII is based on inverter CMOS operating in trans conductance mode in which low voltage operation is feasible. In the following, ADCs and CCIIs are described and the proposed circuit is evaluated.

2. Analog to Digital Converter

Ideally, an ADC maps the input continuous signal to a series of N-bit digital words, as shown in Eq. 1.

$$V_{IN} = V_{FS}\sum_{k=0}^{N-1}\frac{b_k}{2^{k+1}} + \varepsilon \quad (1)$$

where, V_{FS} is maximum input voltage, b_k represents a single output bit and ε is the quantization error. This equation can also be written based on the least significant bit (LSB).

$$V_Q = \frac{V_{FS}}{2^N} = 1LSB \quad (2)$$

$$V_{IN} = V_Q\sum_{k=0}^{N-1} b_k 2^k + \varepsilon \quad (3)$$

A single digital code includes a small range of input with 1 LSB width around the code center. The difference between input analog and the nearest equivalent analog to the code center is called quantization error. Since the number of ADC bits is limited, even an ideal ADC produces quantization error. Signal-to-quantization-noise ratio (SQNR) can be calculated directly. The error range is equal to quantum voltage (LSB). Assuming that quantization error is uniformly distributed between 0.5 LSB and 0.5 LSB within each code, the value of the voltage error is equal to Eq. 4[12,13].

$$E\{\varepsilon^2\} = \frac{1}{V_Q}\int_{-\frac{1}{2}V_Q}^{\frac{1}{2}V_Q}\varepsilon^2 d\varepsilon = \frac{1}{V_Q}\left[\frac{\varepsilon^3}{3}\right]_{-\frac{1}{2}V_Q}^{\frac{1}{2}V_Q} = \frac{V_Q}{12} \quad (4)$$

Assuming the independent noise, a maximum range input is equal to Eq. 5.

$$V_{rms} = \frac{2^N V_{FS}}{2\sqrt{2}} = \frac{2^N V_Q}{2\sqrt{2}} \quad (5)$$

QSNR is calculated by Eq. 6.

$$SNR = 20\log\left(\frac{V_{rms}}{\sqrt{E(\varepsilon^2)}}\right) = 20\log\left(2^N\sqrt{1.5}\right) = 6.02N + 1.76dB \quad (6)$$

There are different types of ADCs including flash and pipeline ADCs. Figure 1 shows the structure of these converters.

3. Current Conveyors

Current mode circuits such as CCs and operational trans conductance amplifiers play a key role in design of analog signal processing circuits. CCs provide additional advantages such as greater bandwidth, less complexity and wider voltage range over voltage mode circuits in different analog signal processing circuits. Following current mirrors, CCs are the most common analog circuit cells. CCs are preferred over op-amps for their concurrent voltage and current processing, bandwidth or gain multiplier at higher bandwidth and bandwidth-independent gain.

Recently, CCIIs are used in active filters and oscillators due to their larger signal bandwidth, linearity and wider dynamic range. CC processor is a three terminal structure, as shown in Figure 2[14-17].

The governing equations of this processor can be shown by a complex matrix as Eq. 7.

$$\begin{pmatrix} i_y \\ V_x \\ i_z \end{pmatrix} = \begin{pmatrix} o & a & o \\ c & o & o \\ o & b & o \end{pmatrix}\begin{pmatrix} V_y \\ i_x \\ V_z \end{pmatrix} \quad (7)$$

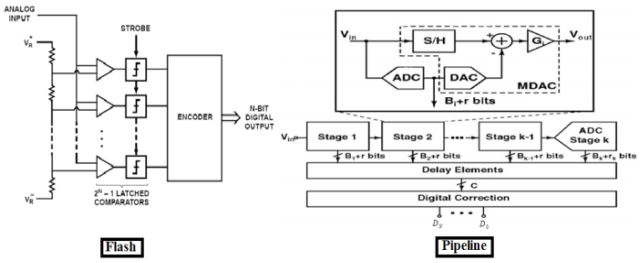

Figure 1. Flash and pipeline ADCs

Figure 2. A CC circuit[15].

where, z, y and x are input and output terminals. The parameter b represents the current flows from x to z, which is ideally equal to 1;for any b = ± 1, two types of CC can be defined (CC + and CC-). The parameter c represents the separation factor or voltage conversion, which is ideally equal to 1. Based on the parameter a, three generations can be defined for CC including CCI, CCII and CCIII. In CCI, introduced in 1968, the current flows in x and y as shown in Eq. 8.

$$a = +1 \quad , \quad i_Y = +i_X \tag{8}$$

In CCII, introduced in 1970, no current flows through the terminal y(a = 0); ideally, input impedance is infinite. In CCIII, introduced in 1995, the current is reversed in x and y(a = -1). Unlike CCI, Eq. 9 holds for CCIII.

$$I_Y = -I_X \tag{9}$$

4. Discussion

This section describes the CCII-based ADC design, its bandwidth, power consumption, etc. As noted earlier, a characteristic CCII is defined as Eq. 10 and Eq. 11.

$$V_X = V_Y \tag{10}$$

$$I_Z = I_X \tag{11}$$

The terminal x is an output in Eq. 10, while it is input in Eq. 11; this needs to be considered in the design. In any case, the terminals y and z are considered as input and output, respectively. To hold Eq. 10, two inverters in series are used (Figure 3).

In this case, the circuit analysis shows that the transistor M1 is saturated, while the transistor M2 is linear; therefore, the used structure requires two saturated transistors. Thus, two other transistors are used to supply BIOS voltage of transistors, as shown in Figure 4[18-23].

Note that the transistor with connected drain and gate acts as a diode with output resistance $\frac{1}{g_m}$. Thus, the transistors M_5 and M_6act as two resistors, modeled in Figure 5.

As shown in Figure 5, Eq.12holds for voltage of the point M using voltage divider.

$$V_M = \left(\frac{\frac{1}{g_{m5}}}{\frac{1}{g_{m5}} + \frac{1}{g_{m6}}} \right) Vdd \tag{12}$$

Since this circuit is to supply BIOS of transistors, Eq.13 holds assuming equal g_m for n- and p-type transistors.

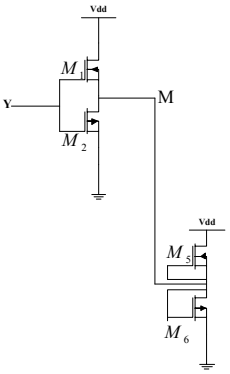

Figure 4. The used structure to supply BIOS of transistors.

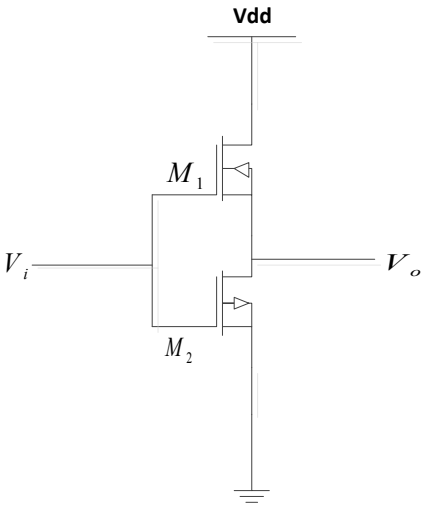

Figure 3. CC inverter circuit.

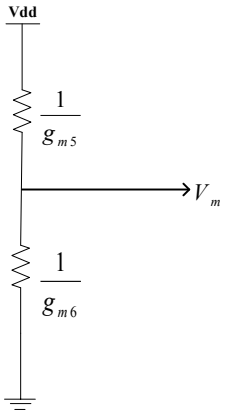

Figure 5. Equivalent circuit of the transistors M_5 and M_6.

$$V_M = \left(\frac{1}{\frac{g_{m5}}{2}} \right) Vdd = \frac{1}{2} Vdd \tag{13}$$

Moreover, g_ms are required to hold Eq. 14.

$$g_{m_n} = g_{m_p} \tag{14}$$

Considering $g_m = \frac{1}{2}\mu C_{ox}\left(\frac{w}{l}\right)$,we have:

$$\frac{1}{2}\mu_n C_{ox}\left(\frac{w}{l}\right)_n = \frac{1}{2}\mu_p C_{ox}\left(\frac{w}{l}\right)_p \tag{15}$$

Considering equal C_{ox}s, Eq.16 is derived by eliminating $\frac{1}{2}$ of both sides.

$$\mu_n \left(\frac{w}{l}\right)_n = \mu_p \left(\frac{w}{l}\right)_p \tag{16}$$

Thus:

$$\frac{\mu_n}{\mu_p} = \frac{\left(\frac{w}{l}\right)_p}{\left(\frac{w}{l}\right)_n} \tag{17}$$

For $\mu_n = 4\mu_p$, we have:

$$\frac{\left(\frac{w}{l}\right)_n}{\left(\frac{w}{l}\right)_p} = \frac{1}{4} \tag{18}$$

To see how the inverter works, a pulse is applied as an input to see the inverter output. Thus, the output is evaluated by applying the pulse to the inverter input, as shown in Figure 6.

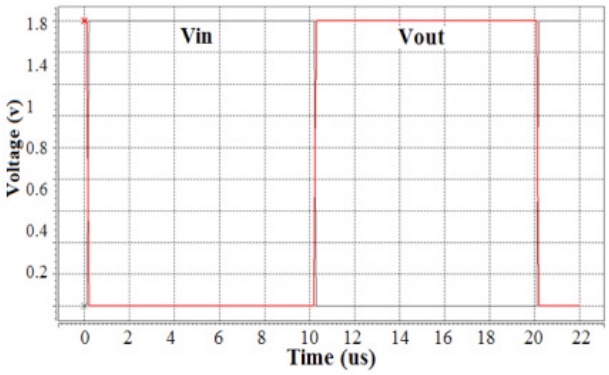

Figure 6. Output of CC inverters output for input pulse.

To see if Eq. 10 holds for CCs, the equation for Figure 4 is written as follows:

$$V_m = -(g_{m1} + g_{m2})V_y \left(\frac{1}{g_{m5}} \middle\| \frac{1}{g_{m6}} \right) \tag{19}$$

Assuming equal g_ms, we have:

$$V_m = -(2g_m)V_y \left(\frac{1}{2g_m} \right) = -V_y \tag{20}$$

where, M voltage is equal to Y voltage with a minus sign; thus, another inverter is used as shown in Figure 7.

The transistors M_5 and M_6 shown in Figure 7 are inverters. The saturated transistors M_7 and $M_8$are used to supply BIOS of above transistors. Moreover, Eq. 21 can be derived for the transistors M_3 and M_4.

$$V_x = -(g_{m3} + g_{m4})V_m \left(\frac{1}{g_{m7}} \middle\| \frac{1}{g_{m8}} \right) \tag{21}$$

Assuming equal g_ms, Eq. 22 is derived as follows.

$$V_x = -(2g_m)V_m \left(\frac{1}{2g_m} \right) = -V_m \tag{22}$$

Considering Eq. 21 and 22, we have:

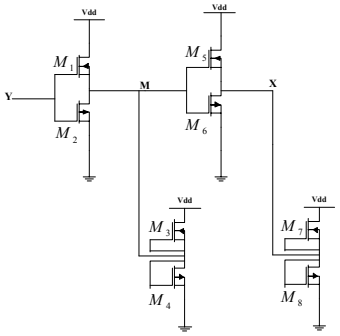

Figure 7. Inverters used in CC.

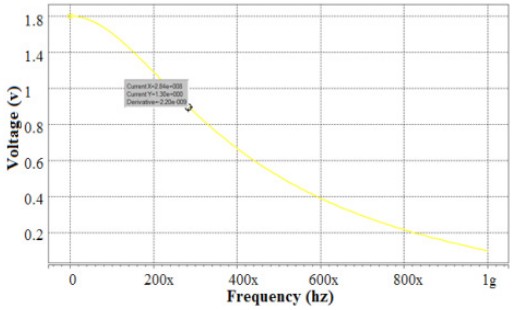

Figure 8. Bandwidth of the suggested CC.

$$\left.\begin{aligned} V_x &= -V_m \\ V_m &= -V_y \end{aligned}\right\} \rightarrow V_x = V_y \tag{23}$$

To see if the first condition holds, 1V voltage is applied to input. The output is shown in Figure 8.

As shown in Figure 8, the circuit bandwidth is reasonable. In addition, the circuit uses power as low as 700 μW. Therefore, this circuit is suggested for medical applications.

To hold Eq. 11, the transistors M_9 and $M_{12}$are used as shown in Figure 9. Given the current flowing in terminals X and Z, Eq. 11is derived.

Ideally, X voltage is equal to Y voltage; however, Eq. 24 holds given the output resistance of the terminal X.

$$V_x = V_y + I_x\left(\frac{1}{g_{m7}}\middle\|\frac{1}{g_{m8}}\right) \tag{24}$$

Eq. 25 shows the current for the terminal Z:

$$I_z = -\left(g_{m11}+g_{m12}\right)V_y + \left(g_{m9}+g_{m10}\right)\left(V_y + I_x\left(\frac{1}{g_{m7}}\middle\|\frac{1}{g_{m8}}\right)\right) \tag{25}$$

Assuming equal g_ms, Eq. 25 can be written as Eq. 26:

$$\begin{aligned} I_z &= -\left(2g_m\right)V_y + \left(2g_m\right)\left(V_y + I_x\left(\frac{1}{2g_m}\right)\right) \\ &= \left(2g_m\right)I_x\left(\frac{1}{2g_m}\right) = I_x \end{aligned} \tag{26}$$

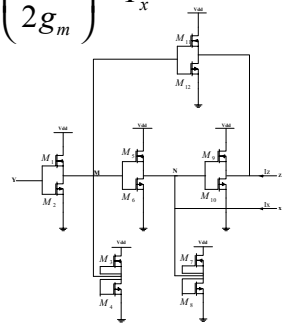

Figure 9. CC for the suggested circuit.

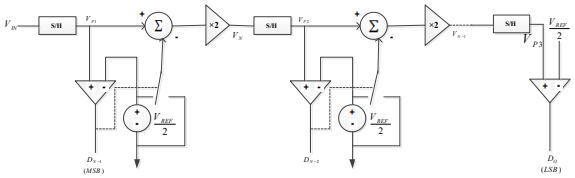

Figure 10. Pipeline ADC.

Considering Eq. (26), the second condition holds for CC. Next, sample and hold unis are designed. Figure 10 shows the pipeline ADC.

Architecture of pipeline ADC combines high operational power and input capacitor by limiting noise. Pipeline ADC is composed of N phases in series and each phase contains one bit ADC (comparator), a collector, a multiplexer etc. In order to design a sample and hold circuit, a circuit which is able to implement the algorithm shown in Figure 11 can be used.

As shown in Figure 11, the circuit contains a main input as well as a stimulating input (clock). In Figure 11,input will be converted to output if stimulation is zero (low) and it will not if the stimulation is 1 (high). Sample and hold circuit is implemented in Figure 12 using MOS transistors.

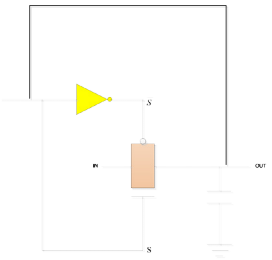

Figure 11. Sample and Hold Circuit.

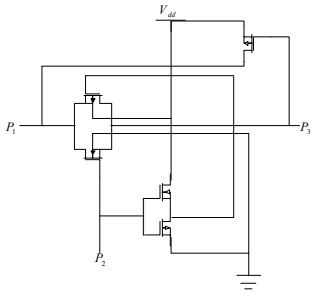

Figure 12. implementation of Sample and Hold Circuit.

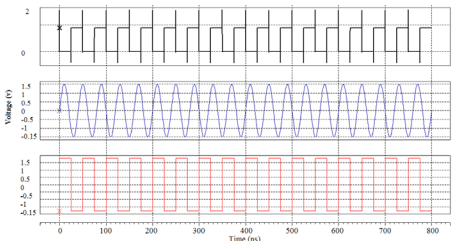

Figure 13. Output of the Sample and Hold Circuit in voltage mode.

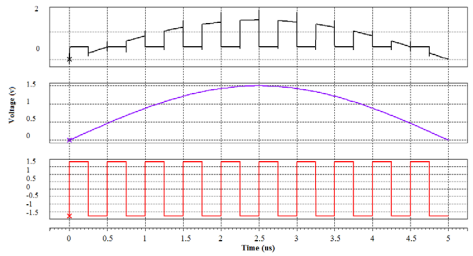

Figure 14. Output of the sample and hold circuit in current mode.

Table 1. Results of the suggested design

Characteristic	Voltage mode	*Current mode*
CC power consumption		696.0367 µW
Total power consumption of Sample and Hold Circuit	1.2824 µW	1.1447µW
CC bandwidth		1.4 G
Technology	0.18 µm	0.18µm
Source Voltage	1.8 V	1.8 V
Sampling frequency	12.5 MHz	25 MHz

Moreover, Figure 14 shows the output of the sample and hold circuit in current mode.

For better comparison, the results are summarized in Table 1.

5. Conclusion

This study designed CCs based on their governing equations using sample and hold unit of ADC. Sample and hold circuit was designed without CC and assessed by CC. The results showed that the circuit is able to shift from current mode to the voltage mode. The application determines the mode to be used; in some applications, only the current mode can be used. According to results, the suggested design can be used for current mode. In addition, the suggested design can be used in medical applications for its very low power consumption (<1 mW). Moreover, the circuit bandwidth increased to a reasonable level. By evaluating circuit speeds before and after application of CCII, the results indicated an increase in circuit speed in current mode.

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