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Low Power and High Performance 8t SRAM Cell with Double Ended Bit Line Configuration for Improved Write Operation

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Abstract

Objectives: To propose a new 8T SRAM architecture that uses two buffer transistors that help in faster discharging of bit line and boosts the cell performance by reducing its delay, power consumption and improving its write SNM. **Methods/ Statistical Analysis:** Parameters that we have taken in this design are power, delay and stability. Stability of the cell is determined with the help of static noise margin. For the simulation of the proposed and existing cell, Synopsys tool (C-Designer) and 90nm CMOS technology is used. **Findings:** We have done our analysis by varying the voltage. We have scale down the voltage from 1.8V to 0.5V. Maximum power reduction is observed in our proposed design. The power consumption of cell is significantly reduced to 0.175 µW as compared to 0.707 µW in standard 8T Static-RAM cell (keeping supply voltage as 1.2V). 8T Static-RAM cell proposed is 85% faster than the standard 8T Static-RAM. The stability of proposed Static-RAM cell is calculated using SNM. The read and write SNM values for the proposed cell is 301mV and 654mV respectively. **Application:** SRAMs have a wide range of applications for example handheld devices, portable appliances, Desktop, laptop, mobile phone etc. SRAM is used also in FPGAs and CPLDs.

Keywords: Bit Line, Low Power, Performance, SRAM, Stability

1. Introduction

CMOS devices are being scaled continuously down from past few decades so as to attain lower power consumption, higher speed and better performance[1,2]. Down scaling theory is predicted by the Moore's law which prompts to improve the features like speed, delay and density in Integrated circuits. As the size of transistor is reduced, some short channel effects come into picture[3]. It is necessary to be congruent with the operating condition of the low power IC's as supply voltage decreases. Accordingly at the same time during the increment of the parallel architecture of such a low power system, it demands high on-chip cache memory to split the data across the parallel processing system efficiently[4]. Eventually epidemic growth of device count per chip has been achieved by miniaturization of the semiconductor memories. They have become a key component if digital system design and SOC applications are considered. SRAM (Static Random Access Memory) envisages the universal memory option for CMOS ICs. In nutshell, the energy which is consumed by the SRAM improves by scaling down the voltage supply which also reduces its leakage power significantly[5]. However to achieve memory cell with low power and less area, researchers have focused on new materials like silicon-germanium, high K-dielectrics in its design and experimented with high performance devices like FDSOI, FINFET, junction less FETs etc[5,6]. Integrating more

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memory on chip gives successful intends to utilize silicon as a result of memory's reduced power density, regularity in layout design and power profits by diminished off-chip transfer speed[7].

In contrast with DRAM, SRAM occupy less area and has low power dissipation. DRAM requires the refresh logic so it has higher power dissipation but in SRAM, data is stored statically so no refresh logic is required. Wearable gadgets, compact medical equipment and other military equipment are some applications which need to store a large amount of data and long working time from battery power. So SRAM gives huge advantages in such fields in terms of speed, density and power[8].

Static cell is back to back connected inverter design that stores the state as voltage differential[9]. It is also known as the basic cache cell. To perform the read and write operation in the cell, access transistors are used. It consists pull up and pull down transistors which helps to perform successful read and write operation. The storage nodes named as Q and QB stores the data which is compliment to each other. The basic SRAM cell architecture consist of memory cell array, sensing and write circuit, row and address decoder, column or bit address decoder and control unit. This decoder helps to address the particular memory cell in memory bank. In some SRAM architectures different read and write circuitry is used to perform the desired operation[10].

The performances of 6-T SRAM bit cell degraded at deep submicron technology so the researchers are focused on to propose a still better architecture of SRAM bit cell which has low power dissipation and high speed although they have proposed such architecture[11]. We are also proposing a new SRAM bit cell architecture which is much better than the previously proposed architecture in terms of speed and power. In this research paper, a brief study and design of traditional SRAM cells such as standard 6-T Static cell, Standard 8-T bit cell, 9-T Static cell and proposed 8-T SRAM bit cell are presented and simulated. The variation in parameters namely power, delay and static noise margin (SNM) are analyzed. We have presented a new 8-T Static cell using two buffer transistors that boosts the overall performance of the circuit over the existing SRAM bit cells.

The excess of the research paper is divided into five sections. Section 2 illustrates the operation of existing Static-RAM cell & proposed 8-T Static-RAM cell design and also discusses the pros and cons of these designs. Section 3 describes the SNM analysis of SRAM cell. Simulation results and performance evaluation is addressed in Section 4 and conclusion of the paper is presented in Section 5.

2. Various Architectures of SRAM cells

Read stability is one of the major issues in the standard 6-T SRAM cell. To overcome this issue, several architectures are proposed with additional circuitry. The read and write operation are made totally separated from each other by including two transistors in a 8-T bit cell as the information from the nodes are detected through the separate bit line which is named as RBL (read bit line). Thus for the write task the remaining cell segment of the 6-T bit cell is make advanced, bringing about a general lower supply voltage. However, a lots of benefits contrast with conventional 6T bit cell design have been suggested of different cell topologies. These SRAM's can be classified as single ended SRAM cells. In this section we have briefly summarize the several existing architectures of SRAM cells.

2.1 6T Static-RAM Bit Cell

In standard 6T Static-RAM bit cell as shown in Figure 1, while analysis of read operation BL, BLB & WL is gripped to V_{dd} and one of the bit line is discharged by memory cell in accordance to the data stored in the storage node. A logic level output converted from differential signal through a sense amplifier. When the read cycle is completed these bitlines get again precharge for next read cycle. In the duration of write operation depends upon the required data, BL's are gripped to either V_{dd} or ground and WL is need to be raised. To perform the sufficient write operation, the strength of pass gate transistor to pull up transistor is too strong[12]. Likewise in the duration of hold WL is kept low by connect to ground and the BLs are left floating. For successful read and write operation, pull up ratio and cell ratio are taken in the ratio of 1.5. Table 1 reveals the width (w) of transistors. As the technology node is 90nm so the length of the transistors are 100nm which is the minimum length of transistor that can be accepted by the 90nm CMOS technology node.

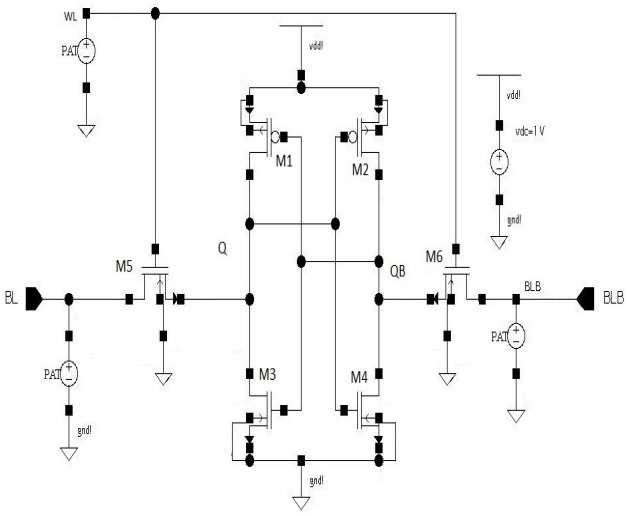

Figure 1. Schematic of 6-T SRAM cell.

Table 1. Transistor width of Different SRAM cell

Transistor	6-T SRAM cell	Standard 8-T SRAM cell	9-T SRAM cell	Proposed 8-T SRAM cell
M1	0.45 µm	0.12 µm	0.12 µm	0.12 µm
M2	0.45 µm	0.12 µm	0.12 µm	0.12 µm
M3	0.45 µm	0.12 µm	0.12 µm	0.18 µm
M4	0.45 µm	0.12 µm	0.12 µm	0.18 µm
M5	0.3 µm	0.6 µm	0.6 µm	0.6 µm
M6	0.3 µm	0.24 µm	0.6 µm	0.6 µm
M7	-	0.45 µm	0.24 µm	0.45 µm
M8	-	0.45 µm	0.24 µm	0.45 µm
M9	-	-	0.48 µm	

2.2 8T Static-RAM Cell

In the architecture of 8T Static-RAM bit cell current path of read and write operation is separated by using three additional transistors which evade the accidental spin of bit cell data while read task is performed[13]. This leads to considerably oversize SNM throughout read operation. This cell structure contains single bit line operation and a separate RBL is introduced for read task. As compare to double bit line, single bit line Static-RAM bit cell has larger RSNM[13].

2.2.1 Read Operation

In 8-T SRAM bit cell read task is execute by take advantage of M6, M7 and M8 transistors as demonstrated in Figure 2. It is recommended to make bit line precharged and then word line is raised for fruitful read operation. The gate terminals of read circuitry transistors M7 & M8 are associated with storage node terminal QB. By utilizing the read bit line, when the transistor M6 is on, current will start streaming through the read circuitry. To pursue the cell information a sense amplifier is utilize which detect the bit line voltage vacillation. Input voltage contrast is sensed by this amplifier and converted into logic level output. For read operation of logic '1', assume storage node Q and QB stores logic '1' & '0' respectively which turns ON the PMOS transistor M8 which results in charging of bit line through transistor M6 & M8. Bit swing is observed by the sense amplifier and logic '1' is acquired. At the time of read operation of logic'0', storage node QB stores logic '1' and RBL turns ON M7 & M6 transistor respectively. Thus through M6 and M7 bit line get discharged and voltage variation is sensed by sense amplifier, a result in logic'0' is acquired at the output.

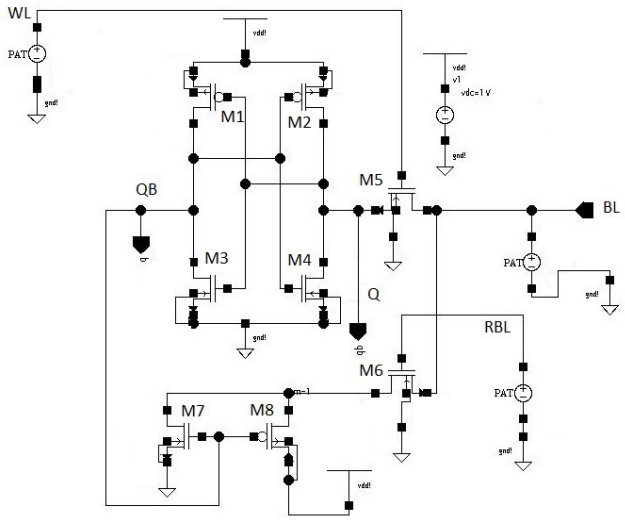

Figure 2. Schematic of 8-T SRAM cell.

2.2.2 Write Operation

To perform write operation in 8-T SRAM bit cell structure just single bit line is utilized when contrasted with standard 6-T Static-RAM cell as appeared in Figure 2. At the time of write operation of logic '1' transistor M5 turns ON when WL is empowered. BL is charged to V_{dd} i.e. logic '1' and the storage node Q will charge through the transistor M5. As the node Q will charged it will turn ON the transistor M3 and turned OFF the M1 transistor which prompt to toss node QB to logic '0'. Now QB

node helps to empowering the node Q by turning on the transistor M2 and turn off the transistor M4. Then again at the time of write logic '0' operation, BL is connecting to ground in order to charge to logic '0' and transistor M5 is kept ON by making WL high. The storage node Q starts releasing its stored charge and turn ON transistor M1 and turns OFF the transistor M3. Now the node QB will starts charging through transistor M1 and Q node start discharging through M4. Therefore logic '0' is acquired at storage node Q.

At the output of sense amplifier, bit cell storage node with logic '0' can produce a false '1' due to the single ended technique. To detect the potential difference, the voltage difference between BL with logic '0' and bit line BL with logic'1' won't defeat the counterbalance of the related sense amplifier. This issue can be intensifies in circuits by making variation in timings.

2.3 9T SRAM Cell

In 9-T SRAM bit cell, three extra transistors with high threshold voltage are employed in standard 6-T bit cell, to bypass read-current from the storage nodes, as depicts in Figure 3. A 9T Static-RAM cell is used for concurrently diminish the leakage power and build up data stability. At the time of execution of read operation, the stored data from the nodes Q and QB is detached from the BL's. Static read noise margin obtained during read task of the used circuit is augmented a contrast to 6T standard SRAM cell. The leakage power consumption is reduced by this 9-T SRAM bit cell as this idle cell placed under super suspended sleep mode. The architecture of 9-T SRAM bit cell is depicts in Figure 3. In Static-RAM cell discontinue power supply circuit leads to loss of stored data and it is intensely mandatory to keep the cell on also in the idle state. This creates a challenge of reducing the leakage power or power consumption while cell in the standby mode. To bring under control the above mentioned limitation read task is executed in the different manner in the 9-T SRAM cell. This helps to proscribe the data corruption of the cell by quarantine the data from external read circuitry. In this research the storage node Q and QB is connected with transistor M7 & M8 respectively as depicts in Figure 3. The leakage of energy might increase as it uses the highest number of transistor. The transistor M7 and M8 are of high threshold voltage which helps to reduce the leakage current. Transistors with low threshold voltage are used for the access transistor which helps to decrease the write delay. The design of cell is such that it works with lower power supply and reduces the leakage power consumption which makes the cell more efficient.

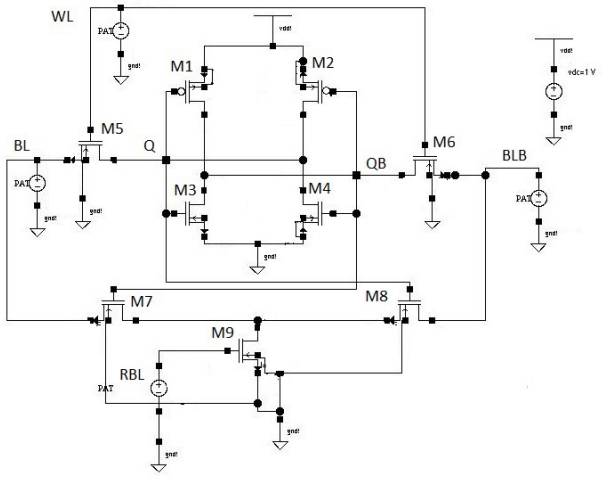

Figure 3. Schematic of 9-T SRAM cell.

2.4 Proposed 8-T SRAM cell

Suggested SRAM cell design is resemble with the standard 6-T SRAM cell. By adopting the appropriate width of transistors, performance and density of the cell is achieved. The schematic diagram of proposed 8-T Static-RAM cell is depicts in Figure 4.

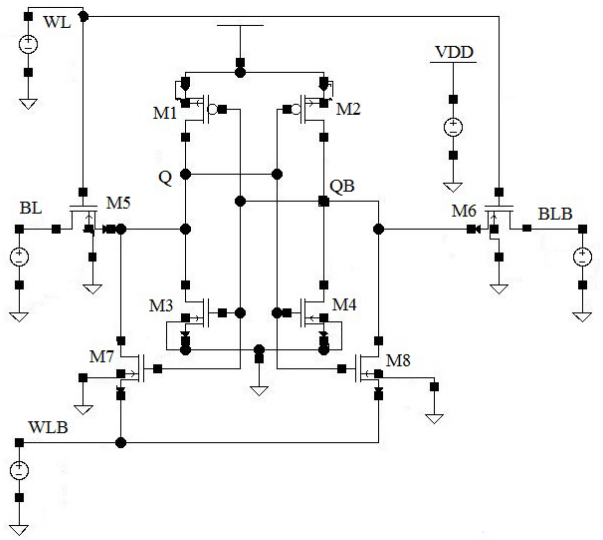

Figure 4. Schematic of proposed 8-T SRAM cell.

2.4.1 Read Operation

The read task of suggested architecture is execute by pre-charging the both BL and BLB of SRAM cell to logic '1', then V_{dd} and ground supply is provide to WL& WLB respectively as the WL and WLB are compliment to each other. Depends upon the logic store in the capacity nodes Q and QB, one of the buffer transistors M7 or M8 will start conducting. Bit lines BL and BLB releases through access transistor M5 & M6, trailed by two paths i.e. one through buffer transistor M7 or M8 and WLB and other through pull down transistor M3 or M4. This outcome in quicker read operation. Case in point, if capacity node Q stores logic '1' then pull-down transistor M4 and support transistor M8 will starts conduct. In consequence of these two discharging path, BLB will discharge speedily through the transistor M6 & M4 and along the path M6, M8 & WLB, at the same time BL is gripped to VDD as M3 and M7 are OFF (because of logic "0" put away at storage node QB). The sense amplifier is utilize to decode the stored information by detecting the potential distinction amongst BL and BLB.

2.4.2 Write Operation

WL is connected to VDD at the time write operation. Accordingly, the correlative of WL (i.e. WLB) is connected to ground. As a result of high WL, both the entrance transistors (M5/M6) are ON. Now consider that logic '1' and '0' is acquired by node Q & QB respectively. Now to perform logic '0' operation at storage node Q, charge the BL and BLB to logic '0' and logic '1' respectively. This results in discharging of storage node Q by bit line BL through transistor M5. At the same time storage node QB starts charging through transistor M6 using BLB. Initially the storage node QB releases its charge through transistor M4 to ground and M8 through WLB however in the final time storage node Q starts releases its stored charge through M3 to ground and M7 through WLB. Hence, the appropriate logic is written accurately.

3. SNM Analysis

The butterfly curve helps to determine the stability of any SRAM bit cell[14]. Through the voltage transfer characteristics (VTCs) of inverter pair framed by PMOS and NMOS transistors butterfly curve is obtained. In standard 6-T SRAM bit cell, inverter pair is framed by using NMOS transistor (M3, M5), PMOS (M1) and NMOS transistor (M4, M6), PMOS (M2) separately. On the same set of axis, the input and output relation from node Q to QB and from QB to Q node are plotted by expecting that BL and BLB are operated by DC voltage source individually. Thus it is also called as DC characteristics of the cell. At the time of read or hold, bistability of the cell is demonstrated by three crossing points as shown in Figure 5. But there is only one crossing point at the time of write task, so that the cell will forcefully charged to either logic '0' or logic '1', as set by the BL extremity.

The largest square formed in the inner lobe of butterfly curve helps to determine the static noise margin of SRAM bit cell. To measure the stability of read and write task of cell, a separate RSNM & WSNM named as read static noise margin and write static noise margin respectively is calculated.

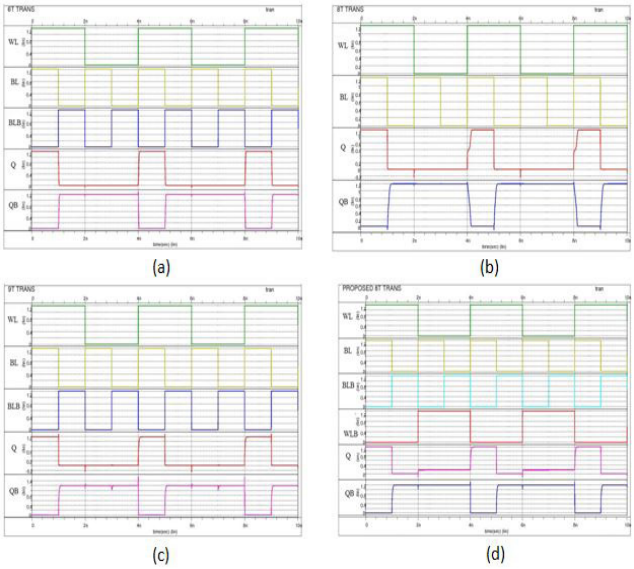

Figure 5. Transient response of a) 6-T SRAM cell b) 8-T SRAM cell c) 9-T SRAM cell d) Proposed 8-T SRAM cell.

3.1 Read Stability

RSNM helps to estimate the read stability of Static-RAM bit cell[14]. Static-RAM bit cell is more prone to noise at the time of read task due to voltage divider between two access transistor connected with bit lines and driver transistors. Because both transistors are turned on thus the node with logic '0' is charged to some extent. Bit Cell proportion (β_{ratio}, characterized as $\beta_{ratio} = \beta_{driver}/\beta_{access}$) provides a estimation about by how much amount of voltage, node having '0' logic is rises while the read task is performed. High driver resistance is inferred by smaller

cell proportion which results a little noise voltage at the capacity node '0', would be adequate to alter the stored data. Accordingly, RSNM of any bit cell is more significant than hold SNM of bit cell[15]. The estimation of static noise margin is calculated graphically by evaluating the length of largest square which is recorded inside the littler flap of the butterfly curve. The proposed 8-T SRAM bit cell demonstrates change in RSNM contrasted with conventional 6-T,8-T & 9-T cell (Figure 2). This change in RSNM is seen because of an additional path to discharge the voltage, created at nodestorage'0'.

3.2 Write-Ability

WSNM helps to estimate the write noise margin of any Static-RAM bit cell. It helps to measure the minimum static voltage that can be tolerate by the SRAM bit cell to reduce the voltage level up in high storage node to lower than threshold voltage of transistor placed in other inverter with the goal that bit cell substance can be stumbled effectively. If the cell has high WSNM then it is easier to perform a write task in the cell. WSNM of proposed 8-T SRAM bit cell and different cells are assessed similarly as done in[16].

4. Simulation Results

The results of simulation are presented in Figure 5. It indicates the variations in parameters which are associated with power dissipation and delay. The performance of the suggested 8T Static-RAM cell is contrasted with existing standard 6-T, 8T and 9T SRAM cell architectures. All the simulations have been performed using Synopsys (custom designer) EDA Tool with 90nm CMOS technology. The transient response and static noise margin (SNM) of various SRAM cells are studied and designed.

Figure 5(a) signifies the transient response of traditional 6T Static-RAM cell at 1.2v supply voltage. Write and hold of data is shown by these transient waves.

Figure 5(b) illustrates the transient response of standard 8T cell at 1.2V. The function of cell is depicts in Figure 2. Delay of the cell is increased as the data is writing only through one bit line and the power dissipation is increases as compare to standard 6T cell.

Figure 5(c) shows the transient response of 9T SRAM cell at 1.2V supply voltage. This circuit delivers better static noise margin as compare to other standard SRAM cells but it comprises of significant number of transistors so large area is required and large power is dissipated.

Figure 5(d) shows the transient response of suggested 8T Static-RAM cell at 1.2V supply voltage. The operation of proposed cell is shown in Figure 4. It shows less power dissipation and high performance.

Variation in power and delay is shown in Figure 6. From this bar graph it can be seen that at what level power and delay is reduced in proposed Static-RAM cell.

Table 2 summarized the overall performance comparison of standard SRAM cells with proposed 8-T bit cell at 1.2V supply voltage. The power dissipation of proposed cell is decreased as contrast with the traditional SRAM cells .SNM plot is additionally great when contrasted with traditional SRAM cells. This demonstrates the better execution and predominance of the circuit.

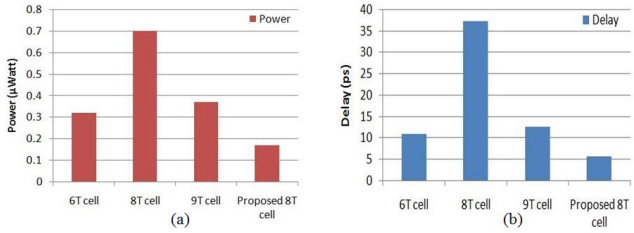

Figure 6. a) Comparison of Power dissipation of respective SRAM cells at 1.2 V b) Comparison of Delay of respective SRAM cells at 1.2 V.

Table 2. Comparison Table

Parameter	6T cell	8T cell	9T cell	Proposed 8T cell
Technology	90nm	90nm	90nm	90nm
Supply voltage	1.2V	1.2V	1.2V	1.2V
Temperature	25°C	25°C	25°C	25°C
Delay(p sec)	10.8	37.2	12.6	5.58
Power(µWatt)	0.32	0.24	0.37	0.17
RSNM (mV)	196	390	390	301
WSNM (mV)	397	172	630	654

4.1 Power and Delay Analysis

The power dissipation of Static-RAM cell mainly subjected to the supply voltage, aspect ratio of transistors (W/L), capacitance and the transistor threshold voltage. The key method used to significantly reduce the power dissipation is supply voltage scaling. We carried out supply voltage scaling for different Static-RAM cell and the observations are plotted as depicts in Figure 6.

The power dissipation is reduced by lowering the supply voltage as the dynamic power is directly proportional to the square of supply voltage. The results of proposed 8T SRAM cell as summarized in Table 3&4 are found to be quite better than the traditional designs.

The voltage scaling in supply voltage makes a huge effect on the speed of the SRAM cell. These observations are depicts in Figure 7. As we increase the supply voltage, delay in the SRAM cell is also decreases but it increase the power dissipation as shown in Figure8.

Table 3 describes by what values delay in the SRAM cell is varies in according to the supply voltage. Figure 8 describes the effect of power supply on speed of the Static-RAM cell. Power dissipation in proposed 8T SRAM cell is reduced by 46%, 29% and 53% when contrasted with standard 6T cell, 8T cell and 9T cell respectively.

Delay in Proposed 8T SRAM cell is reduced by 48%, 85% and 55% when contrasted with standard 6-T cell, 8-T cell and 9-T cell respectively.

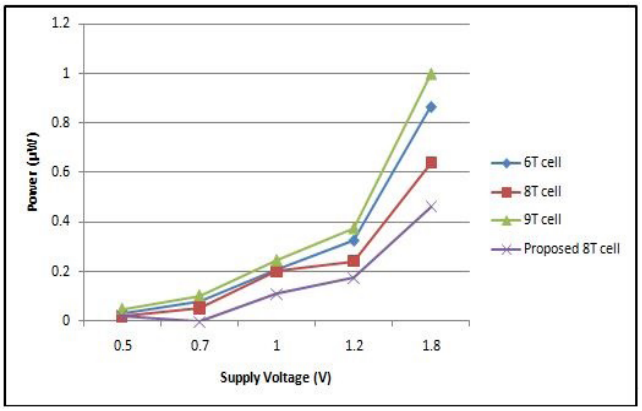

Figure 7. Power dissipation versus supply voltage curve for various SRAM cell.

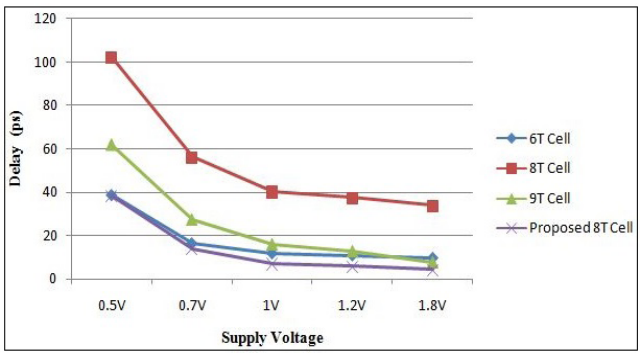

Figure 8. Delay versus supply voltage curve for various SRAM cell.

Table 3. Variation in Power dissipation with supply voltage scaling at 90nm using CMOS Technology

Supply Voltage (V)	6T cell	8T cell	9T cell	Proposed 8T cell
0.5	0.032 µWatt	0.021 µWatt	0.049 µWatt	0.022 µWatt
0.7	0.081 µWatt	0.055 µWatt	0.103 µWatt	0.045 µWatt
1	0.208 µWatt	0.201 µWatt	0.245 µWatt	0.11 µWatt
1.2	0.328 µWatt	0.243 µWatt	0.375 µWatt	0.175 µWatt
1.8	0.867 µWatt	0.637 µWatt	0.999 µWatt	0.461 µWatt

Table 4. Variation in Delay with supply voltage scaling at 90nm using CMOS technology

Supply Voltage (V)	6T cell	8T cell	9T cell	Proposed 8T cell
0.5	38.7 ps	102 ps	61.8 ps	38.1 ps
0.7	16.3 ps	56 ps	27.2 ps	13.8 ps
1	11.7 ps	40.2 ps	15.8 ps	6.9 ps
1.2	10.8 ps	37.2 ps	12.6 ps	5.58 ps
1.8	9.54 ps	33.8 ps	7.47 ps	4.17 ps

4.2 RSNM plot (Read Static Noise Margin)

Due to increase in bitline leakage, the RSNM of standard 6-T cell is decreases as depicts in Figure 9(a). Thus this cell is more prone to noise.

Figure 9(b) shows the read noise margin of the standard 8-T SRAM cell. The RSNM of this cell is much better as compare to standard 6-T cell because of the usage of separate read circuitry for read operation.

Figure 9(c) shows the read noise margin of the 9-T SRAM bit cell which is quite similar with the standard 8-T bit cell as both these cells use additional read circuitry for their operation.

Figure 9(d) shows the read noise margin of the proposed 8-T SRAM bit cell. The cell structure is quite similar with the 6-T bit cell but has the improved read SNM.

4.3 WSNM plot (Write Static Noise Margin)

Figure 10(a) reveals the write static noise margin of the standard 6-T SRAM bit cell which is quit optimum for write operation due to its pull up ratio.

Figure 10(b) shows the write noise margin of the standard 8-T SRAM bit cell. In this cell for write operation single bit line is used hence reduce in write static noise margin. Thus this cell is more prone to noise.

Figure 10(c) shows the write static noise margin of the 9-T SRAM bit cell. This cell shows the better noise margin as compare to other cell.

Figure 10(d) shows the write static noise margin of the suggested 8-T SRAM bit cell. With use of accurate transistor sizing and double bit line, the WSNM of cell is enhanced as compare to standard 8-T bit cell.

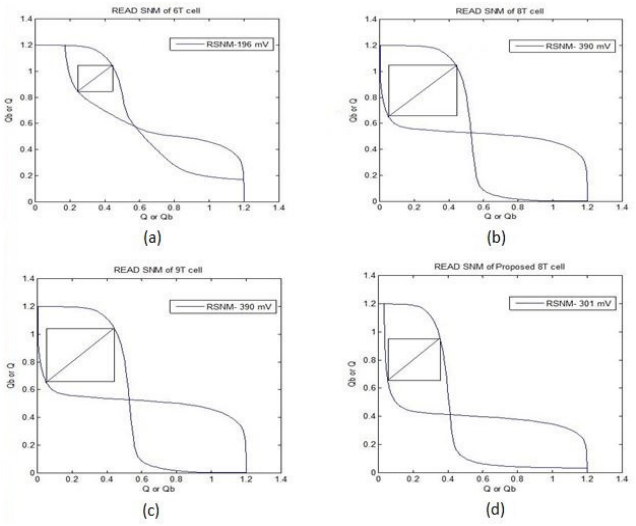

Figure 9. a) RSNM of 6T cell b) RSNM of 8T cell c) RSNM of 9T cell d) RSNM of proposed 8T cell.

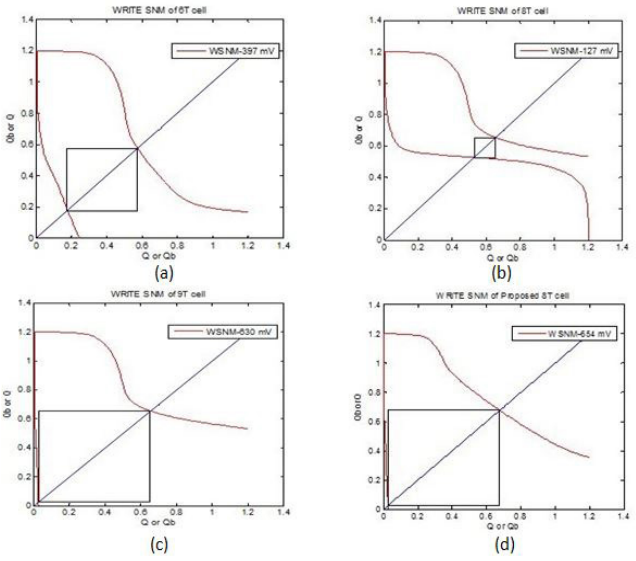

Figure 10. a) WSNM of 6T cell b) WSNM of 8T cell c) WSNM of 9T cell d) WSNM of proposed 8T cell.

5. Conclusion and Future Scope

In this research paper, a complete analysis of power, delay and static noise margin (SNM) of various Static-RAM cells is presented. Different categories of existing architectures of SRAM cells have been examined and on the basis of the results of existing architectures of SRAM cell, a different Static-RAM cell with eight transistors is proposed. Simulation results using Synopsys tool with 90nm CMOS technology verify that the power dissipation of the suggested cell is reduced to significant level in comparison with the traditional SRAM cells are shown in Figure 11. The proposed SRAM circuit has reduced the power dissipation by 29% as compare to existing single ended 8-T cell.

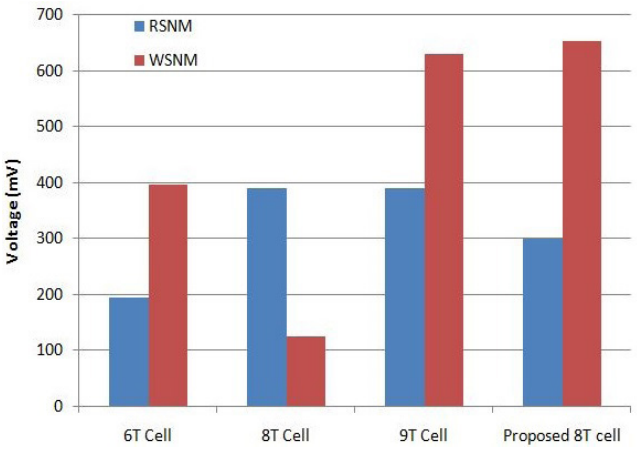

Figure 11. Comparison of WSNM & RSNM of different SRAM bit cell.

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