

# Robustness Study and Comparison between P-channel and N-channel Input Single-stage OTA

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## Abstract

**Objectives:** This paper carries out robustness study on p-channel and n-channel input differential amplifier (which is also known as single-stage operational transconductance amplifier). **Methods and Analysis:** The impact of Process, Voltage and Temperature (PVT) variations on the design metrics of both differential amplifiers is studied and suitable conclusions are drawn. **Findings:** The n-channel input differential amplifier is found to be more robust than p-channel input differential amplifier. Moreover, it provides higher gain, and 3-dB bandwidth as compared to its p-channel counterpart. All the results were obtained from extensive simulation using Virtuoso Analog Design Environment of Cadence @ 45-nm technology node. **Application:** Operational Transconductance Amplifier (OTA) can be used in the design of simple amplifiers with voltage-controllable gain and to the design of first-order and second-order active filters with controllable gains and controllable critical frequencies.

**Keywords:** Differential Amplifier, PVT Variation, Robustness, Single-stage OTA

## 1. Introduction

Advances in CMOS technology has allowed for continuing Moore's law<sup>1</sup>. Since the introduction of CMOS technology, it has been possible to achieve lower power dissipation, higher speed of operation, higher density of integration. These have been possible due to down-scaling of the transistor dimensions. However, Process, Voltage and Temperature (PVT) variations are the major problems in designing reliable and robust analog circuits<sup>2,3</sup>. Exhaustive down-scaling of device dimensions has made all types of circuits sensitive to PVT variations. Digital circuits by their nature are more robust due to higher noise margin, whereas analog circuits are prone to PVT variations. Hence they need in-depth analysis of their design metrics against PVT variations.

Process variations are classified into global (inter-die) and local (intra-die) variations. The global variation refers to fluctuation for identical MOSFETs isolated at larger distance or fabricated at different interval of time. Wafer-to-wafer, die-to-die, and lot-to-lot variations come

under global category. Conversely, in local variations (also known as mismatch or random uncorrelated variations) each transistor is affected differently. The local variation is termed as the parametric variation of identical MOSFETs across a short distance. In other words, variations are distinguished by their spatial correlation distance. For local variations there is no correlation, whereas for global variations the correlation distance is very large. Normally, the local variability is within a die and the global variability is from die-to-die, wafer-to-wafer, and lot-to-lot. Local variability can further be of two types: systematic and random variability<sup>4-12</sup>.

Differential amplifier is one of the most important building blocks of an OTA. Differential amplifier forms a differential-transconductance stage or input stage of an OTA. It sometimes provides the differential to single-ended conversion. Normally, a good portion of the overall gain of an OTA is provided by the differential-input stage, which improves noise and offset performance. The first stage of an OTA consists of a source-coupled differential pair converting the differential input voltage to

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differential currents. Generally, these differential currents are applied to a current-mirror load recovering the differential voltage. The differential pair and current-mirror load combined together is nothing more than the differential voltage amplifier<sup>13</sup>. The first (or input) stage of an OTA provides high input impedance in addition to gain in order to avoid loss of signal level when the amplifier is fed from a high impedance source. The differential input amplifier stage also provides large common mode rejection. Therefore, differential amplifier is also considered as single stage OTA<sup>14</sup>.

Whether it is a single-stage OTA or double-stage OTA or multi-stage voltage operational amplifier, it is an integral part of all these kind of amplifiers. And hence it has an important role in designing analog amplifiers and comparators. Therefore, this paper carries out an in-depth analysis of its design metrics such as gain. Since analog circuit design using aggressively scaled devices in the presence of PVT variations is a critical issue, this paper performs temperature sensitivity analysis of its gain. It also performs comparison of its design metrics between n-channel input CMOS differential amplifier with a p-channel input CMOS differential amplifier.

The remainder of this paper is organized as follows. Section 2 presents a brief discussion on basics of differential amplifier. Section 3 reports device dimension sizing for this analysis. Section 4 illustrates and compares simulation results. Finally, the conclusion of the paper appears in Section 5.

## 2. Basics of Differential Amplifier

The objective of the differential amplifier is to amplify only the difference between two different potentials irrespective of the common-mode value. Thus, a differential amplifier can be exemplified by its common-mode rejection ratio (CMRR), which is the ratio of the magnitude of the differential gain to the common-mode gain. An ideal differential amplifier will have a zero value of common-mode gain, and therefore an infinite CMRR. In addition, the input common-mode range (ICMR) suggests over what range of common-mode voltages the differential amplifier continues to sense and amplify the different signal with the same gain<sup>15-17</sup>.

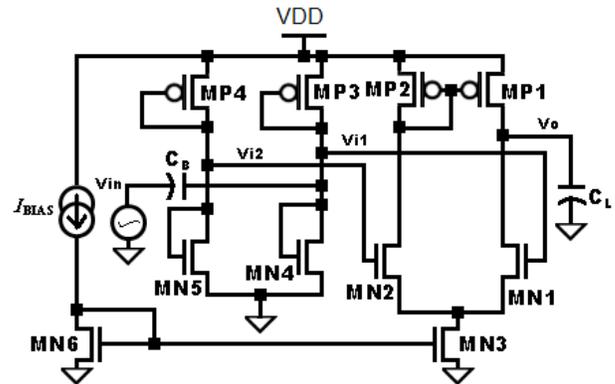
Configurations which interest us for analysis in this work are p-channel input and n-channel input differential amplifiers that use current mirror loads. Circuit-level models of the n-channel input CMOS differential amplifier

and p-channel input CMOS differential amplifier are shown in Figures 1 and 2, respectively.

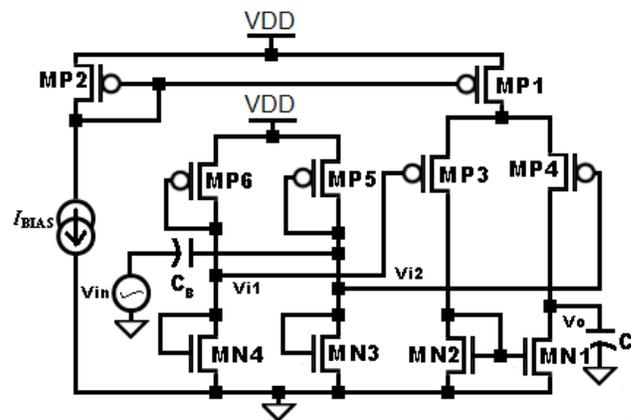
Under quiescent conditions (no applied differential signal, i.e.,  $V_{id}=0$  V) the two currents in MN1 and MN2 are equal and their sum is equal to  $I_{SS}$ , the current in the current sink, MN3 in n-channel differential pair (see Figure. 1).

$$I_{SS} = I_{D(MN1)} + I_{D(MN2)}. \tag{1}$$

The current through MN1 ( $I_{D(MN1)}$ ) determines the current through MP2 ( $I_{D(MP2)}$ ). Ideally, this current is mirrored in MP1. If gate voltages ( $V_{gs1}$  and  $V_{gs2}$ ) across MN1 and MN2 are equal and matched, then the currents in MN1 and MN2 are same (if MN2 is also operated in saturation region). Thus, the current that MP1 sources to MN2 is equal to the current that MN2 requires, causing output current to be zero, provided that the load is negligible<sup>18</sup>.



**Figure 1.** An n-channel input CMOS differential amplifier with current mirror load and diode-connected MOS active voltage divider.



**Figure 2.** A p-channel input CMOS differential amplifier with current mirror load and diode-connected MOS active voltage divider.

Due to any reason if gate voltage of MN1 increases compared to that of MN2,  $I_{D(MN1)}$  increases. This leads to increase in  $I_{D(MP2)}$ , which is mirrored to MP1. This implies that  $I_{D(MP1)}$  increases with increase in  $I_{D(MN1)}$ . However, MN2 cannot pass increased  $I_{D(MP1)}$  since there is no change in its gate voltage. Hence, the difference between the increased  $I_{D(MP1)}$  and  $I_{D(MN2)}$  flows out through output node, giving rise to a positive  $I_{OUT}$  that charges  $C_L$  up. If gate voltage of MN2 increases (due to any reason) compared to that of MN1,  $I_{D(MN2)}$  increases.  $I_{D(MP1)}$  is now not enough to fulfill the current requirement of MN2. Hence  $C_L$  charges down to meet that requirement. Hence voltage drops. Similar explanation is applicable for p-channel input differential pair.

### 3. Device Sizing

For obtaining maximum output voltage swing, the dc bias point was set to  $\sim V_{DD}/2$  at the output node.  $I_{BIAS}$  was selected to be  $20.67 \mu A$ , which resulted in a gate voltage of  $\sim V_{DD}/2$  for MN1 and MN2. Device sizing is a critical piece of our design strategy. We sized devices with such values that the gate voltage of all PMOS devices made them to operate in saturation region. In both types of differential amplifier or single stage OTA, we used channel width of  $2.7 \mu A$  and channel length of  $180 \text{ nm}$  with load capacitor of  $100 \text{ fF}$ . All the devices could be operated in saturation region due to appropriate dimensioning of devices and selection of  $I_{BIAS}$  [19].

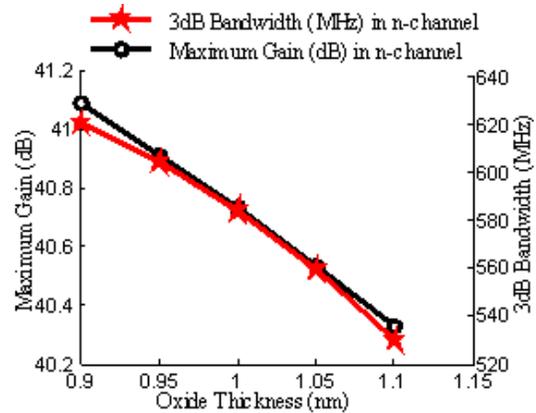
### 4. Simulation Results and Discussion

This section presents simulation results and discusses impact of process, voltage and temperature variations on an n-channel input CMOS differential amplifier and a p-channel input CMOS differential amplifier. All the estimations are carried out at  $27^\circ \text{C}$ .

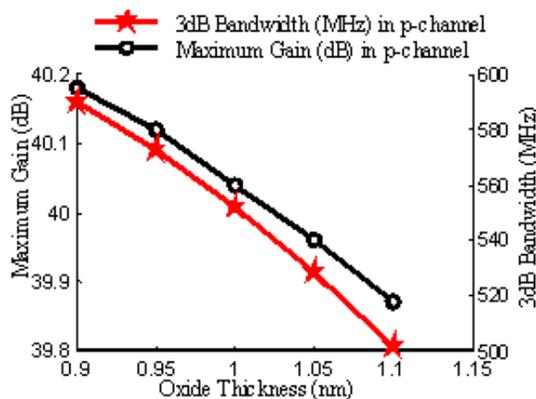
#### 4.1 Impact of Variation in Gate Oxide Thickness ( $t_{OX}$ ) on Differential Gain

The impact of oxide thickness on differential gain of both p-channel input and n-channel input differential amplifiers is shown in Figures 3 and 4.

The nominal oxide thickness is  $1 \text{ nm}$ , which is varied from  $0.90 \text{ nm}$  to  $1.10 \text{ nm}$  ( $\pm 10\%$  variations) to observe variations in differential gain ( $A_V$ ) and  $3 \text{ dB}$  bandwidth of both the amplifiers considered in this analysis and the simulation results are noted. As can be seen, the maximum gain  $A_V$  as well as  $3 \text{ dB}$  bandwidth depicts a negative



**Figure 3.** Variation in maximum (in 20 dB) gain and 3 dB bandwidth of n-channel input differential amplifier due to variation in oxide thickness.



**Figure 4.** Variation in maximum (in 20 dB) gain and 3 dB bandwidth of p-channel input differential amplifier due to variation in oxide thickness.

dependence on oxide thickness for both n-channel and p-channel input differential amplifiers.

An n-channel input differential amplifier exhibits variation in maximum gain (in 20 dB) from  $41.09 \text{ dB}$  to  $40.53 \text{ dB}$  and variation in  $3 \text{ dB}$  bandwidth from  $620.18 \text{ MHz}$  to  $530.03 \text{ MHz}$  when  $t_{OX}$  is varied from  $0.90 \text{ nm}$  to  $1.10 \text{ nm}$  whereas p-channel input differential amplifier shows a variation in maximum gain (in 20 dB) from  $40.18 \text{ dB}$  to  $39.87 \text{ dB}$  and variation in  $3 \text{ dB}$  bandwidth from  $589.91 \text{ MHz}$  to  $501.22 \text{ MHz}$  when  $t_{OX}$  varied from  $0.90 \text{ nm}$  to  $1.10 \text{ nm}$ . Tables 1 and 2 show observed values when both n-channel and p-channel input differential amplifiers are subjected to oxide thickness variation. Thus from above illustrations, n-channel input differential amplifier shows lesser variation in maximum gain and bandwidth as compared to p-channel input differential amplifier when subjected to oxide thickness.

**Table 1.** Variation in 20 dB differential gain and 3 dB bandwidth of n-channel input differential amplifier due to variation in gate oxide thickness ( $t_{ox}$ )

Gate oxide thickness ( $t_{ox}$ )	Maximum Gain (in 20 dB)	3 dB bandwidth
0.90 nm	41.09 dB	620.18 MHz
0.95 nm	40.91 dB	604.28 MHz
1.00 nm	40.73 dB	583.83 MHz
1.05 nm	40.53 dB	559.15 MHz
1.10 nm	40.33 dB	530.03 MHz

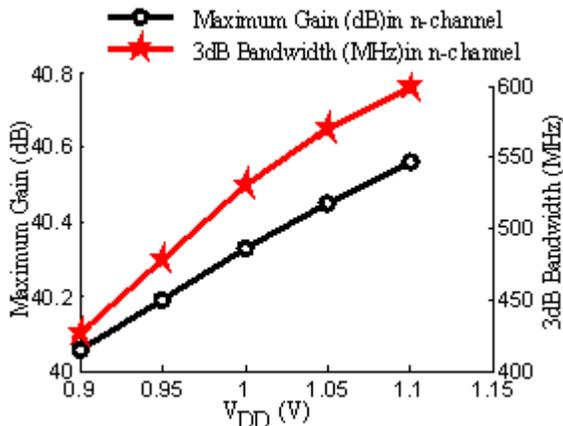
**Table 2.** Variation in 20 db differential gain and 3 dB bandwidth of p-channel input differential amplifier due to variation in gate oxide thickness ( $t_{ox}$ )

Gate oxide thickness (tOX)	Maximum Gain (in 20 dB)	3 dB bandwidth
0.90 nm	40.18 dB	589.91 MHz
0.95 nm	40.12 dB	573.02 MHz
1.00 nm	40.04 dB	551.82 MHz
1.05 nm	39.96 dB	528.62 MHz
1.10 nm	39.87 dB	501.22 MHz

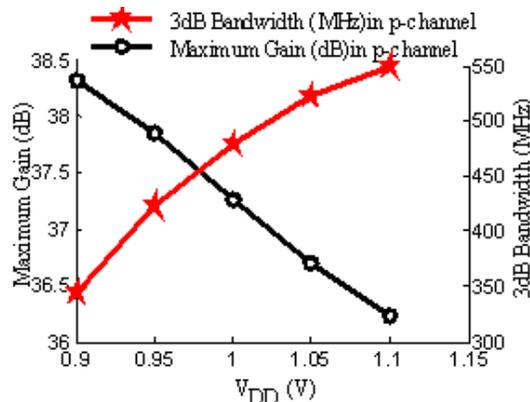
### 4.2 Impact of Variation in Supply Voltage ( $V_{DD}$ ) on Differential Gain

The impact of variation in  $V_{DD}$  on differential gain is studied in this subsection. Supply voltage  $V_{DD}$  is varied from 0.90 V to 1.10 V to observe variation in differential gain and 3dB bandwidth of both the amplifiers as shown in Figures 5 and 6.

The impact of variations in supply voltage ( $V_{DD}$ ) on maximum gain and 3 dB bandwidth is reported in Tables 3 and 4, which are also plotted for making the comparison



**Figure 5.** Variation in maximum (in 20 dB) gain and 3 dB bandwidth of n-channel input differential amplifier due to variation in supply voltage.



**Figure 6.** Variation in maximum (in 20 dB) gain and 3 dB bandwidth of p-channel input differential amplifier due to variation in supply voltage.

**Table 3.** Variation in maximum 20 dB gain and 3 dB bandwidth of n-channel input differential amplifier due to variation in supply voltage

$V_{DD}$	Maximum Gain (20dB)	3dB Bandwidth
0.90 V	40.05 dB	426.08 MHz
0.95 V	40.19 dB	477.70 MHz
1.00 V	40.33 dB	530.02 MHz
1.05 V	40.45 dB	570.20 MHz
1.10 V	40.56 dB	599.05 MHz

**Table 4.** Variation in maximum 20 dB gain and 3 dB bandwidth of p-channel input differential amplifier due to variation in supply voltage

$V_{DD}$	Maximum Gain (20dB)	3dB Bandwidth
0.90 V	38.31 dB	344.24 MHz
0.95 V	37.85 dB	422.71 MHz
1.00 V	37.26 dB	479.06 MHz
1.05 V	36.69 dB	522.33 MHz
1.10 V	36.23 dB	548.98 MHz

clearly visible. As can be seen from Figure 5 maximum gain and 3 dB bandwidth of n-channel input differential amplifier show a positive dependence on  $V_{DD}$ , i. e., they increase with increase in the supply voltage  $V_{DD}$ . An n-channel input differential amplifier shows a variation in maximum gain ( $A_v$ ) from 40.5 dB to 40.56 dB and variation in 3dB bandwidth from 426.08 MHz to 599.05 MHz when  $V_{DD}$  is varied from 0.90 V to 1.10 V. Figure 6 shows dependence of maximum gain and 3 dB bandwidth on supply voltage variation. Maximum gain of p-channel

input differential amplifier exhibits negative dependence on supply voltage variation. In this single stage OTA the maximum gain ( $A_v$ ) varies from 38.31 dB to 36.23 dB due to variation in  $V_{DD}$  from 0.90 V to 1.10 V. However, its 3 dB bandwidth shows positive dependence on  $V_{DD}$  variation. Its 3dB bandwidth varies from 344.24 MHz to 548.98 MHz due to variation in  $V_{DD}$  from 0.90 V to 1.10 V.

### 4.3 Impact of Variation in Temperature on Differential Gain

The temperature dependence on gain is generally due to the variations in threshold voltage and mobility of MOSFETs, which in turn modulates drain to source currents ( $I_{DS}$ ). Impact of variation in temperature on differential gains is reported in Tables 5 and 6 for both n-channel and p-channel input differential amplifiers respectively. The same are plotted in Figures 7 and 8 for visual comparison.

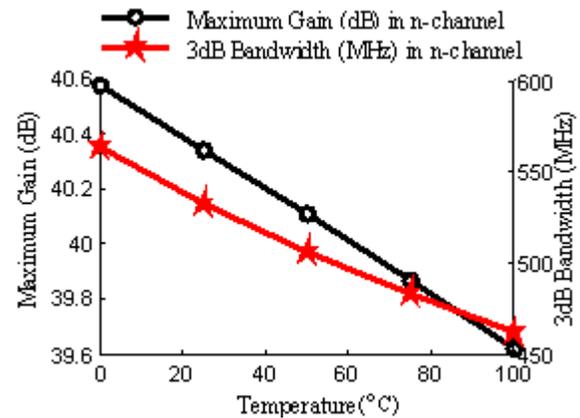
As can be seen the maximum differential gain ( $A_v$ ) decreases with increase in temperature for both n-channel and p-channel differential input single stage OTAs. However, trend is different due to difference in mobility and its dependence on temperature. The maximum differential gain of n-channel input single stage OTA decreases from 40.57 dB to 39.62 dB due to variation in temperature

**Table 5.** Variation in 20 dB differential gain and 3 dB bandwidth of n-channel input differential amplifier due to variation in temperature

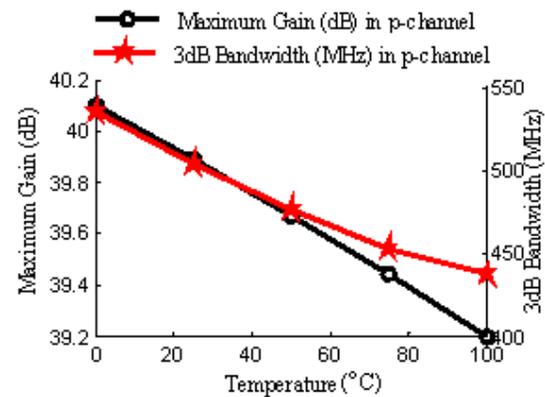
Temperature °C	Maximum Gain (20dB)	3dB Bandwidth
0	40.57 dB	564.06 MHz
25	40.34 dB	532.32 MHz
50	40.11 dB	506.04 MHz
75	39.87 dB	483.34 MHz
100	39.62 dB	462.73 MHz

**Table 6.** Variation in 20 dB differential gain and 3 dB bandwidth of p-channel input differential amplifier due to variation in temperature

Temperature °C	Maximum Gain (20dB)	3dB Bandwidth
0	40.10 dB	535.41 MHz
25	39.89 dB	503.51 MHz
50	39.67 dB	476.61 MHz
75	39.44 dB	452.40 MHz
100	39.20 dB	437.28 MHz



**Figure 7.** Variation in maximum (in 20 dB) gain and 3 dB bandwidth of n-channel input differential amplifier due to variation in temperature.



**Figure 8.** Variation in maximum (in 20 dB) gain and 3 dB bandwidth of p-channel input differential amplifier due to variation in temperature.

from 0 °C to 100 °C, whereas the maximum differential gain of p-channel input single stage OTA decreases from 40.10 dB to 39.20 dB due to variation in temperature from 0 °C to 100 °C<sup>20</sup>.

## 5. Conclusion

This paper investigates impact of process, voltage and temperature (PVT) variations on design metrics of n-channel input CMOS differential amplifier and a p-channel input CMOS differential amplifier and presents comparative results. The results are obtained by simulating both types of single-stage OTAs using Virtuoso Analog Design Environment of Cadence @ 45 nm technology node. It is observed that n-channel differential amplifier is more robust than p-channel differential amplifier when subjected to PVT variations.

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