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Impact of Process Variations on Open Circuit Voltage Gain of CMOS Inverting Amplifiers

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Abstract

Objectives: The impact of process variations on the open circuit voltage gain of CMOS inverting amplifiers is investigated and appropriate aspect ratios are calculated so as to minimize the effect of threshold voltage modulation in short channel devices. **Methods/Analysis:** A diode connected MOS voltage divider is used for biasing the amplifiers. These dividers are less bulky as compared to their resistive counterparts, save chip area and provide better reliability when subjected to variations. **Findings:** The sensitivity parameters for the voltage gain are modeled and their dependences are studied. All simulation results have been performed using CADENCE Virtuoso Analog Design Environment @ 45-nm technology node. **Application:** Push-pull inverting amplifiers are used in CMOS Transimpedance Amplifier forlow noise, high gain and large dynamic range. Transimpedance amplifiers find numerous applications inthe field of optical communications.

Keywords: Aspect Ratio, Gain, Inverting, MOS Divider, Saturation, Sensitivity, Variability

1. Introduction

Aggressive scaling down of semiconductor devices to the nanometer regime results in a decrease in reliability and controllability of the fabrication process. Tolerating process variations, managing design margins and overcoming the short channel effects is becoming increasingly difficult. As a result of which, sensitivity of design parameters such as speed, gain, power dissipation etc. to process imperfections is on the rise.

A number of strategies have been reported in literature to overcome the above issues which include design of robust biasing circuits and current sources. A novel biasing technique for CMOS radio frequency power amplifiers has been proposed in[1] which provides resilience through the threshold voltage adjustment without degradation in the performance. A similar study is carried out in[2] which holds variation in V_{th} responsible for variability in the gain of standard amplifier topologies where transconductance determines the voltage gain and recommends a compensation scheme for an inductively degenerated cascode LNA. Addition-based and square-root-based current generators are presented in[3] which provide significant improvement in the output standard deviation and can be used to obtain improved control over gain, bandwidth, skew etc. of analog circuits. A compensation circuit for LNA and mixers is reported in[4] which reduce the variability in device performance metrics by adapting to the temperature and process variations and generating an appropriate bias voltage accordingly. Another current source topology in reported in [5]which consists ofa ring based connection of odd number of inverters and additional transistors and can be used for biasing inverter chains and other integrated circuits.

Several analysis and studies of different analog and digital integrated circuits have also been reported which help in better understanding of process variations and lay down the guidelines to reduce their impact. The influence of gate-oxide breakdown on CS amplifiers with diode-connected active loads is investigated in[6]. In[7], the impact of the intrinsic-parameter fluctuations such as metal-gate work-function fluctuation (WKF) and random- dopant fluctuation (RDF) etc. is estimated for MOS circuits. Further, the static, dynamic and short

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circuit power dissipations are looked upon. A similar study involving the impact of process mismatch on the performance of domino and static 1-bit full adders is presented in[8]. However, a thorough variability analysis of CMOS inverting amplifiers has not been carried out before.

In view of the above, this paper makes the following contributions:

- Deviation in threshold voltage (V_{th}) with process variations is studied and designs are sized accordingly.
- Diode-connected MOS dividers are used for biasing which provide robustness to the amplifier design.
- Variability analysis of open circuit voltage gain of CMOS inverters is carried out and sensitivity parameters are modeled.

The rest of the paper is organized as follows. Section 2 describes the experimental setup used. In Section 3, the dependence of threshold voltage (V_{th}) on transistor aspect ratios is studied and optimum channel lengths and widths are selected. A brief review of the expressions for gain of inverting amplifiers is presented in Section 4. The behavior of open circuit voltage gain of three basic inverting amplifier topologies when subjected to process variations is described in Section 5 and sensitivity parameters are determined. Finally, the concluding remarks are provided in section 6.

2. Experimental Setup

Three basic CMOS inverting amplifiers namely active PMOS load inverter, current source inverter and push-pull inverter are analyzed and dependence of their open circuit voltage gain on various parameters is studied.

The amplifiers are biased in saturation and the output DC voltage level is kept at $V_{DD}/2$ so as to provide maximum room for output swing. A diode connected MOS divider as shown in Figure 1 is used to provide the appropriate gate bias to the amplifying transistor. This biasing scheme makes the amplifier robust as compared to its resistor-only and resistor-MOS counterparts. This also makes the amplifier less sensitive to temperature variation[9]. Also, transistors are sized such that minimum variation in threshold voltage V_{th} is observed since invariant threshold voltage directly influences the overall robustness of the circuit.

The bias voltage can be determined by equating the current in the two MOSFETs i.e.

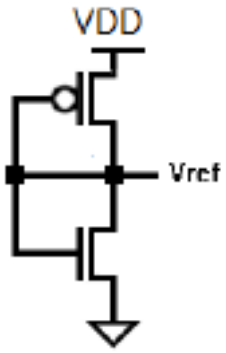

Figure 1. Circuit level model of diode-connected voltage reference.

$$I_{DN} = I_{DP} \tag{1}$$

which is equivalent to

$$\beta_N \left(V_{ref} - V_{tn}\right)^2 = \beta_P \left(V_{DD} - V_{ref} - V_{tp}\right)^2 \tag{2}$$

Solving for V_{ref} from (2),

$$V_{ref} = \frac{V_{DD} - V_{tp} + \sqrt{\frac{\beta_N}{\beta_P}}\left(V_{tn}\right)}{\sqrt{\frac{\beta_N}{\beta_P}} + 1} \tag{3}$$

where, β_N and β_P and V_{tn} and V_{tp} are the beta effective and threshold voltage values for NMOS and PMOS transistors respectively. V_{ref} is the bias voltage.

Similarly, the beta ratio for the two transistors can be calculated if the V_{ref} is known i.e.

$$\frac{\beta_1}{\beta_2} = \left[\frac{V_{DD} - V_{ref} - V_{tp}}{V_{ref} - V_{tn}}\right]^2 \tag{4}$$

The circuit level model for each of the inverting amplifiers is shown in Figure 2.

3. Sizing Ratio Selection

The threshold voltage V_{th} is affected by process variations and decreases with decrease in the channel length (L) and channel width (W) due to short channel effects[10]. To study the above, an NMOS transistor was biased in saturation in such a way that $V_{DS}=V_{DD}/2$ and the impact of its aspect ratio on V_{th} was analyzed. The results obtained are shown in Figures 3 and 4.

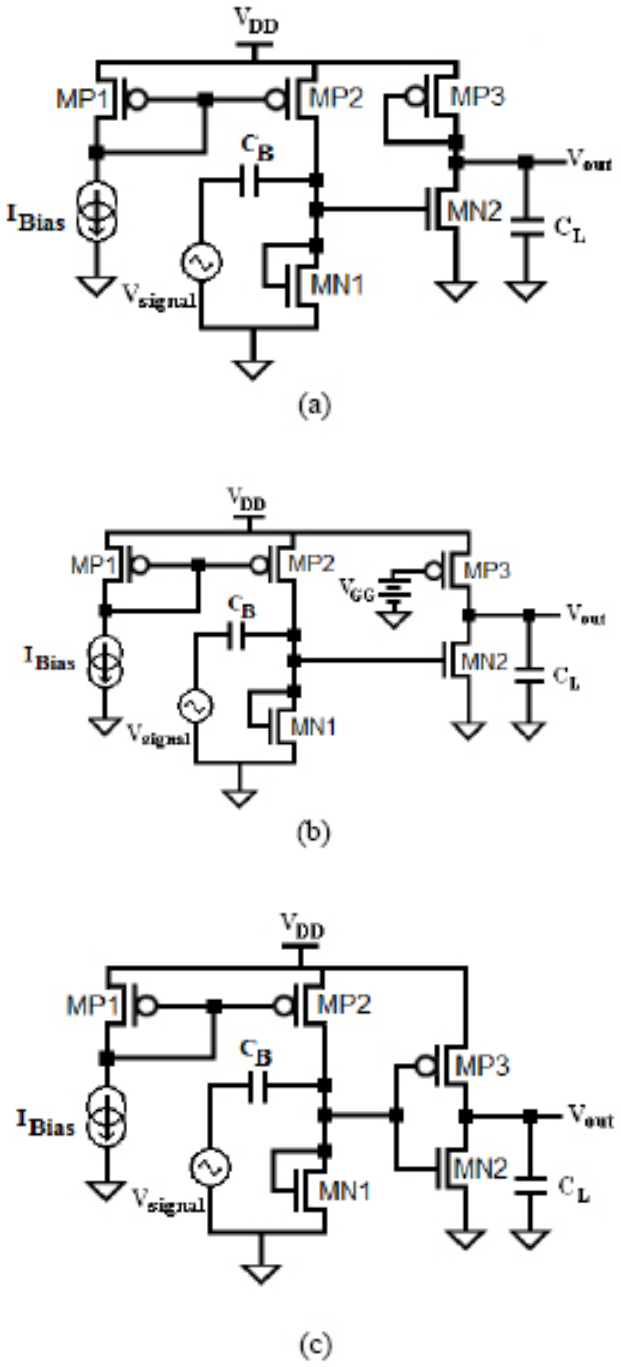

Figure 2. **(a)** Active PMOS load inverter, **(b)** Current source load inverter and **(c)** Push-pull inverter.

From Figure 3, it is observed that V_{th} becomes more or less constant after 180 nm (3.5 times 45 nm) making it suitable for circuit design.

Similarly, from [Figure 4], it is observed that V_{th} is essentially constant after 6 µm. However, the effect of

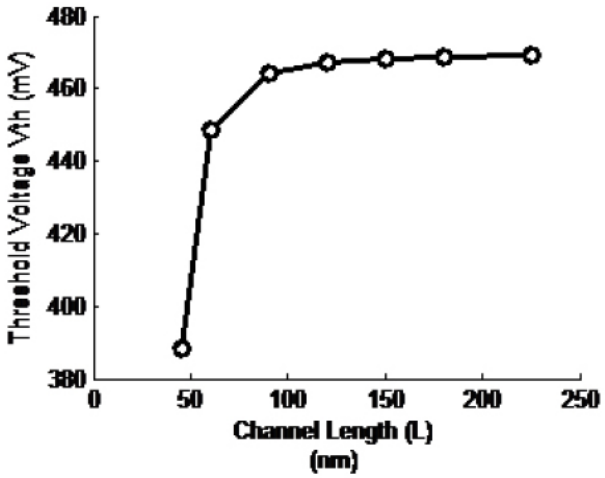

Figure 3. Variation of threshold voltage with channel length.

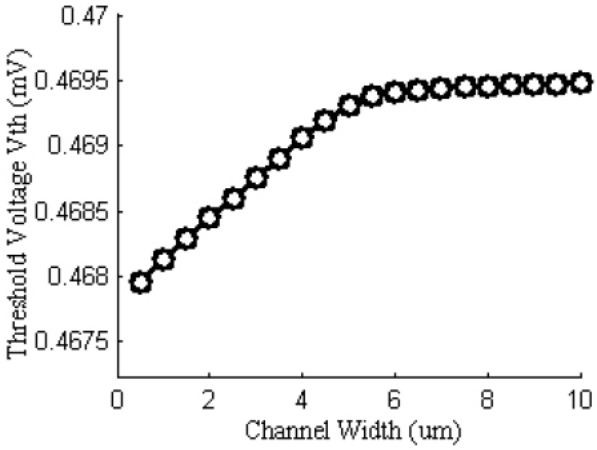

Figure 4. Dependence of threshold voltage on channel width.

channel length L variation on V_{th} is much more dominant in comparison to W variation. Hence, taking the above and required bias voltages into consideration the transistors are appropriately sized. The sizing ratio for each of the amplifiers is tabulated in Table 1, Table 2 and Table 3 respectively.

4. CMOS Inverting Amplifiers

The CMOS inverting amplifiers differ from each other in respect to the gate connection of the load PMOS such that:

Table 1. Specifications for active PMOS load Inverter

Transistor	Channel Length (L)	Channel Width (W)	Threshold Voltage (V_{th})
MN1, MN2	180 nm	2.7 µm	468.61 mV
MP1, MP2	180 nm	2.7 µm	–417.44 mV
MP3	180 nm	7.0 µm	–417.37 mV

Table 2. Specifications for current source inverter

Transistor	Channel Length (L)	Channel Width (W)	Threshold Voltage (V_{th})
MN1, MN2	180 nm	2.7 µm	468.61 mV
MP1, MP2	180 nm	2.7 µm	–417.44 mV
MP3	180 nm	7.05 µm	–417.37 mV

Table 3. Specifications for push-pull inverter

Transistor	Channel Length (L)	Channel Width (W)	Threshold Voltage (V_{th})
MN1, MN2	180 nm	2.7 µm	468.61 mV
MP1, MP2	180 nm	2.7 µm	–417.44 mV
MP3	180 nm	4.65 µm	–417.40 mV

- $V_{GS} = V_{DS}$, as in case of active PMOS load inverter
- $V_{GS} = V_{GG} - V_{DD}$, for current source load inverter
- $V_{GS} = V_{IN}$, push-pull inverter.

The Active PMOS Load Inverter (APLI) is a low gain inverting stage with highly predictable small and large signal characteristics. Its gain and output resistance can be defined as

$$A_V = \frac{-g_{mN}}{g_{dsN} + g_{dsP} + g_{mP}} \approx \frac{-g_{mN}}{g_{mP}} \tag{5}$$

which is equivalent to

$$A_V = -\left(\frac{K_N W_N L_P}{K_P L_N W_P}\right)^{\frac{1}{2}} \tag{6}$$

Here, g_{mN} and g_{mP} are the transconductances of the amplifying NMOS and load PMOS devices respectively. The negative sign depicts the phase difference of 180° between the output and the input excitation. The equivalent output resistance for the APLI can be defined as

$$R_{out} = \frac{1}{g_{dsN} + g_{dsP} + g_{mP}} \approx \frac{1}{g_{mP}} \tag{7}$$

The current source load inverter (CSLI) has a higher gain as compared to the PMOS load inverter and consists of a common-gate configuration with gate bias equal to V_{GG}. It can be modeled as

$$A_V = \frac{-g_{mN}}{g_{dsP} + g_{dsN}} = \left(\frac{-1}{\lambda_P + \lambda_N}\right)\left(\frac{2K_N W_N}{L_N I_D}\right)^{1/2} \tag{8}$$

where, g_{mN} is the transconductance of the amplifying NMOS and g_{dsN} and g_{dsP} are the reciprocal values of the channel resistance of NMOS and PMOS transistors respectively.

From above, it can be seen that

$$A_V \propto \frac{1}{\sqrt{I_D}} \tag{9}$$

where, I_D is the DC bias current through the amplifying transistor. Hence, the gain A_V has a negative dependence on the DC current which is true only until the current reaches the sub threshold region of operation[11].The output resistance for the current source inverter can be written as

$$R_{out} = \frac{1}{g_{dsN} + g_{dsP}} \cong \frac{1}{I_D\left(\lambda_P + \lambda_N\right)} \tag{10}$$

The push-pull inverter has the maximum gain out of all the inverter configurations which can be defined as

$$A_V = \frac{-\left(g_{mN} + g_{mP}\right)}{g_{dsN} + g_{dsP}} \tag{11}$$

Here, $g_{mN}$and g_{mP} are the transconductances and g_{dsN} and g_{dsP} are the reciprocal of channel resistance of MN2 and MP3 respectively. From (11),

$$A_V = -\sqrt{\frac{2}{I_D}}\left[\frac{\sqrt{K_N\left(\frac{W_N}{L_N}\right)} + \sqrt{K_P\left(\frac{W_P}{L_P}\right)}}{\lambda_N + \lambda_P}\right] \tag{12}$$

A negative dependence on the DC current is observed as in case of the current source inverter. Also, the output resistance is identical to that in equation (10).

5. Impact of Process Variation on Gain

The sensitivity of open circuit voltage gain (A_V) of an amplifier with respect to any parameter p can be modeled using the following sensitivity parameter[12].

$$S_p^{A_v} = \frac{\partial A_V}{\partial p} \cdot \frac{p}{A_V} \tag{13}$$

5. 1 Sensitivity of Gain to Channel Length of Load PMOS

For the APLI, the above can be defined with respect to L_P (channel length of PMOS) as

$$S_{L_P}^{A_v} = \frac{\partial A_V}{\partial L_P} \cdot \frac{L_P}{A_V} \tag{14}$$

Differentiating A_V with respect to L_p,

$$\frac{\partial A_V}{\partial L_P} = -\frac{1}{2}\left(\frac{K_N W_N}{K_P L_N W_P L_P}\right)^{\frac{1}{2}} \tag{15}$$

and substituting the values in (14), we get

$$S_{L_P}^{A_v} = \frac{1}{2}\left(\frac{K_N W_N}{K_P L_N W_P L_P}\right)^{\frac{1}{2}} \cdot \frac{L_P \left(K_P L_N W_P\right)^{\frac{1}{2}}}{\left(K_N W_N L_P\right)^{\frac{1}{2}}} \tag{16}$$

which can be simplified to

$$S_{L_P}^{A_v} = \frac{1}{2} \tag{17}$$

Hence, the sensitivity of A_V is a constant. Also from (6), it can be seen that magnitude of A_V has a positive dependence on L_P which can be verified from (15).

For current source inverter considering the NMOS in saturation region, the gain A_V from (8) can be defined as

$$A_V = -\left(\frac{1}{\lambda_N + \lambda_P}\right)\left\{\frac{2K_N W_N L_P}{L_N K_P W_P \left(V_{SG} - \left|V_{tp}\right|\right)}\right\}^{\frac{1}{2}} \tag{18}$$

Differentiating (18) with respect to L_p,

$$\frac{\partial A_V}{\partial L_P} = -\left(\frac{1}{\lambda_N + \lambda_P}\right)\sqrt{\frac{2K'_N W_N}{L_N K'_P W_P}}\,\frac{\partial}{\partial L_P}\left(\sqrt{\frac{L_P}{V_{SG} - \left|V_{tp}\right|}}\right) \tag{19}$$

where,

$$\frac{\partial}{\partial L_P}\left(\sqrt{\frac{L_P}{V_{SG} - \left|V_{tp}\right|}}\right) = \frac{1}{2}\sqrt{\frac{V_{SG} - \left|V_{tp}\right|}{L_P}}\left(\frac{V_{SG} - \left|V_{tp}\right| + L_P \frac{\partial V_{tp}}{\partial L_P}}{\left(V_{SG} - \left|V_{tp}\right|\right)^2}\right) \tag{20}$$

Considering the variation of threshold with channel length negligible due to appropriate sizing ratios i.e.

$$\frac{\partial V_{tp}}{\partial L_P} \approx 0. \tag{21}$$

Therefore, from (20)

$$\frac{\partial A_V}{\partial L_P} = -\frac{A_V}{2L_P} \tag{22}$$

which on substituting in (14) gives

$$S_{L_P}^{A_v} = -\frac{1}{2}. \tag{23}$$

In case of the push-pull inverting amplifier

$$A_V = -\left(\frac{1}{\lambda_N + \lambda_P}\right)\left\{\sqrt{\frac{4K'_N W_N L_P}{L_N K'_P W_P \left(V_{SG} - \left|V_{tp}\right|\right)}} + \sqrt{\frac{4}{V_{SG} - \left|V_{tp}\right|}}\right\} \tag{24}$$

This on differentiation gives

$$\frac{\partial A_V}{\partial L_P} = \left(\frac{1}{\lambda_N + \lambda_P}\right)\left[\frac{2}{L_P}\left\{A_V\left(\lambda_N + \lambda_P\right) - \sqrt{\frac{4}{V_{SG} - \left|V_{tp}\right|}}\right\}\right]. \tag{25}$$

The sensitivity parameter in this case can be derived in a similar way as seen in (14) i.e.

$$S_{L_P}^{A_v} = 2\left\{1 - \frac{1}{A_V\left(\lambda_N + \lambda_P\right)}\sqrt{\frac{4}{V_{SG} - \left|V_{tp}\right|}}\right\}. \tag{26}$$

The variation of gain A_V and the output voltage swing with L_p is shown in Figure 5.

5. 2 Sensitivity of Gain to Channel Length of Amplifying NMOS

For the active PMOS load inverter, sensitivity with respect to the channel length of the amplifying transistor L_N can be determined using (6) as

$$S_{L_N}^{A_v} = \frac{1}{2} \tag{27}$$

Since differentiating (6) w. r. t L_N gives

$$\frac{\partial A_V}{\partial L_N} = \frac{A_V}{2L_N}. \tag{28}$$

Hence, the open circuit voltage gain A_V of the APLI has the same sensitivity to both L_N and L_P.

A similar expression for the sensitivity parameter is obtained for the current source inverter, as in the previous case.

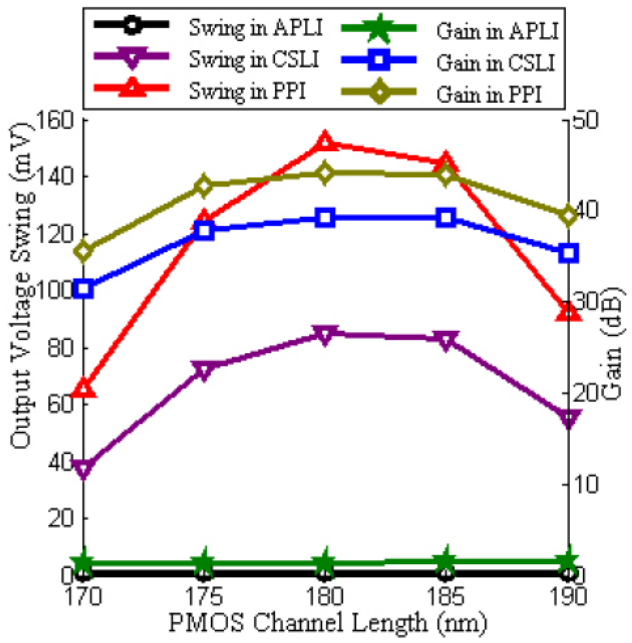

Figure 5. Variation of gain and output voltage swing with channel length of PMOS load.

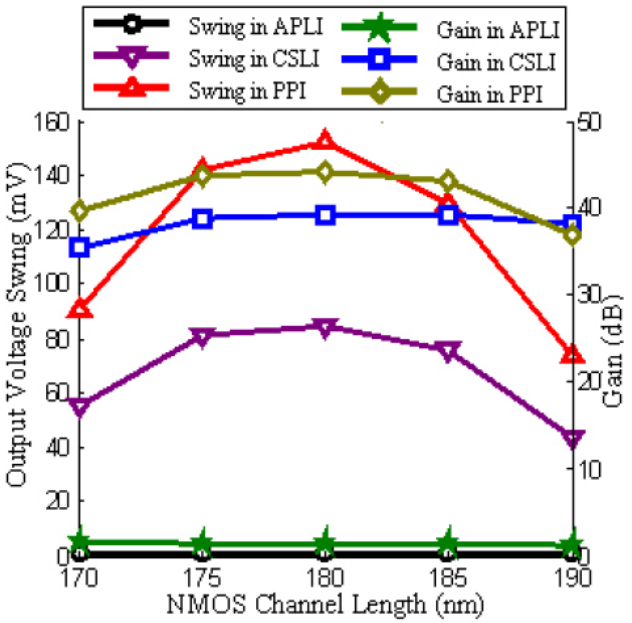

Figure 6. Dependence of gain and output voltage swing on the channel length of amplifying NMOS.

For the push-pull inverter,

$$\frac{\partial A_V}{\partial L_N}=\left(\frac{1}{\lambda_N+\lambda_P}\right)\left[\frac{1}{2L_N}\left\{-A_V\left(\lambda_N+\lambda_P\right)-\sqrt{\frac{4}{V_{SG}-\left|V_{tp}\right|}}\right\}\right] \quad (29)$$

which gives

$$S_{L_N}^{A_v}=-\frac{1}{2}\left\{1+\frac{1}{A_V\left(\lambda_N+\lambda_P\right)}\sqrt{\frac{4}{V_{SG}-\left|V_{tp}\right|}}\right\}. \quad (30)$$

The variation of gain A_V and the output voltage swing with L_N is shown in Figure 6.

5. 3 Sensitivity of Gain to Width of Load PMOS

The variation of gain A_V with respect to width of the load PMOS is shown in Figures 7 and 8. For the active PMOS load inverter, differentiating (6) w. r. t. W_P

$$\frac{\partial A_V}{\partial W_P}=\frac{A_V}{2W_P} \quad (31)$$

$$S_{W_P}^{A_v}=\frac{1}{2}. \quad (32)$$

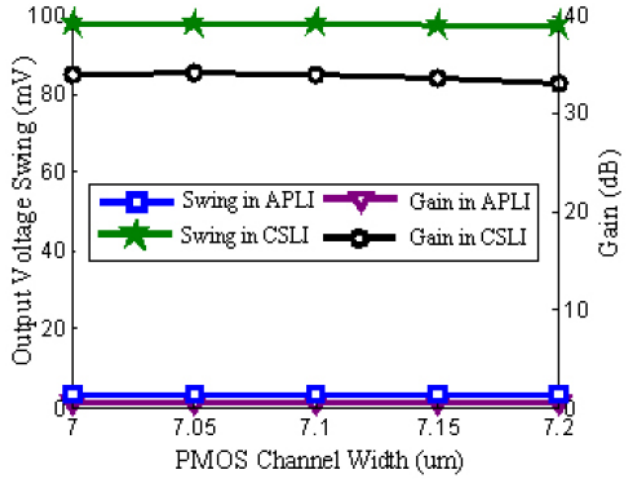

Figure 7. Gain and output voltage swing variation with respect to channel width of Load PMOS.

Similarly, for the current source inverter

$$\frac{\partial A_V}{\partial W_P}=-\frac{A_V}{2\left(V_{SG}-\left|V_{tp}\right|\right)}\left\{V_{SG}-\left|V_{tp}\right|-W_P\frac{\partial V_{tp}}{\partial W_P}\right\}. \quad (33)$$

Since the variation in threshold voltage with W_P is negligible,

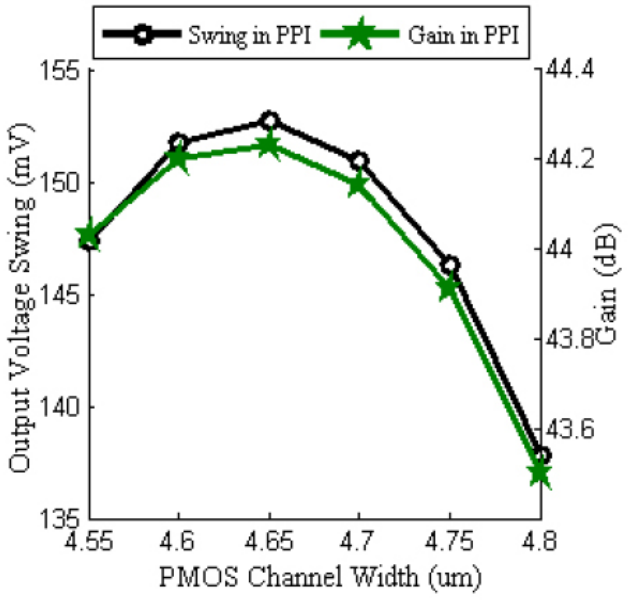

Figure 8. Gain and output voltage swing variation with W_P for PPI.

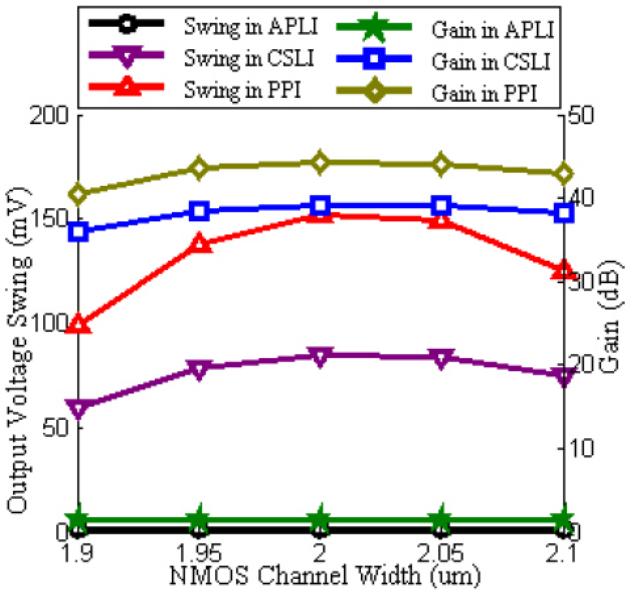

Figure 9. Deviation in gain and output voltage swing channel width of amplifying NMOS.

$$\frac{\partial V_{tp}}{\partial W_P} \approx 0 \tag{34}$$

Substituting in (33) and solving for *S* gives

$$S_{W_P}^{A_v} = -\frac{1}{2}. \tag{35}$$

In case of the push-pull inverting amplifier,

$$\frac{\partial A_V}{\partial L_N} = \left(\frac{1}{\lambda_N + \lambda_P}\right)\left[\frac{1}{2W_P}\left\{-A_V\left(\lambda_N + \lambda_P\right) - \sqrt{\frac{4}{V_{SG} - |V_{tp}|}}\right\}\right] \tag{36}$$

which gives the sensitivity of A_V w.r.t W_P as

$$S_{W_P}^{A_v} = -\frac{1}{2}\left\{1 + \frac{1}{A_V\left(\lambda_N + \lambda_P\right)}\sqrt{\frac{4}{V_{SG} - |V_{tp}|}}\right\}. \tag{37}$$

5. 4 Sensitivity of Gain to Width of Amplifying NMOS

A similar analysis for APLI as in previous cases shows that

$$\frac{\partial A_V}{\partial W_N} = -\frac{1}{2}\left(\frac{K'_N L_P}{K'_P L_N W_P W_N}\right)^{\frac{1}{2}} \tag{38}$$

$$S_{W_N}^{A_v} = \frac{1}{2}\left(\frac{K'_N L_P}{K'_P L_N W_P W_N}\right)^{\frac{1}{2}} \cdot \frac{W_N\left(K'_P L_N W_P\right)^{\frac{1}{2}}}{\left(K'_N W_N L_P\right)^{\frac{1}{2}}} = \frac{1}{2} \tag{39}$$

For the current source inverter

$$S_{L_P}^{A_v} = -\frac{1}{2}. \tag{40}$$

Similarly, for the push-pull inverter

$$\frac{\partial A_V}{\partial W_N} = \left(\frac{1}{\lambda_N + \lambda_P}\right)\left[\frac{2}{W_N}\left\{A_V\left(\lambda_N + \lambda_P\right) - \sqrt{\frac{4}{V_{SG} - |V_{tp}|}}\right\}\right] \tag{41}$$

$$S_{W_N}^{A_v} = 2\left\{1 - \frac{1}{A_V\left(\lambda_N + \lambda_P\right)}\sqrt{\frac{4}{V_{SG} - |V_{tp}|}}\right\} \tag{42}$$

The variation in A_V and output voltage swing with change in W_N is depicted in Figure 9.

6. Conclusions

The impact of process variations on open circuit voltage gain of three basic CMOS inverting amplifier configurations is studied and appropriate sizing ratios for enhancing the circuit robustness are proposed. The Active

PMOS Load Inverter has the least gain out of the three amplifiers. However, it presents the least variation when subjected to variations in various device parameters. The push-pull inverter has the maximum gain but also the most sensitive to changes in aspect ratios. All the simulation results have been performed using Virtuoso Analog Design Environment of Cadence@ 45-nm technology node.

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