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Robust Study and Design of a Low Power CMOS CSVCO using 45nm Technology

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Abstract

This paper consist of the design and detailed study of a three stage Current Starved Voltage Controlled Oscillator having a very low voltage supply of 1V with low phase noise. The Three stage CSVCO is designed. This work is being done on Cadence virtuoso analog and digital IC design tools with gpdk 45nm CMOS technology process. The voltage supply is taken to be 1V which is low and quite useful according to the latest trends. The center frequency is taken to be 2.4 GHz which is best suitable for satellite and many other applications. The proposed CSVCO consumes low power, low area, low phase noise and high oscillation frequency. The design procedure adopted and the simulation results acquired are illustrated. This CSVCO is suitable for a fast locking PLL, for frequency synthesizer, for clock generation and recovery etc. The results obtained are compared with the previous works and improvements are observed. The Phase noise of the proposed CSVCO is less as compared to the other works.

Keywords: CMOSFET (Complementary Metal Oxide Semiconductor Field Effect Transistor); CSVCO(Current Starved Voltage Controlled Oscillator); low area; low phase noise, PLL (Phase locked loop).

1. Introduction

A CMOS VCO(Voltage Controlled Oscillator) is an important block of PLL(Phase Locked Loop) and also it has multiple applications in digital as well as analog communication[1]. The power consumption and the area occupied by a PLL is mainly depend on VCO[2,3]. Thus VCO should be of less area and low power consumption as well. This proposed design methodology consumes minimum phase noise due to novel infeasibility driven evolutionary algorithm (IDEA)[4]. VCO is an important component of Radio Frequency transceivers and it is commonly used in various tasks of signal processing such as selection of frequency and generation of signal[4]. These days Radio Frequency transceivers also constitute of PCF (Programmable Carrier Frequencies) and thus they also rely on PLL. The transceivers of wireless communication system comprises of PA (Power Amplifiers), LNA(Low Noise Amplifiers), DSP(Digital Signal Processing) chip, mixers, filters and PLL. Reducing phase noise or jitter and optimization of Oscillators are the main areas of work these days[5,6]. Ultra low power, less area and low phase noise are the main requirements of device to be portable and having good performance[7,8]. However, for battery operated devices the low power consumption is the main requirement. Fig.1 shows the schematic of a conventional CSVCO (Current Starved Voltage Controlled Oscillator). It consists of inverter and Current Starved Stage which consumes low power and low phase noise.

Nowadays, in advance PLL two different categories of VCO, CSVCO and SCVCO (Source Coupled Voltage Controlled Oscillator) are used. Recent studies show LC oscillators also have low power consumption as well as good phase noise performance. But they also have some drawbacks such as First, the tuning range of LC Oscillators are low as compared to ring oscillators and Second, the quality of on chip spiral inductors mainly decides the phase noise performance of Oscillators, which is not easy

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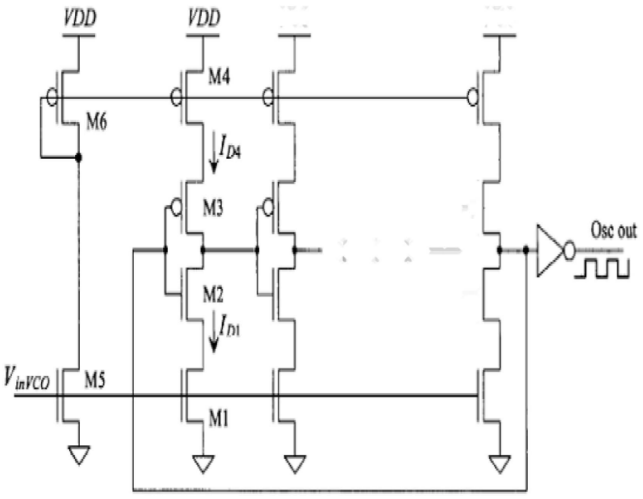

Figure 1. Conventional Current Starved VCO.

to be achieved. However, Ring oscillators have no such complication of spiral inductors like LC Oscillators. Thus they occupy less area. In this paper mainly focus on the design technique of a low power CSVCO with 1V of voltage supply which also has less area and low phase noise with high oscillation frequency. Rest of the paper is demonstrated in following sections: Section II explains the design of current starved VCO and the previous works done on it. Section III demonstrates the simulation results, discussion and performance comparison of proposed VCO with previous works and Section IV finally shows the conclusion.

2. Circuit Description

Current starved voltage controlled oscillator can be designed using ring oscillators. Because in ring oscillators, the gate capacitances of most inverter varies by controlling the charging and discharging of the gate capacitances. Decrease in the peak available charging current results in increase of the time when discharging and charging the gate capacitance; and thus there is decrease in frequency. Ring oscillators can generate high frequency of oscillation which ranges up to a few GHz. The Fig.1 shows the schematic of current starved VCO. The operation of CSVCO is similar to that of a Ring Oscillator. The transistors M2 and M3 i.e. NMOS and PMOS works together as an inverter, whereas transistors M1 and M4 i.e. NMOS and PMOS works as current sources. These current sources limits the current being passed to the transistors M2 and M3. And it illustrates that Inverter is starved for current. The input control voltage sets the drain current of transistors M5 and M6 are same[9,10]. Each inverter/current source stage has same drain current as transistors M5 and M6 and are said to be mirrored. Consequently, the change in $V_{control}$ leads to the change in inverter current at each stage. The frequency of oscillation for N stage Current Starved Voltage Controlled Oscillator (CSVCO) is represented as:

$$f = \frac{1}{2NT} \quad (1)$$

Where f is the frequency of oscillation of CSVCO.

Total Capacitance of CSVCO can be determined by the following equation:

$$C_{tot} = C_{out} + C_{in} \quad (2)$$

$$C_{tot} = C_{ox}(A_p + A_n) + \frac{3}{2}C_{ox}(A_p + A_n)$$

$$C_{tot} = \frac{5}{2}C_{ox}(A_p + A_n) \quad (3)$$

Where, $A_n = W_n L_n$, $A_p = W_p L_p$, C_{ox} is the oxide capacitance, L_p, L_n are channel lengths and W_p, W_n, are channel widths and A_p, A_n are cross sectional areas of the PMOS and NMOS transistors respectively.

3. Methodology

Here, three stages current starved VCO circuit is being implemented using Cadence virtuoso analog and digital IC design tools of gpdk 45nm CMOS process technology. The voltage supply of 1V is provided. The schematic of 3 stages CSVCO is shown in Fig. 2 and it is also verified

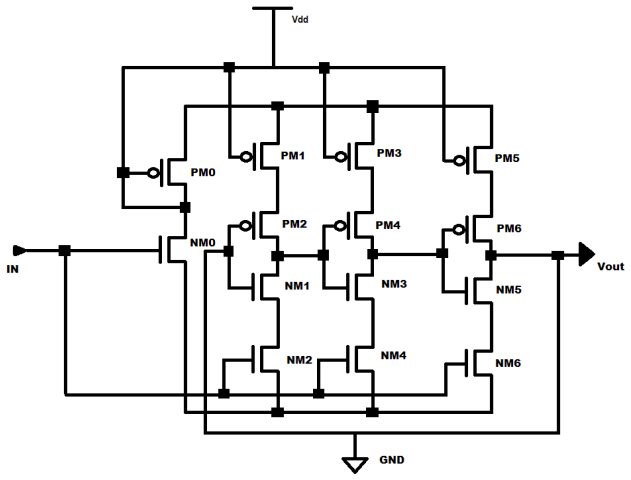

Figure 2. Schematic of the three stage Current Starved VCO.

using Cadence spectre tools of gpdk 45nm CMOS technology process.

4. Simulation Result and Discussion

After simulating the three stages CSVCO with voltage supply 1V and Center frequency 2.4GHz. We get the outputs as shown. Fig.3 shows the transient response of three stages current starved VCO. The Phase noise output of three stages current starved VCO is shown in Fig.4 and it is being observed that the phase noise comes out to be -112.9 dBc/Hz. Fig. 5 shows the power consumption output of three stage current starved VCO. The power consumed by the circuit is observed to be 32μW. The Frequency Vs control voltage graph of a CSVCO ideally should be linear. But in practical it is difficult to achieve a proper linear curve. The Fig.6 shows the graphical representation of Frequency versus Control Voltage. The

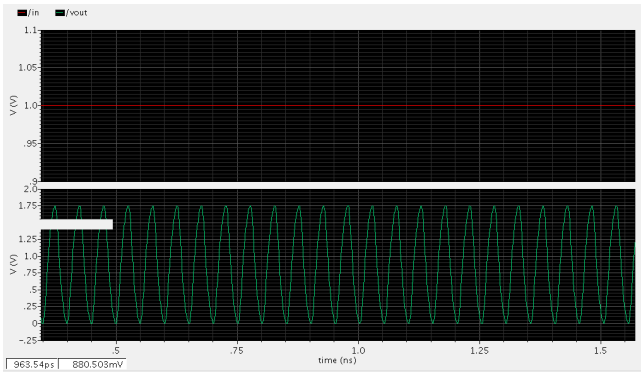

Figure 3. Transient response of three stage Current Starved VCO.

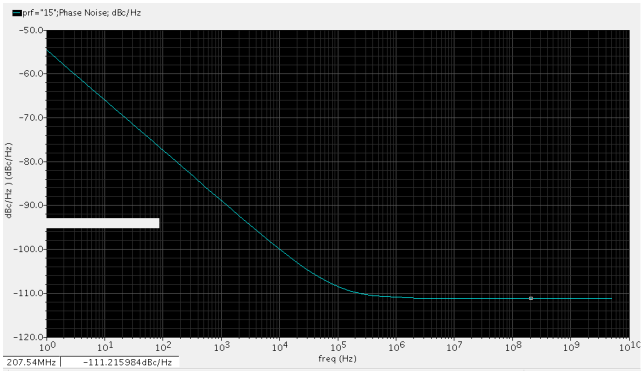

Figure 4. Phase Noise of three stage Current Starved VCO.

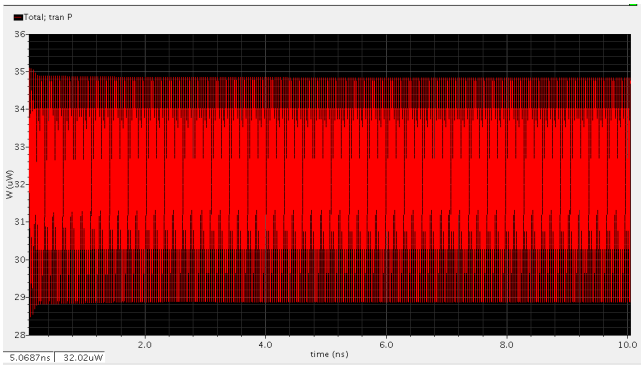

Figure 5. Power consumption of three Stage Current Starved VCO.

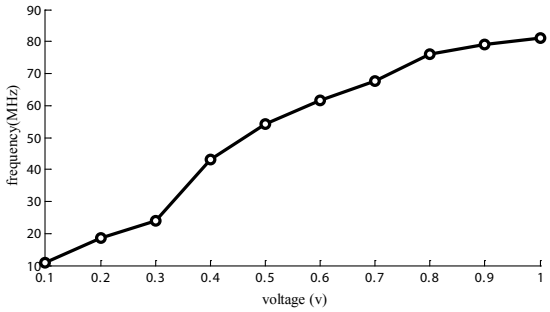

Figure 6. Graphical representation of Frequency Vs Control Voltage.

Table 1. Performance Comparison of Present Work with earlier reported Work

Parameters	Ref.[4]	Ref[9]	Ref[10]	This Design
Technology	90nm	180nm	130nm	45nm
Voltage supply	1.2 V	1.8V	1.2V	1V
Phase noise @ 1MHz	–87.7dBc/Hz	–93dBc/Hz	–92.6dBc/Hz	–112.9dBc/Hz
Center frequency	2GHz	320–960MHz	1.2GHz	2.4GHz
Power consumption	412.71uW	20mW	25mW	32uW

performance of this three stage CSVCO is being compared with the other works and found that this work is better than other works. Table 1 shows the comparison on the basis of various parameters.

5. Conclusion

This paper presents a design of low power, low phase noise CMOS three stage Current starved Voltage Controlled

Oscillator (CSVCO) using 45nm CMOS technology. Finally, the comparison of the present work with the earlier published work has been done and the improvements are observed. With the simulation results it can be concluded that the proposed CSVCO could achieve high frequency of oscillation having low power consumption and better phase noise performance. The proposed design is suitable for wireless communication.

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