ISSN (Print) : 0974-6846
Indian Journal of Science and Technology, *Vol 9(45), DOI: 10.17485/ijst/2016/v9i45/99076, December 2016* ISSN (Online) : 0974-5645

Neutral Point Clamped and Cascaded H-Bridge Multilevel Inverter Topologies – A Comparison

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Abstract

Objectives: This work emphasizes on the analysis of two five levels inverter topologies - neutral point clamped topology and Cascaded H-Bridge inverter topology. **Methods/Analysis:** The neutral point clamped topology requires only one DC source, eight switches and four clamping diodes with two voltage balancing capacitors. The cascaded topology carries two voltage sources and eight switching devices. Phase disposition pulse width modulation technique generates gating pulses for both the multilevel inverter topologies. All the simulations are done in MATLAB-Simulink simulation environment. **Findings:** The output waveforms, switching stress and harmonic spectrum of the output waveforms of both the inverter topologies are obtained using phase disposition pulse width modulation technique for a modulation index of unity. Moreover, the work aims to perform a comparison of both the inverter topologies with respect to total harmonic distortion, switch stress and complexity of the topology. It is found that though a cascaded inverter needs less overall components when compared to neutral point clamped inverter, yet both the inverter topologies carries the same stress across their switches and produce an almost the same harmonic distortion on their output waveforms. **Applications/Improvement:** Conventional voltage source inverters are gradually being replaced by multilevel inverters in various applications like photovoltaic systems, reactive power compensators, FACTS devices, adjustable speed drives etc. The stress across each of the switches gets decreased in both the multilevel inverter topologies compared to conventional inverters. Further, neutral point clamped inverters carry the advantage of requiring only one DC source for its operation.

Keywords: Cascaded H-Bridge (CHB), Neutral Point Clamped (NPC), Sinusoidal Pulse Width Modulation (SPWM), Total Harmonic Distortion (THD)

1. Introduction

Multilevel inverters are being preferred as an alternative for conventional two level inverters in many applications involving drives, FACTS and renewable energy sources. The conventional inverters possess many drawbacks such as high switching stress, increased Total Harmonic Distortion (THD), high dv/dt and EMI[1–4]. Further operating these inverters at high switching frequency produces high switching loss. Multilevel inverters on the other hand, produce improved waveforms, lesser switching losses and THD and decreased voltage stress[4]. With multilevel inverters it is possible obtain increased number of output levels and with this high power output can be obtained without the use of transformers and high voltage semiconductor switches[1]. Also, multilevel inverters can operate at both lower and higher switching frequencies[5]. The basic topologies employed are, the neutral point clamped topology[6–10], capacitor clamped topology[11,12] and cascaded multilevel inverter topology[13–15]. Capacitors are involved to increase the levels in a capacitor clamped multilevel inverter. For an n-level inverter, (n-1) DC link capacitors are required. Excessive number of storage capacitors is required to obtain high voltage steps. This topology also has voltage unbalance issues. A neutral point clamped topology carries more clamping diodes to increase the output levels. Further, voltage unbalance occurs inherently in a diode clamped topology. Use of clamping diodes creates complexity and increases the inverter size and cost. In a Cascaded H-Bridge (CHB) inverter, a number of single phase inverters are connected in series. The number of inverters influences the output

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level. An 'm' level CHB inverter involves (m-1) single phase inverters. It carries a simple structure and is more reliable. However each H-Bridge needs an isolated power supply. Many new multilevel inverter topologies with additional features such as decrease in the switches, capacitors, diodes, sources etc. have been obtained from these basic topologies[16–19].

These multilevel inverters employ a modulation technique to switch ON and OFF their devices. Different modulation schemes characterized to get lesser harmonic content and better output waveforms have been proposed[20,21]. These modulation techniques play a crucial role in determining the efficiency, switching stress and harmonic content of a multilevel inverter system. The major modulation strategies employed for multilevel inverters are the sinusoidal pulse width modulation[22], Space Vector Modulation[23–25] (SVM) and selective harmonic elimination techniques[26–29]. In SVM technique, it is flexible to select the best switching state among the various redundant states and it provides better harmonic performance[22]. But, implementing the SVM technique is complex and involves computational burden. SHE techniques are low frequency methods and require iterative procedures to arrive at optimal switching angles to realize the switching state in a multilevel inverter[30]. SPWM technique is based on the multicarrier PWM technique wherein multiple carrier waves are compared with a reference signal to obtain gating pulses for the inverter. The different SPWM techniques include the Phase Disposition PWM (PDPWM) technique, Phase Opposition Disposition PWM (PODPWM) technique, Alternate Phase Opposition Disposition PWM (APODPWM) and Level Shifted multi carrier PWM (LSPWM) modulation techniques[20,21]. Multicarrier modulation techniques offer easy implementation mechanism compared to the other modulation strategies.

This work focuses on the analysis of a five levels Neutral Point Clamped (NPC) inverter. The inverter comprises of two voltage sharing capacitors and eight IGBT switches. Four clamping diodes are embedded with the IGBT switches and due to the three accessible DC potentials; the topology is able to generate five levels on the output. The NPC inverter unlike a conventional H-bridge inverter provides nine possible switching states, due to which better modulations can be achieved. Further, the five levels neutral point clamped structure requires one source unlike a conventional five levels CHB inverter which requires an individual source for each H-bridge and require eight switching devices. In this work, PDPWM modulation technique is used to produce switching pulses. The output voltage/current, switching stress and harmonic spectra is obtained for the five levels NPC inverter for a modulation index of unity. Further a comparison is established between the performance of a NPC inverter and a conventional five levels CHB inverter. MATLAB-Simulink is used to perform all the simulations.

This work is organized as follows: Section 2 describes the five levels CHB inverter. Section 3 discuses on the Neutral Point Clamped topology. Section 4 gives the simulation results followed by conclusion.

2. Five Levels CHB Multilevel Inverter

Figure 1 shows the five levels CHB multilevel inverter. Two separate DC power supplies are provided to two of the H-Bridges connected in series. The multilevel inverter switches are operated in five modes such that five levels of output as $+v_{dc}$, $^{+v_{dc}}/_{2}$, 0, $-{}^{v_{dc}}/_{2}$, $-v_{dc}$ are obtained.

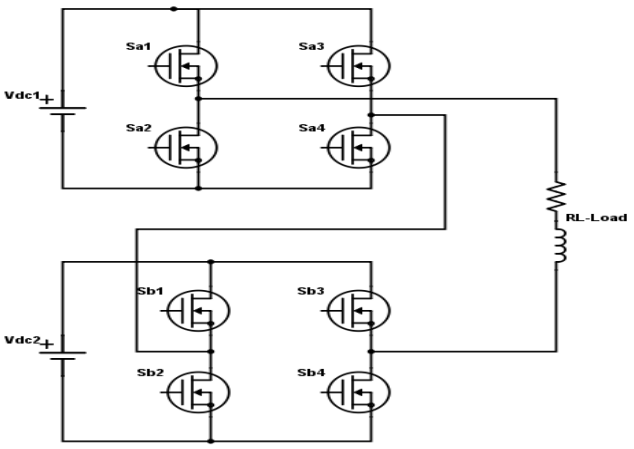

Figure 1. Five levels Cascaded H-Bridge multilevel inverter.

Table 1 shows the eight switching states of the five inverter to produce five levels of output[12–14]. For obtaining $+v_{dc}$, switches, S_{a1} , S_{a2} , S_{b1} and S_{b2} are ON and the other switches are OFF. In mode II, to obtain a voltage of $^{+v_{dc}}/_{2}$, except S_{a1} and S_{a2} all other switches are in the OFF state. S_{a4} and S_{b4} are the two switches which are in ON condition and rest in OFF condition in mode III and would not produce any voltage. While the

inverter is operated in mode IV to get $-{}^{v_{dc}}/_{2}$, switches S_{a3} and S_{a4} are ON and rest of the switches is in OFF state. Since mode V is complement of mode I, the switches, S_{a3}, S_{a4}, S_{b3} and S_{b4} are in ON state and remaining are in OFF state to get voltage level of $-v_{dc}$. The switch is in ON position when '1' and OFF when '0'.

Table 1. Modes of operation of five levels CHB multilevel inverter

V_0	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{b1}	S_{b2}	S_{b3}	S_{b4}
$+v_{dc}$	1	1	0	0	1	1	0	0
$+{}^{v_{dc}}/_{2}$	1	1	0	0	0	0	0	0
0	0	0	0	1	0	0	0	1
$-{}^{v_{dc}}/_{2}$	0	0	1	1	0	0	0	0
$-v_{dc}$	0	0	1	1	0	0	1	1

Figure 2 shows that the five levels of output are obtained by employing PDPWM technique. In this method, one reference wave and four carrier wave signals are compared to generate gate pulses which are used to drive the inverter switches. The carrier signals are arranged such that all of them are in phase with equal magnitude and are arranged one above the other. These carrier signals are compared with a reference sine signal to obtain switching pattern shown in Table 1.

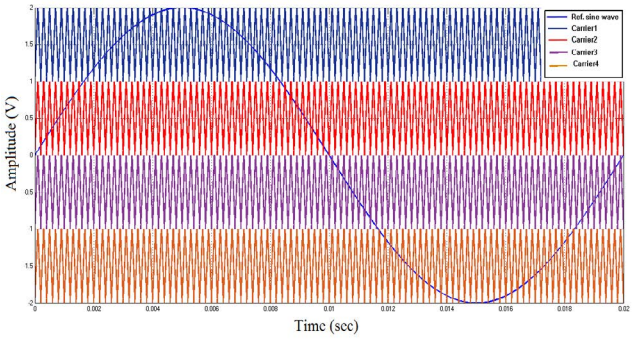

Figure 2. Multicarrier sinusoidal PWM technique.

Figure 3 shows the pulses generated out of the comparison. The output of the five levels CHB inverter is expressed using Fourier series expansion. The Fourier series representation of a double variable controlled waveform (reference and carrier waveform) is given by Equation (1). The Fourier series for a waveform f (a,b_1)) which varies as a function of two variables is:

$$f\ (a, b_1) = \frac{x_0(b_1)}{2} + \sum_{n=1}^{\infty} [x_n(b_1)cosna + y_n(b_1)sinna] \quad (1)$$

$$x_n(b_1) = \frac{1}{\pi}\int_{-\pi}^{\pi} f(a, b_1)cosna\ da \quad (2)$$

$$y_n(b_1) = \frac{1}{\pi}\int_{-\pi}^{\pi} f(a, b_1)sinna\ da \quad (3)$$

Here n = 0, 1, 2……

The coefficients $x_n(b_1), y_n(b_1)$ are two functions which are vary over 'b'.

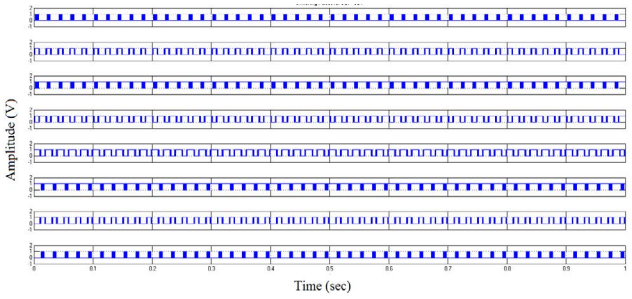

Figure 3. Gate signals for switches Sa1-Sb4.

3. Five Levels NPC Multilevel Inverter

Figure 4 shows a five levels NPC inverter. It consists of two inverter legs each having four IGBTs. Two series connected diodes are connected across the two switches of each leg and are shorted at the neutral point.

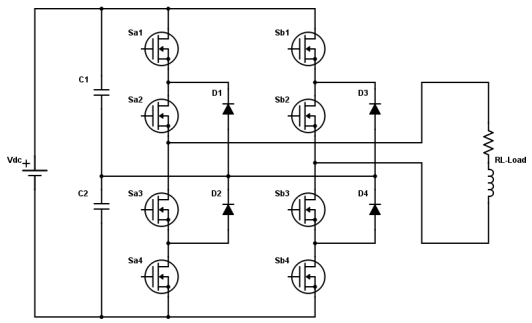

Figure 4. Five levels NPC multilevel inverter.

Table 2 shows the different switching states possible in a NPC inverter. The inverter is operated as per modes presented in Table 2 to get five levels[6–9]. The five levels of output voltage is $+v_{dc}, {}^{+v_{dc}}/_{2}, 0, -{}^{v_{dc}}/_{2}, -v_{dc}$. The

switches, S_{a1}, S_{a2}, S_{b3} & S_{b4} are in ON position and remaining Switches are in OFF position in mode I. S_{a1}, S_{a2}, S_{b3} and S_{b2} are in ON and others are in OFF position in mode II. S_{a2}, S_{a3}, S_{b3} **and** S_{b4} switches are in ON position and remaining are in OFF position in mode III. S_{a1}, S_{a2}, S_{b1} and S_{b2} are in ON position and others are in OFF position in mode IV. S_{a2}, S_{a3}, S_{b2} and S_{b3} are in ON state and remaining switches are OFF in mode V. Switches, S_{a3}, S_{a4}, S_{b3} and S_{b4} are in ON state and other switches are in OFF state in mode VI. S_{a2}, S_{a3}, S_{b1} and S_{b2} are ON and others are made OFF in mode VII. In mode VIII, switches S_{a3}, S_{a4}, S_{b2} **and** S_{b3} are in ON position and remaining switches are in OFF position. In mode IX the switches, S_{a3}, S_{a4}, S_{b1} **and** S_{b2} are made ON and other made OFF. The output voltage for different switching pattern is given in Table 2.

Table 2. Modes of operation of five levels NPC multilevel inverter

V_0	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{b1}	S_{b2}	S_{b3}	S_{b4}
$+v_{dc}$	ON	ON	OFF	OFF	OFF	OFF	ON	ON
$+v_{dc}/_2$	ON	ON	OFF	OFF	OFF	ON	ON	OFF
$+v_{dc}/_2$	OFF	ON	ON	OFF	OFF	OFF	ON	ON
0	ON	ON	OFF	OFF	ON	ON	OFF	OFF
0	OFF	ON	ON	OFF	OFF	ON	ON	OFF
0	OFF	OFF	ON	ON	OFF	OFF	ON	ON
$-v_{dc}/_2$	OFF	ON	ON	OFF	ON	ON	OFF	OFF
$-v_{dc}/_2$	OFF	OFF	ON	ON	OFF	ON	ON	OFF
$-v_{dc}$	OFF	OFF	ON	ON	ON	ON	OFF	OFF

Figure 5 shows the gate pulses generated for switches Sa1 to Sb4. To realize five levels of output from the NPC inverter, PDPWM modulation technique is used. As shown in Figure 2, in PDPWM technique a single reference wave is compared with the multiple carrier wave signals to get required number of levels. If the sine wave is greater than "carrier1" then Sa1 is made ON and Sa5 is made OFF. If the reference sine wave is lesser than "carrier1", then switch Sa5 is ON and Sa1 is made OFF, to get output level of +Vdc. If the sine wave is greater than the carrier signal, "carrier2" then the switch Sa3 is operated in the ON state and Sa7 is operated in the OFF state. If the sine wave is lesser than "carrier2", then the switch Sa3 is made ON and Sa7 is made OFF to get output as +Vdc/2. In case of reference sine wave greater than "carrier3" switch Sa2 becomes ON and Sa4 is OFF. If the reference sine wave is lesser than "carrier3", then switch Sa2 becomes ON and Sa4 is OFF, to reach the output level of -Vdc/2. If the reference sine wave is greater than "carrier4," then the switch Sa4 is in ON state and Sa8 is in OFF state. If the sine wave is lesser than "carrier4", then switch Sa4 is in ON state and Sa8 is in OFF state to reach output level of -Vdc/2.

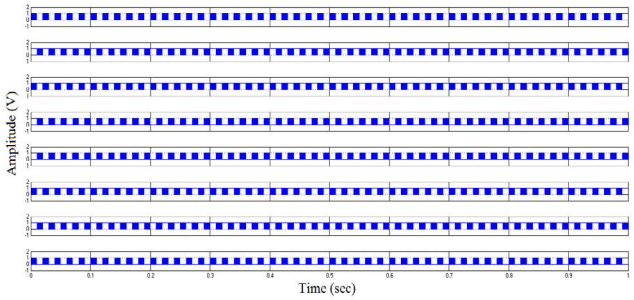

Figure 5. Gate signals for switches Sa1-Sb4.

4. Simulation Results

The simulation of the five levels NPC and CHB inverters are done in MATLAB-Simulink simulation tool. The simulations are performed assuming that the modulation index is 1 and switching frequency is 5 kHz for both the inverter topologies.

Table 3 shows the simulations parameters. The load voltage, load current, voltage stress harmonic spectrum are captured for each inverter.

Table 3. Simulation parameters

DC voltage($V_{\downarrow DC}1 + V_{\downarrow DC}2$)	**100V**
Modulation index(m)	1
Switching Frequency	5 KHz
RL load	50Ω, 12.6mH

Figure 6 presents load voltage and current waveforms for a modulation index of unity. It is seen that the output voltage waveform has synthesized five levels of output and the load current is nearly sinusoidal due to nature of the load.

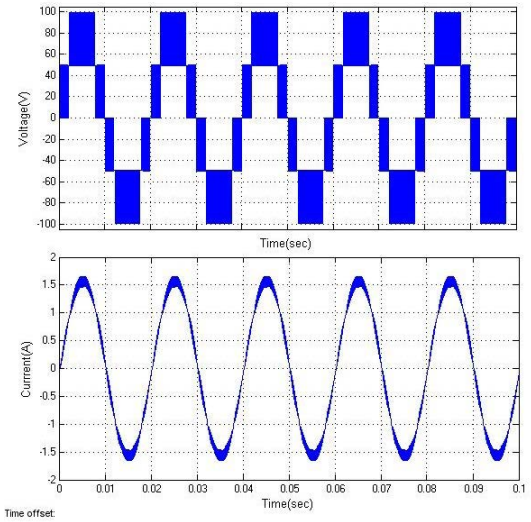

Figure 6. Output voltage and current of CHB multilevel inverter.

4.1 Output Waveforms of CHB Multilevel Inverter

Figure 7 indicates the switching stress of the single phase five levels inverter for a modulation index of 1. With the 100 V as input, the stress across each switch is 50 V. Only half of the input voltage gets applied across each switch thereby decreasing the switching stress.

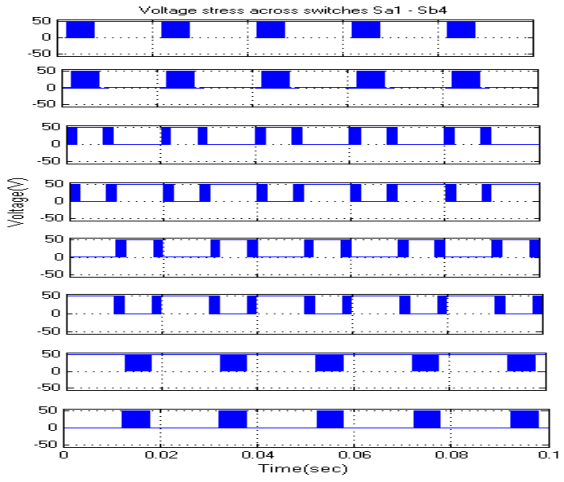

Figure 7. Voltage stress across the switches Sa1-Sb4 of CHB multilevel inverter.

Figure 8 presents the output harmonic spectrum. It is observed that the THD is 27.14% for the voltage and that for the current waveform is 2.92%. The magnitude of the harmonics is high near to the switching frequency of 5 KHz and the percentage of fundamental is 100.

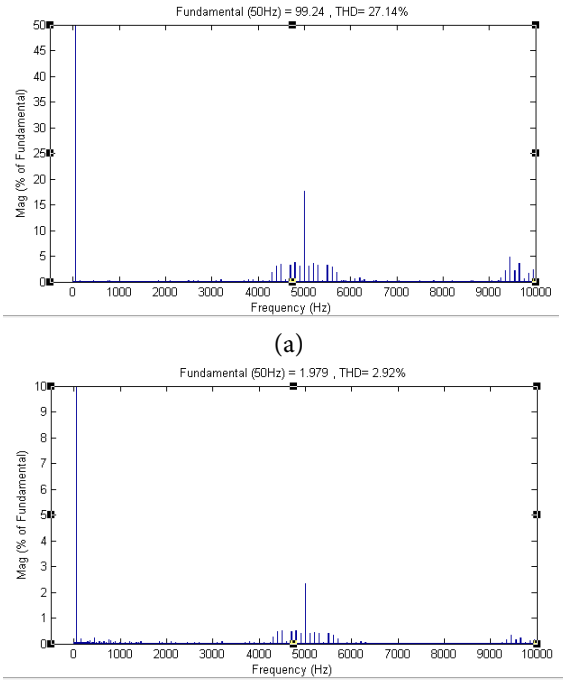

Figure 8. Harmonic spectrum obtained with CHB multilevel inverter
(a) Output voltage and (b) Output current.

4.2 Output Waveforms of NPC Multilevel Inverter

Figure 9 shows the load voltage and current waveforms of the NPC inverter for a modulation index of unity. It is seen that the output voltage waveform has synthesized five levels of output. The load current is nearly sinusoidal due to the nature of the load.

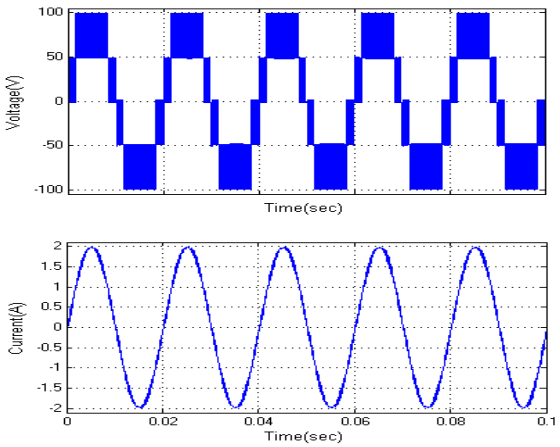

Figure 9. Output voltage and current of NPC multilevel inverter topology.

Figure 10 shows the stress across each switch of the NPC inverter for a modulation index 1. This also confirms that the voltage stress across each switch of the NPC inverter is about 50% of the supplied voltage.

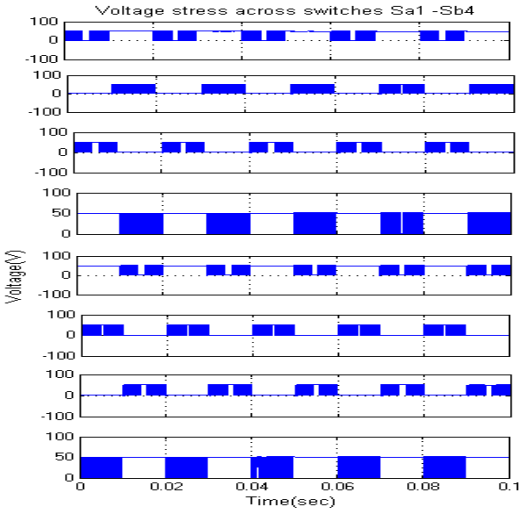

Figure 10. Voltage stress across the switches of NPC multilevel inverter.

Figure 11 presents the harmonic spectrum. It is observed that the THD is 27.14% for the output voltage and that for the current waveform is 2.92%. The magnitude of the harmonics is high near to the switching frequency of 5 KHz which is as expected.

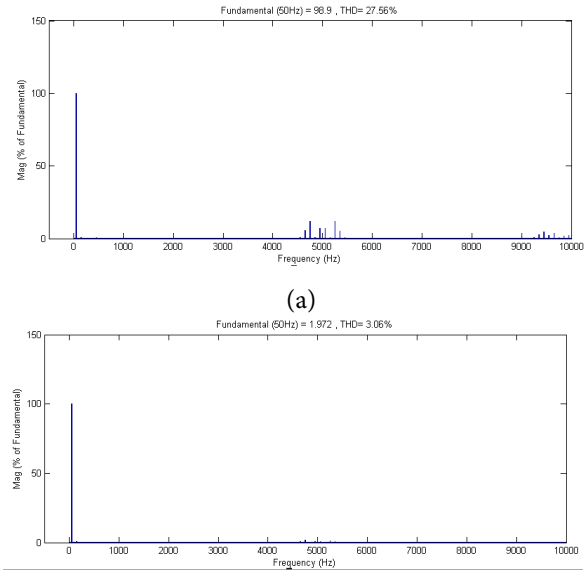

Figure 11. Harmonic spectrum of NPC multilevel inverter topology
(a) Output voltage and (b) Output current.

Table 4 shows the comparison of the THD in both voltage and current waveforms of the NPC and CHB inverters. It can be seen that both the inverters produce almost the same THD on the load voltage and load current waveforms, except for a small reduction in the CHB inverter.

Table 4. Comparison of THD for CHB and NPC multilevel inverters

Modulation index(m)	Topology	Voltage THD	Current THD
1	NPC	27.56%	3.06%
1	CHB	27.14%	2.92%

Table 5 gives an overview of these switching stresses for each of the switches of both the multilevel inverters. As only half of the switches are operated at a particular instant, the switches in both the CHB and NPC inverter will have to withstand only half of the stress. It can also be concluded that since soft switching action taken place in both the multilevel inverters, they make better option for high voltage applications.

Table 5. Comparison of switching stress for CHB multilevel inverter and NPC multilevel inverter

switches	Total input voltage for CHB (V)	Stress across the switch (V)	Input voltage for NPC (V)	Stress across the switch (V)
S_{a1}	100	50	100	50
S_{a2}	100	50	100	50
S_{a3}	100	50	100	50
S_{a4}	100	50	100	50
S_{b1}	100	50	100	50
S_{b2}	100	50	100	50
S_{b3}	100	50	100	50
S_{b4}	100	50	100	50

5. Conclusion

In this work, the analysis of two five levels inverter topologies is presented. Four clamping diodes, two voltage balancing capacitors, eight IGBT switches and one DC source are employed for a NPC inverter, whereas in the case of a CHB inverter topology two voltage sources and eight IGBT switching devices are used. PDPWM technique is used to create gating instants for both the

multilevel inverter topologies. A unity modulation index and a switching frequency of 5 kHz is considered for capturing output waveforms, switch stress and the harmonic spectrum of the output waveforms of both the inverter topologies. Further, both the inverter topologies are compared with respect to total harmonic distortion, switch stress and complexity of the topology. It is found that though a CHB inverter topology needs a lesser number of overall components when compared to a NPC inverter, yet both the inverter topologies carries the same stress across their switches and produce an almost the same harmonic distortion on their output waveforms. NPC inverters carry the advantage of requiring only one DC source for its operation.

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