Indian Journal of Science and Technology, *Vol 7(S6), 82–86, October 2014*
ISSN (Print) : 0974-6846
ISSN (Online) : 0974-5645

Energy Efficient Voltage Conversion Range of Multiple Level Shifter Design in Multi Voltage Domain

S. Sinthuja[1*], J. Harish Kumar[2] and N. Manoharan[3]

[1]Department of Tejas research Centre of excellence, AMET University, Kanathur, Chennai-603112, India; sinthuja.engg@gmail.com, Directorresearch@ametuniv.ac.in
[2]Department of Mechanical Engineering, AMET University, Chennai, India; harishkumarj20@gmail.com
[3]AMET University, India

Abstract

Level shifter is inserted between two modules when low voltage drives high voltage modules. Multi supply voltage is used to reduce the static and dynamic power consumption. Multi supply voltage domain technique consists of portioning the design into separate voltage domain. So the time critical domain runs at higher power supply voltage where non-critical domain is runs at lower power supply voltage. The conventional differential cascade voltage switch is the level shifter circuit. The conventional multi threshold CMOS (MTCMOS) greatly reduces the leakage power. But it does wide voltage conversion range is not achieved in level shifter design. So we use a multiple level shifter instead of single level shifter with multi threshold CMOS device. The multiple level shifter design can be achieved the conversion voltage range of 1V to 1.8V. The inter mediate power supply voltage of level shifter contains 400mV,600mV.800mV ranges of operation. It can be designed by using cadence 180nm technology. The synthesis results can be achieved in 310µW power supply.

Keywords: Differential Voltage Cascade Switch, Multi Threshold CMOS, Multiple Level Shifter, Wide Voltage Conversion Range

1. Introduction

In modern VLSI technology, SOC design has building blocks of component (analog, digital, mixed single chip). Each component of a chip has operating at proper power supply voltages. For communications among the different voltage domain, time critical domain runs at higher power supply and non critical domain runs at lower supply voltage. .Level shifter is needed when signal passes from low level logic to high level logic. So the level shifter can be placed between these two voltage domains (low-to-high). Inverter is enough when signal passes from high level logic to low level logic. No need level shifter between these two voltage levels (high-to-low). Differential cascade voltage switch is the level shifter circuit. Multiple threshold CMOS circuit is acts in low voltage and high voltage domain. If low voltage domain directly drives a high voltage domain leads to product failure and speed will affects greatly. Multi threshold CMOS IS used to reduce the leakage power and increase the speed of the level shifter circuit. The proposed multiple level shifter circuit between two voltage domain achieve the better conversion range of operation compared to single level shifter and MTCMOS technique.

**Author for correspondence*

Zhai. et al. used to convert the circuit from 200mV to 1.2V. it consists of three intermediate stages of conversion between two voltage domain. The major drawback of the circuit is increasing the power dissipation.[13]

S.Lutkemeir et al. proposed DCVS circuit by using 90-nm technology. It contains multiple level shifter circuit is used to employ supply voltage range from 200mV to 1.2mV. it has to increase the power consumption.[12]

Wooter[7] estimate the conversion range of the circuit is 188mV t 1.2V. The advantage of this design is number of PMOS transistor is tied to Vdd. So it can easily weakening the pull up network. The main drawback of this circuit is it contains only two stages, both stages uses only cross coupled differential inverter. So it requires more leakage power consumption.

Marco Lauzza, Pasqule corsonella, stefania perri describes the low power level shifter. The logic voltage has shifted in the range of 180mV input signal into 1.8V. it has to proposed by using 90-nm technology. The advantage of this circuit is minimizing the leakage power by using MTCMOS technique in DCVS circuit. Another advantage is guarantee a wide voltage conversion range of power supply. The drawback of this design is using a dual supply voltage. It leads more power consumption compared to the single supply voltages.[4]

2. Conventional Level Shifter

2.1 Differential Cascade Voltage Switch as Level Shifter Circuit

The traditional Level shifter design is the differential cascade voltage switch (DCVS) circuit, as shown in Figure 1. It consists of two PMOS transistors (MP2 and MP3) and a pair of NMOS transistors. It can be operated by the differential low-voltage input signals A and AN. When the input voltage A (AN) goes from low (high) to high (low), MN2 (MN3) is turned on (off). As a consequence, the voltage at node NH (NL) is pulled down, leading MP3 (MP2) to be turned on. This occurs when NH (NL) voltage reaches VDDH-Vth, MP3 (VDDH-Vth,MP2)[4]. Once MP3 (MP2) is turned on, the node NL (NH) starts to be charged, weakening MP2 (MP3).As a consequence, pull-up and pull-down strengths need to be properly balanced to assure correct functionality. Information for all authors. Include full mailing addresses, telephone.

The main drawback of the Differential cascade voltage switch circuit leads large power penalties. So we need to require multiple power switching to generate intermediate high voltage devices Level shifter with Multi threshold CMOS technique. It does not contain the intermediate power line.

2.2 Level Shifter with Multi Threshold CMOS Circuit

Figure 2 represents the implementation of multi threshold CMOS is to reduce the power consumption. The input inverter is used for low threshold device. The main voltage conversion stage consists of differential cascade voltage

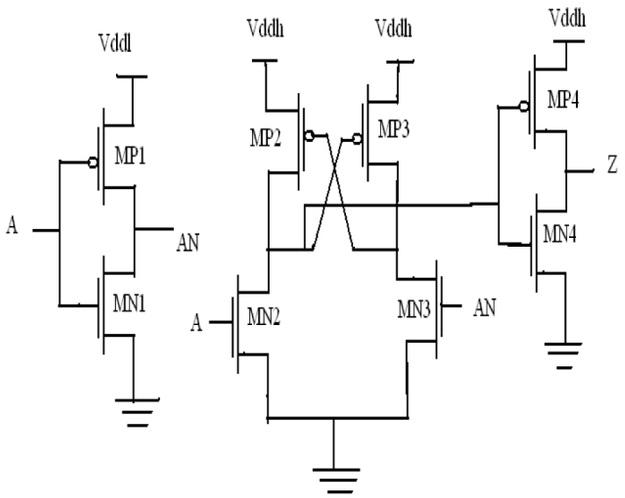

Figure 1. Differential cascade voltage switch level converter circuit.

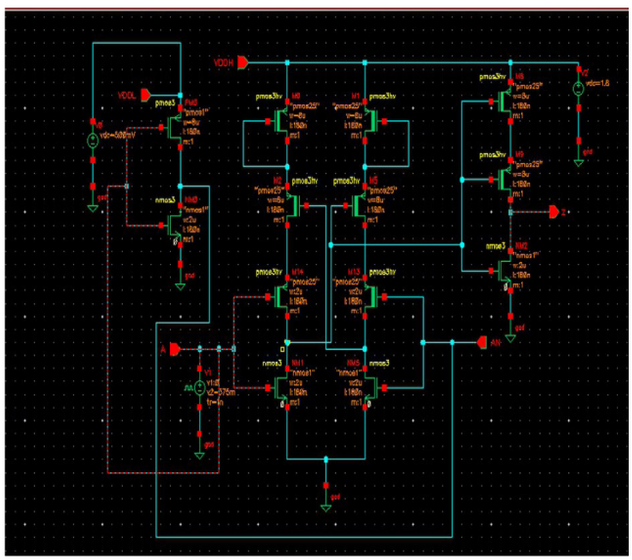

Figure 2. Level shifter with multi threshold CMOS technique.

switch circuit with multi threshold CMOS Transistor to provide fast differential low-voltage input signals and to increase the strength of the pull-down network of the main voltage conversion stage. MTCMOS technique is used to reduce the subthreshold leakage level. When MP4 is turned on, MP5 is consequently turned off. In this case, the small leakage current flowing through MP5 is not enough to turn MP7 on. For this reason, MP5 results power gated from the VDDH power rail, leading to a significant reduction in its sub-threshold current.

2.3 Multi-threshold CMOS

Multi threshold circuit contains low threshold and high threshold function. MTCMOS technique is used on high Vt transistors in level shifter circuit. It is used to reduce leakage and increase the speed of the level shifter.

It does allow high-speed performance to be achieved compared to the differential cascade voltage switch as a level shifter circuit. The draw back of the circuit is the voltage conversion is greatly affected particularly in level shifter stage.

3. Proposed Multiple Level Shifter with Multi Supply Voltage

Figure 3 shows the multiple level shifter circuit. Multiple supply voltage is applied to the circuit. Instead of multi threshold CMOS transistor multiple level shifter circuit is used in different voltages.It consists of multiple level shifter with multi supply voltage. The proposed design contains 3 stages of differential cascade voltage switch level shifter circuit. Each stage of level shifter operates from low voltage to high voltage level. Each stage operates at different power supply voltage. first stage operates at 400mV power supply, second stage operates at 600mV power supply, third stage operates at 800mV power supply. 1V power supply is used to drive all stages of leveel shifter circuit.

4. Design of Multiple Level Shifter Circuit

4.1 Low Voltage Domain

In a low voltage domain 1V supply voltage is given to the input inverter. 1V supply voltage will drive the level shifter circuit of main voltage conversion range. So the output of the inverter will be applied to the input of the level shifter circuit.

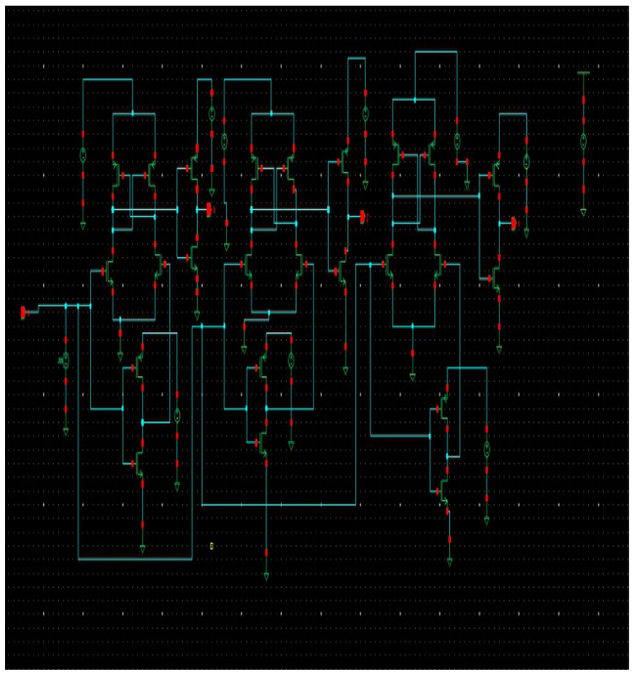

Figure 3. Proposed multiple level shifter with multi supply voltage.

4.2 Main Voltage Conversion Stage

It consists of three differential cascade voltage switch circuit connected to each other. To increase the effective voltage conversion range from one voltage domain to another voltage domain and to increase the speed of the level shifters. We introduce a different level shifter with different supply voltage instead of single level shifter with MTCMOS technique. The level shifter can act thee supply voltage of 400mV,600mV,800mV of proper power supply range. Each stages of the level shifter will operate from low to high operations.

4.3 High Voltage Domain

The output stage of the inverter is act as a high voltage domain. The output of the final stage of the level shifter is given to the input of the high voltage inverter.

5. Results and Discussions

The proposed design contains 3 stages of differential cascade voltage switch level shifter circuit. Each stage

of level shifter operates from low voltage to high voltage level. Each stage operates at different power supply voltage. first stage operates at 400mV power supply, second stage operates at 600mV power supply, third stage operates at 800mV power supply. 1V power supply is used to drive all stages of leveel shifter circuit. It can be done by cadence design tool 180nm technology. the above digram will achieve the effective conversiion range of each stage of level shifter design. The propoer power supply voltage is applied to alll level shifter circuit. The static and dynamic power dissipationj can be achieved in the above level shifter design circuit.

The Figure 4 shows the static analysis of the proposed multiple circuit. It shows all level shifter design is achieved the proper supply voltages from 1v to 1.8V.

The Figure 5 shows the logic level shifting of proposed multiple level shift circuit. It can be designed by using cadence 180nm technology.

The logic level can be shifted from 1V to 1.8V. The voltage level of the input to the output is achieved from 1V to 1.8V in between 400mV,600mV,800mV power supply can be achieved.

The power dissipation of the proposed LS circuit can be expressed as

$$\text{Static power} = I_{AVG}\ VDDH \quad (1)$$

$$\text{Dynamic power} = CL\ V^2DDH\ f_{IN} \quad (2)$$

Where I_{AVG} is the average current flowing through the circuit. Equation (1) shows that P is independent of

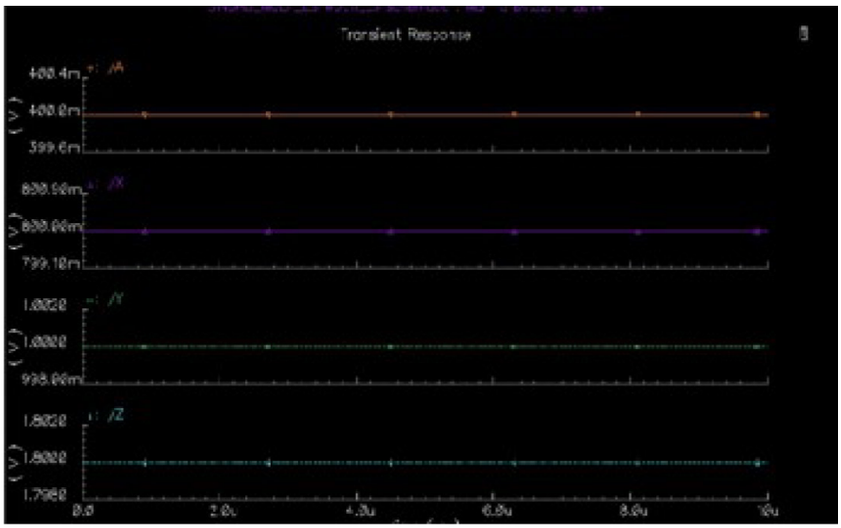

Figure 4. Static analysis of proposed multiple level shifter circuit.

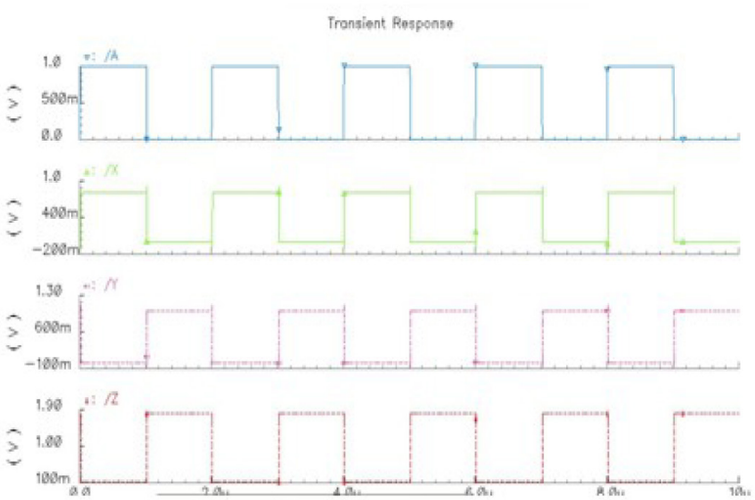

Figure 5. Logic level of Proposed multiple level shifter output.

VDDL and depends on f_{IN} and the square of VDDH. Therefore average power calculation is expressed as

$$P_{AVG} = \alpha_{D\to1}, C_L, V_{DD}2\ f_{c[k]} \quad (3)$$

6. Table Formation

Table 1. Performance comparison table

	Supply voltage range	Predicted power consumption
Differential cascade voltage switch level shifter	375mV-1.8V	516mW
Differential cascade voltage switch with MTCMOS level shifter	1V-1.8V	1.56mW
Multiple differential cascade voltage switch level shifter	1V-1.8V	310μW

The circuit have been simulated in 180nm cadence design tool. The output level can be achieved an power can be calculated.

7. Conclusion

In this paper, comparison of various design of level shifter on the basics of output voltage, conversion range of operation, power consumption was made. The proposed multiple level shifters shows better conversion range of all conventional level shifter design and also it can be achieved minimum power consumption compared to the other.

8. References

1. Shrivastava M, Baghini MS, Gossner H, and Rao VR. Part I: Mixed-signal performance of various high-voltage demos devices. IEEE Trans Electron Devices. 2010; 57(2):448–57.
2. Gutnik, Chandrakasan AP. Embedded power supply for lowpower DSP. IEEE Trans Very Large Scale Integ.(VLSI) Syst. 1997; 5(4):425–35.
3. Klass F, Amir C, Das A, Aingaran K, Truong C, Wang R, Mehta A, Heald R, Yee G. 1 -V Power Supply High-speed Digital Circuit Technology with Multithreshold-Voltage CMOS. IEEE Journal of solid-state circuits. 1999; 34(5).
4. Lauzza M, Corsonell P, Prri S. Low power level shifter for multi supply voltage designs. IEEE Tras Circuits ad Systems-II: Express. 2012; 59(12).
5. Romli NB, Mamun M, Bhuiyan MAS, Husain H. Design of a Low Power Dissipation and Low Input Voltage Range Level Shifter in Cedec 0.18-μm Cmos Process. World Appl Sci J. 2012; 19 (8):1140–8.
6. Koo H, Seo J-H, Ko M-L, Kim J-W. A new level-up shifter for high speed and wide range interface in ultra deep sub micron. Proc IEEE Int Symp Circuits Syst; 2005; Kobe, Japan. p. 1063–5.
7. Wooters N, Calhoun BH, Blalock T. An energy-efficient sub threshold level converter in 130-nm CMOS. IEEE Trans Circuits Syst II Exp Briefs. 2010; 57(4):290–4.
8. Kumar P, Verma M, Lamba V. Low Power Level-Up Shifter for Reduction of Static Power Dissipation in CMOS Technology. 2012; 2(6).
9. Diril, Dhillonn AU, Chatterjee YS, Singh A. Level shifter free design of low power dual supply voltage CMOS circuits using dual threshold voltages. IEEE Transaction on very large scale integeration (VLSI) system. 13(5):1002–107.
10. Liu Z, kursun V. Leakage power charachterestics of dynamic circuits in nanometer CMOS technologies. IEEE Trans on circuits and systems: express brief. 2008; 53(8):692–6.
11. Shao H, Tsui C. A robust, input voltage adaptive and low energy consumption level converter for sub-threshold logic. Proc. 33rd ESSCIRC; 2007; p. 312–5.
12. Lütkemeier S, Rückert U. A subthreshold to above-threshold levelshifter comprising a wilson current mirror. IEEE Trans Circuits Syst II, Exp Briefs. 2010; 57(9):721–4.
13. Zhai B, Pant S, Nazhadali L, Hanson S, Olson J, Reeves A, Minuth M, Helfand R, Austin T, Sylvester D, Blaauw D. Energy efficient subthreshold processor design. IEEE Trans (VLSI) Syst. 2009; 17(8):1127–37.